

Abstract

An image buffer is described for an $X \times Y$ pixel display, which image buffer stores compressed image pixel data for a plurality of $n \times m$ matrices of pixels, each matrix represented by a pair of color codes and MASK having nm bit position, each positions mapping to a pixel in the matrix, a manifested bit value in a MASK bit position defining the color code assigned to a mapped pixel. The image buffer includes serial registers for feeding pixel color code values to a buffer serial output and multiplexers for providing n bit values from the MASK on n of its output lines. Gating circuitry, controlled by bit values on the output lines, are operative to gate either a first set of inputs or a second set of inputs into the shift registers. Control circuitry is provided for feeding a pair of color codes and the MASK bit values to the gating circuits and multiplexers, respectively, and for serially operating the serial shift registers in response to the gating of the inputs from the gating circuits.

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