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PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Semiconductor Device and Method of Making Same

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to semiconductor devices, and more particularly but not solely to an improved metal-oxide-semiconductor field effect transistor and a novel method of making it. The improved field effect transistor is particularly useful in ultra high frequency (uhf) circuits, and the novel method is particularly useful for making integrated circuits.

One type of field effect transistor of the depletion type has a conduction channel of low resistivity in semiconductor material of one conductivity type. It also has two spaced-apart electrical contact regions, referred to as the source and the drain, respectively, connected to opposite ends of the conduction channel. This transistor also includes a gate electrode adjacent to, and electrically insulated from, the conduction channel. When a voltage is applied between the source and the drain, current flows through the conduction channel. The amplitude of the current can be modulated by voltage signals applied to the gate electrode.

Two basic types of field effect transistors are the depletion type and the enhancement type. In the enhancement type, the channel is electrically induced by the application of an external forward bias to the gate electrode, and no current flows with a zero or back bias on the gate electrode. This application deals with the

depletion type, which contains a conduction channel that allows current to flow from the source to the drain with zero bias on the gate electrode. The current may be controlled with either a back bias or a forward bias on the gate electrode.

In many prior art, depletion type, field effect transistors, the conduction channel between the source and the drain is in semiconductor material of one conductivity type and the drain and source contacts are regions of an opposite conductivity type. This forms back-to-back diodes (P-N junctions) between the source and drain. The use of P-N junctions between the source and drain electrodes and the bulk of the semiconductor body is desirable so that most of the source-drain current can be confined to the extremely thin inversion layer at the surface of the channel. While these prior art field effect transistors are suitable for many applications, some have an output capacity and leakage currents that may be unsuitable for certain applications.

The maximum amplitude of the bias voltage that may be safely applied to the gate electrode of a field effect transistor is limited by the breakdown potential of the dielectric material between the gate electrode and the conduction channel. The conduction channel should, therefore, have a relatively small cross-sectional area to enable current to be pinched off by a back bias voltage of a tolerated amplitude.

In a depletion type field effect transistor, the magnitude of gate back bias voltage required to completely pinch off current in the conduction channel is directly proportional to the depth of the channel. On the other hand, the maximum amplitude of bias voltage that can be safely applied to the gate electrode is limited by the breakdown potential of the dielectric material between

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the gate electrode and the surface of the channel. In order not to exceed the safe bias voltage limit on the gate electrode, the depth of the conduction channel should not be too large.

Therefore, it is an object of the present invention to provide an improved semiconductor device and a method for making the device which comprises a single crystal and associated electrode regions of semiconductor material of only one conductivity type, thereby eliminating P-N junctions.

According to the invention we provide a method of making a semiconductor device comprising the steps of fixing a wafer of lightly doped monocrystalline semiconductor material to a support member by means of electrically insulating bonding material, removing portions of said supported wafer until said wafer has a relatively uniform thickness of 4 microns or less, arranging a layer of insulating material on said supported wafer, making two spaced-apart openings in said layer of insulating material to expose two portions on the upper surface of the wafer, adding a dopant in each of said two exposed portions to provide regions of relatively high conductivity of the same conductivity type as said lightly doped semiconductor material and arranging electrically conductive contacts respectively on said two regions of relatively high conductivity and on a portion of said layer between said two regions.

Further, according to the invention we provide a semiconductor device comprising a support member insulated from or separated by an insulating layer from a high resistivity monocrystalline layer of semiconductor material, two spaced-apart regions, of relatively low resistivity semiconductor material of the same conductivity type as said monocrystalline layer forming a source and a drain in said layer, and an insulated gate electrode arranged to control current flow between said source and drain.

In the accompanying drawings:

FIGURE 1 is a perspective view of a wafer of semiconductor material used in the method of making a field effect transistor according to the present invention;

FIGURE 2 is a fragmentary, front-elevation view of the wafer of semiconductor material illustrated in FIGURE 1, showing one major surface thereof with an insulating, oxide layer thereon;

FIGURES 3, 4, 5 and 6 are fragmentary, enlarged, cross-sectional views of a pair of bonded wafers of the type shown in FIGURE 1 during successive steps in the fabrication of a semiconductor device in accordance with the invention;

FIGURE 7 is an enlarged, cross-sectional view of a semiconductor device in accordance with the present invention, and;

FIGURE 8 is a schematic diagram of an amplifier circuit employing a semiconductor device which is an embodiment of the present invention.

Referring to the drawings and more particularly to FIGURE 1, there is shown a single crystal wafer 10, preferably of lightly doped, N-type silicon having a relatively high resistivity, of about 1 to 10 ohm-centimeters. Initially, the wafer 10 has a pair of opposed, parallel upper and lower major surfaces 12 and 14 spaced about 10 mils apart. Each of the surfaces 12 and 14 has an area of about 1 square inch. The semiconductor device according to the present invention is to be formed in the wafer 10 after it is reduced to a relatively uniform thickness of between .05 and 4 microns.

As pointed out above, we desire to pinch off current flow through the semiconductor device by a voltage of safe amplitude applied to its surface. To provide a thin wafer 10, two of the wafers 10 are fixed to each other. Thus, one wafer 10 can function as a support for the other wafer 10. The second wafer 10 can be ground and lapped to the desired cross-sectional dimension.

A preferred method for accomplishing this includes oxidizing at least one surface of each of a pair of wafers 10 to form an insulating oxide layer 16 of silicon dioxide as shown in FIGURE 2. The upper surface 12 of each of the wafers 10 may be oxidized by any suitable method known in the art, such as by heating for about 30 minutes in steam at a temperature of about 1050°C. The thickness of the silicon dioxide layer 16 formed should be about 25,000 Å (Angstrom units).

The two wafers 10 are now disposed with their oxide layers 16 against each other as shown in FIGURE 3. Heat is applied to them until the oxide layers 16 fuse together. The heating step may be carried out preferably in an induction furnace at a temperature of between 1,150 and 1,200°C. until fusion takes place. During the heating step, pressure is applied between the two wafers 10, in the directions indicated by the arrows 18 and 20 in FIGURE 3. The pressure may be within the range of from 500 to 1,000 psi. By using two wafers 10 of the same material, the fused wafers react similarly to changes in temperature, thereby producing a structure that is not damaged by changes in temperature.

Due to the fusing, the superimposed wafers 10 are fixed to each other by means of an electrically insulating layer 22 (FIGURE 4) of silicon dioxide. The layer 22 includes the two, fused, oxide layers 16 of the two wafers 10 shown in FIGURE 3. One of the wafers 10 (the top wafer 10

shown in FIGURE 3, for example), is now ground and lapped by any suitable grinding and polishing means known in the art, until the wafer 10 acquires a thickness of between .05 and 4 microns. This ground wafer will now be designated by the reference numeral 10a to represent the lapped wafer of single crystal N-type silicon, as shown in FIGURE 4.

The thickness of the wafer 10a may be measured progressively during the lapping process by periodic observation under a microscope employing a suitable graduated reticle. Also, the thickness of the wafer 10a can be calculated by angle lapping. That is, a corner of the lapped wafer 10a is lapped at a known angle to its parallel major surfaces and the length of the transverse surface is measured.

The upper surface 14a of the lapped wafer 10a is now oxidized by any suitable means, as by the aforementioned oxidation process until an oxide layer 24 (FIGURE 5) of silicon dioxide of about 2,000 Å in thickness is formed. Source and drain contact regions S and D, respectively, may be formed in spaced-apart regions of the wafer 10a by precision oxide masking and photolithographic techniques.

Thus, for example, a photoresist layer 26 (FIGURE 6) is deposited on the oxide layer 24, and the photoresist layer 26 is exposed to a suitable light pattern to provide openings in the oxide layer 24. The exposed photoresist layer 26 is now developed. The portions of the photoresist layer 26 that are not exposed to light are removed by means of a suitable solvent, thereby exposing portions of the oxide layer 24. The hardened polymerized portions of the photoresist that remain on the oxide layer 24 serve as a mask during the subsequent etching step.

The exposed portions of the oxide layer 24 are removed by a suitable etchant, such as a hydrofluoric acid solution to form openings 28 and 30 therein as shown in FIGURE 7. The polymerized portions of the photoresist layer 26 are removed by a suitable stripper, such as methylene chloride, leaving the oxide layer 24 with the pair of spaced-apart openings 28 and 30 through which suitable impurities may be diffused into the wafer 10a for forming source and drain contact regions S and D, respectively.

The exact size and shape of the openings 28 and 30 in the oxide layer 24 are not critical. Openings having a diameter within the range of 5 to 100 mils have been found to be satisfactory. The distance between the source and drain contact regions S and D should be about 10 microns. A suitable N-type impurity, such as phosphorus, arsenic, or antimony, for example, is now diffused into the lapped wafer 10a through the openings 28 and 30 to form the

source S and drain D contact regions.

The diffusion may be accomplished by any means known in the arts as by heating the wafer 10a in an ambient containing phosphorus pentoxide vapors for about 10 to 20 minutes at about 1,000°C. Under these conditions, phosphorus diffuses into the exposed regions S and D of the wafer 10a immediately beneath the openings 28 and 30. No P-N junctions are formed between the diffused source S and drain D regions and the wafer 10a since phosphorus is a donor element in silicon, and the wafer 10a is lightly doped, N-type silicon. The N-type impurity, phosphorus, is diffused completely transversely through the lapped wafer 10a so that the source S and drain D extend from the upper surface 14a of the wafer 10a to its lower surface 12a, as shown in FIGURE 7. The source S and drain D regions have a relatively low resistivity of about .001 ohm-centimeter.

Means are provided to form a metallic gate electrode G adjacent to, and spaced from, the portion of the wafer 10a between the source S and drain D contact regions. To this end, a conductive metal may be deposited by any convenient means over the oxide layer 24 between the source and drain.

In the embodiment of the invention shown in FIGURE 7, the conductive gate G comprises a layer of aluminum of about 5,000 Å in thickness that may be deposited over the oxide layer 24 by evaporation. Aluminum, for example, is first evaporated over the entire oxide layer 24 and over the source S and drain D contact regions. Portions of the deposited metal are next etched away, employing the aforementioned photolithographic technique of a photoresist and a selective etchant, from all areas except the source S, the drain D, and the gate contact regions.

Thus, the metallic (Aluminum) gate G is formed on the oxide layer 24 between the source S and the drain D, and metal (Aluminum) electrodes 32 and 34 are deposited over the source S and drain D regions. Suitable electrical conductors 36, 38 and 40 may be connected to the gate G, the source S, and the drain D electrodes G, 32 and 34, respectively, by any suitable means, as by soldering or thermocompression bonding, for example.

Referring, now, particularly to FIGURE 8, there is shown a schematic diagram of a field effect transistor 50 of the type illustrated in FIGURE 7 connected in an amplifying circuit. The gate electrode G of the transistor 50 is connected to an input terminal 52 through an input capacitor 54. The source S of the transistor 50 is connected to a common connection 56 through a bias resistor 58. An input terminal 60 and an output terminal 62 are also con-



nected to the common connection 56. The bias resistor 58 is shunted by a by-pass capacitor 64 to prevent degenerative current feedback.

- 5 The drain D of the transistor 50 is connected to an output terminal 66 through an output capacitor 68. The drain D is also connected to the positive terminal of a voltage source 70 through a load resistor 72, the negative terminal of the voltage source 70 being connected to the common connection 56. An input resistor 74 is connected between the gate electrode G and the common connection 56.
- 10 In operation, conventional current flows from the positive terminal of the voltage source 70 through the load resistor 72, the path between the drain D and the source S, the bias resistor 58, and returns to the negative terminal of the voltage source 70. Current flows from the drain D to the source S even with a zero signal voltage applied to the gate G. Positive or negative signals applied between the input terminals 52 and 60 modulate the current from the drain D to the source S, producing inverted, amplified, output signals between the output terminals 62 and 66.

Current flow between drain D and the source S can be pinched off by a negative input signal of a predetermined amplitude. This action is possible because the thickness of the wafer 10a is between .05 and 4 microns, and a tolerated negative voltage can pinch off the current flowing between the drain D and source S. As pointed out above a tolerated voltage is one that will not break down the oxide layer 24 of the silicon dioxide dielectric.

- 40 As indicated, an advantage of the method and device according to the present invention is that the layer of semiconductor material 10a is arranged on an insulating substrate, namely the silicon dioxide bonding layer 22. Thus, there is no output capacitance between the drain electrode and a substrate, nor are there P-N junctions or diodes arranged between the source and the substrate or the drain and the substrate.
- 50 Since the device is not limited by output capacitance, the high frequency response of the device is superior to those devices wherein such capacitance is present.

The device will also have remote cutoff characteristics since the pinch-off voltage can be very high due to the thickness of the conducting portion of the wafer 10a.

WHAT WE CLAIM IS:—

1. A method of making a semiconductor device comprising the steps of fixing a wafer of lightly doped monocrystalline semiconductor material to a support member by means of electrically insulating bonding material, removing portions of said supported wafer until said wafer has a rela-

tively uniform thickness of 4 microns or less, arranging a layer of insulating material on said supported wafer, making two spaced-apart openings in said layer of insulating material to expose two portions on the upper surface of the wafer, adding a dopant in each of said two exposed portions to provide regions of relatively high conductivity of the same conductivity type as said lightly doped semiconductor material and arranging electrically conductive contacts respectively on said two regions of relatively high conductivity and on a portion of said layer between said two regions.

2. A method of making a semiconductor device in accordance with claim 1, wherein said dopant is a donor impurity which is diffused into each of said exposed portions, said diffusion extending from said upper surface to the lower surface of said wafer.

3. A method of making a semiconductor device in accordance with claim 1, wherein said semiconductor material is lightly doped N-type silicon, said electrically insulating bonding material is silicon dioxide, said insulating material on said supported wafer is formed by oxidizing the upper major surface of the wafer and said dopant is diffused into said two exposed portions.

4. A method of making a semiconductor device in accordance with claim 1, wherein a pair of wafers of silicon are used, at least one surface of each of said pair of wafers being oxidized to form a first oxide layer of silicon dioxide on said one surface, one of said wafers being lightly doped single crystal silicon of one conductivity type, stacking said pairs of wafers with said oxide layer of one wafer against said oxide layer of the other wafer, heating and pressing together said stacked wafers until said oxide layers bind said pair of wafers together, lapping the upper surface of said one wafer to a relatively uniform thickness of 4 microns or less, oxidizing the upper surface of said lapped wafer to form a second layer of silicon dioxide thereon, making two spaced-apart openings in said second layer to expose two portions of the upper surface of said lapped wafer, diffusing an impurity of the same conductivity type as said one wafer into each of the said two portions to form regions of relatively high conductivity in said lapped wafer, said diffusion extending from the upper surface of said lapped wafer to the lower surface thereof and depositing metallic contacts, respectively, on said two regions and on a portion of said layer between said two regions.

5. A method of making a semiconductor device in accordance with claim 4, wherein said first oxide layer is about 25,000 Å thick, said resistivity of said single crystal silicon being from 1 to 10 ohm-centimeters,

nected to the common connection 56. The bias resistor 58 is shunted by a by-pass capacitor 64 to prevent degenerative current feedback.

5 The drain D of the transistor 50 is connected to an output terminal 66 through an output capacitor 68. The drain D is also connected to the positive terminal of a voltage source 70 through a load resistor 72, the negative terminal of the voltage source 70 being connected to the common connection 56. An input resistor 74 is connected between the gate electrode G and the common connection 56.

10 In operation, conventional current flows from the positive terminal of the voltage source 70 through the load resistor 72, the path between the drain D and the source S, the bias resistor 58, and returns to the negative terminal of the voltage source 70. Current flows from the drain D to the source S even with a zero signal voltage applied to the gate G. Positive or negative signals applied between the input terminals 52 and 25 60 modulate the current from the drain D to the source S, producing inverted, amplified, output signals between the output terminals 62 and 66.

Current flow between drain D and the 30 source S can be pinched off by a negative input signal of a predetermined amplitude. This action is possible because the thickness of the wafer 10a is between .05 and 4 microns, and a tolerated negative voltage 35 can pinch off the current flowing between the drain D and source S. As pointed out above a tolerated voltage is one that will not break down the oxide layer 24 of the silicon dioxide dielectric.

40 As indicated, an advantage of the method and device according to the present invention is that the layer of semiconductor material 10a is arranged on an insulating substrate, namely the silicon dioxide bonding layer 22. Thus, there is no output 45 capacitance between the drain electrode and a substrate, nor are there P-N junctions or diodes arranged between the source and the substrate or the drain and the substrate. 50 Since the device is not limited by output capacitance, the high frequency response of the device is superior to those devices wherein such capacitance is present.

The device will also have remote cutoff 55 characteristics since the pinch-off voltage can be very high due to the thickness of the conducting portion of the wafer 10a.

WHAT WE CLAIM IS:—

1. A method of making a semiconductor 60 device comprising the steps of fixing a wafer of lightly doped monocrystalline semiconductor material to a support member by means of electrically insulating bonding material, removing portions of said supported wafer until said wafer has a rela-

tively uniform thickness of 4 microns or less, arranging a layer of insulating material on said supported wafer, making two spaced-apart openings in said layer of insulating material to expose two portions 70 on the upper surface of the wafer, adding a dopant in each of said two exposed portions to provide regions of relatively high conductivity of the same conductivity type as said lightly doped semiconductor material 75 and arranging electrically conductive contacts respectively on said two regions of relatively high conductivity and on a portion of said layer between said two regions.

2. A method of making a semiconductor 80 device in accordance with claim 1, wherein said dopant is a donor impurity which is diffused into each of said exposed portions, said diffusion extending from said upper surface to the lower surface of said wafer. 85

3. A method of making a semiconductor device in accordance with claim 1, wherein said semiconductor material is lightly doped N-type silicon, said electrically insulating bonding material is silicon dioxide, said insulating material on said supported wafer is 90 formed by oxidizing the upper major surface of the wafer and said dopant is diffused into said two exposed portions.

4. A method of making a semiconductor 95 device in accordance with claim 1, wherein a pair of wafers of silicon are used, at least one surface of each of said pair of wafers being oxidized to form a first oxide layer of silicon dioxide on said one surface. 100 one of said wafers being lightly doped single crystal silicon of one conductivity type, stacking said pairs of wafers with said oxide layer of one wafer against said oxide 105 layer of the other wafer, heating and pressing together said stacked wafers until said oxide layers bind said pair of wafers together, lapping the upper surface of said one wafer to a relatively uniform thickness of 4 microns or less, oxidizing the upper 110 surface of said lapped wafer to form a second layer of silicon dioxide thereon, making two spaced-apart openings in said second layer to expose two portions of the upper surface of said lapped wafer, diffusing 115 an impurity of the same conductivity type as said one wafer into each of the said two portions to form regions of relatively high conductivity in said lapped wafer, said diffusion extending from the upper surface of said lapped wafer to the lower surface 120 thereof and depositing metallic contacts, respectively, on said two regions and on a portion of said layer between said two regions. 125

5. A method of making a semiconductor device in accordance with claim 4, wherein said first oxide layer is about 25,000 Å thick, said resistivity of said single crystal silicon being from 1 to 10 ohm-centimeters, 130





material

and one wafer being lapped to a relatively uniform thickness in a range between .05 and 4 microns, said second layer of silicon dioxide being about 2,000 Å thick and said relatively high conductivity regions having a resistivity of about .001 ohm-centimeters.

6. A method of making a semiconductor device substantially as described with respect to the accompanying drawings.

10 7. A semiconductor device comprising a support member insulated from or separated by an insulating layer from a high resistivity monocrystalline layer of semiconductor material, two spaced-apart regions, of relatively low resistivity semiconductor material of the same conductivity type as said monocrystalline layer, forming a source and a drain in said layer, and an insulated gate electrode arranged to control current flow between said source and drain.

25 8. A semiconductor device as claimed in claim 7 wherein the support member is of semiconductor material and has a substantially flat upper surface, said monocrystalline layer being fixed to said upper surface of said support member by an insulating layer, and said gate electrode being fixed to and insulated from the upper

surface of said monocrystalline layer between said spaced-apart regions by electrical insulating material.

9. A semiconductor device as claimed in claim 7 or 8, wherein the thickness of said monocrystalline layer is 4 microns or less.

10. A semiconductor device as claimed in any one of claims 7 to 9, wherein the semiconductor monocrystalline layer is N-type silicon which is electrically insulated from the support member by silicon dioxide insulating material.

11. A semiconductor device as claimed in any one of claims 7 to 10, wherein said monocrystalline layer of semiconductor material has a resistivity in the range of 1 to 10 ohm-centimeters and said spaced apart regions have a resistivity of about .001 ohm-centimeters.

12. A semiconductor device substantially as herein described with respect to the accompanying drawings.

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