AMENDED SPECIFICATION

Reprinted as amended in accordance with the Decision of the Superintending Examiner acting for the Comptroller General dated the first day of June, 1964, under Section 29 of the Patents Act, 1949.

PATENT SPECIFICATION

945,738



DRAWINGS ATTACHED

945,738

Date of Application and filing Complete Specification: Feb. 2, 1960.
No. 3836/63.
Application made in United States of America (No. 791,602) on Feb. 6, 1959.
(Divided out of No. 945,734.)
Complete Specification Published: Jan. 8, 1964.

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Index at acceptance:—H1 K(1A1, 1CX, 1D3A, 1D3B, 2S1, 2S2, 2S10, 2S20, 3E1, 3J, 3S, 4C, 4F8, 4F11, 5)

International Classification:—H 01 c, l.

COMPLETE SPECIFICATION

Miniature Semiconductor Devices and methods of producing same

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a semiconductor device and more particularly to electrical connections made to various regions on a surface of the semiconductor device.

The present invention is a semiconductor device comprising a body of semiconductor material containing first and second regions of opposite conductivity-types forming therebetween a first p—n junction extending to one surface of said body and there defining a first enclosed area of semiconductor material, said second region underlying said first region, the region immediately underlying said second region being of a conductivity-type opposite to that of said second region to form therewith a second p—n junction extending to said surface and there defining a second enclosed area of semiconductor material surrounding said first enclosed area, first and second contacts secured to said one surface upon opposite sides of said first p—n junction, said first and second contacts being ohmically connected respectively to said first and second enclosed areas, insulation material composed of a silicon oxide on said surface, a first electrical connection to said first contact including conductive material extending from said first contact over said insulation material and being positioned on said insulation material, and a second electrical connection to said second contact including conductive material extending from said second contact over said insulation material and being positioned on said insulation material.

The semiconductor device generally has a circuit element or elements formed closely adjacent one major wafer face and to fabricate the device there may be utilized a combination of steps such as diffusion of conductivity type producing ingredients into a semiconductor wafer, masking in order to define predetermined areas of the wafer in which circuit elements are to be formed and mechanical and/or electrical shaping to confine paths for current flow.

Circuit elements within or on the semiconductor wafer may be effectively electrically isolated through the advantageous employment of electrical and/or mechanical shaping.

Shaping includes various ways of obtaining confined current paths which ways include, as mechanical shaping, the removal of portions of the semiconductor material as by etching, and specialized configuration of the semiconductor material such as long and narrow, "L" shaped, "V" shaped, etc., and which ways further include, as electrical shaping, selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow and selec-

[*Price 4s. 6d.*]

tive conversion of semiconductor material of one conductivity-type to the opposite conductivity-type wherein the p—n junction thereby formed acts as a barrier to current flow.

The invention will be apparent from the following more complete discussion of the cooperative relationships which exist in the forming, shaping and positioning of an area or the various areas within a wafer of single crystal semiconductor material to produce a miniature semiconductor device with electrical connections to various regions on a surface of the wafer.

In the accompanying drawings:—

Figures 1 to 5*a* illustrate schematically various circuit components or elements, a number of which may be fabricated in accordance with the principles set forth in our copending patent application no. 3633/60 (Serial No. 945,734) from which the present application is divided in and/or on a wafer of single crystal semiconductor material to be adapted to form at least part of a miniature electrical circuit;

Figure 6*a* illustrates schematically a multivibrator circuit fabricated in accordance with the principles set forth in said aforementioned copending patent application;

Figure 6*b* shows the wiring diagram for the multivibrator circuit of Figure 6*a* laid out in the same relationship;

Figure 7 illustrates the wiring diagram of the multivibrator circuit of Figure 6*a* in a more conventional presentation;

Figure 8*a* illustrates schematically a phase shift oscillator fabricated in accordance with the principles set forth in said aforementioned copending patent application;

Figure 8*b* shows the wiring diagram for Figure 8*a* with the compounds laid out in the same relationship;

Figure 8*c* portrays the wiring diagram of the phase shift oscillator;

Figure 9 illustrates the semiconductor device of Fig. 6*a* modified in accordance with the present invention; and

Figure 10 illustrates a cross sectional view of the Fig. 9 embodiment taken along the line A—A.

Figures 1—5a inclusive illustrate in detail circuit elements which can be formed in and/or on a single wafer of semiconductor material. It is noted at this point that the wafer of semiconductor material is of single crystal structure, and can be composed of any suitable semiconductor material. There may be mentioned as example of suitable materials germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

Referring particularly to Figure 1, there is shown a typical design for a resistor which may be formed in a wafer of single crystal semiconductor material with at least one other circuit element. As noted in Figure 1, the design contemplates utilizing the bulk resistance of a body 10 of semiconductor material of either n- or p-type conductivity. Contacts 11 and 12 are made ohmically to one surface of the body 10, spaced apart a sufficient distance to achieve a desired resistance. As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in terms of resistance to flow of current therethrough in any suitable direction. If two resistors are to be connected together, it is not necessary to provide separate terminations for the common point. The resistance may be calculated from

$$R = \varrho L/A$$

where L is the active length in centimetres, A is the cross sectional area, and ϱ is the resistivity in ohm—cm of the semiconductor material.

In addition or alternatively to the resistor shown in Figure 1, a resistor may be provided as shown in Figure 1*a* formed as part of a wafer of single crystal semiconductor material. In Figure 1*a*, there is shown a body comprising a region 10*a* of p-type semiconductor material and an n-type region 10*b*. Of course, between the region 10*a* and region 10*b* there is a p—n junction which is designated by the numeral 13. Contacts 11*a* and 12*a* are made to the outside surface of the region 10*b*, spaced apart from each other in order to achieve a desired resistance. As in Figure 1, the contacts 11*a* and 12*a* are ohmic contacts to the region 10*b*. A resistor formed in the manner of Figure 1*a* has several important advantages. First, the p—n junction 13 provides a barrier to current flow from the n-type region 10*b* into the p-type region 10*a* and, thus, the current flow is confined to a path in the n-type region 10*b* between the contacts thereto. The second advantage is that the total resistance value thereof can be controlled to a large degree. The total resistance value may be controlled by etching very lightly over the entire surface to remove the uppermost portion of the n-type region 10*b*, being very careful not to etch through the p—n junction. The third, and perhaps major, advantage in forming a resistor according to Figure 1*a* is in that, by controlling the doping level or impurity concentration in the n-type region 10*b*, lower and more nearly constant temperature coefficients may be provided for the resistor.

The above description has been in terms of a p-type region 10*a* and an n-type region 10*b* but it is obvious that the region 10*a* could be equally as well of n-type conductivity and the region 10*b* of p-type conductivity.

Capacitor designs may be obtained by utilizing the capacitance of a p—n junction, as shown in Figure 2, wherein is shown a

semiconductor body comprising a region 15 of p-type conductivity and an n-type diffused region 16. Ohmic contacts 17 are made to opposite faces of the body 15, 16. The capacitance of a diffused junction is given by

$$C = A\epsilon\left(\frac{q\ a}{12\epsilon V}\right)^{\frac{1}{3}}$$

where A is the area of the junction in square cm, ϵ is the dielectric constant, q is electronic charge, where a is the impurity density gradient and V is the applied voltage.

Instead of the capacitor of Figure 2, capacitance in a body of single crystal semiconductor material may be provided as shown and described in connection with Figure 2*a*, which capacitor is the subject of our copending patent application no. 5691/62 (Serial No. 945,737). Figure 2*a* shows a body 15*a* of single crystal semiconductor material, of either n- or p-type conductivity, which constitutes one plate of the capacitor. Evaporated onto the body 15*a* is a layer 18 providing a dielectric layer for the capacitor. It is necessary that the layer 18 have a suitable dielectric constant and be inert when in contact with the semiconductor body 15*a*. Silicon dioxide has been found to be a suitable material for dielectric layer 18 and may be applied by evaporation or thermal oxidation techniques onto body 15*a*. Plate 19 forms the other plate of the capacitor and is provided by evaporating a conductive material onto layer 18. Gold and aluminium have been found to be satisfactory materials for the plate 19. Ohmic contact 17*a* is made to the body of semiconductor material 15*a* and contact to plate 19 may be made by any suitable electrical contact (not shown). Capacitors formed in the manner described in connection with Figure 2*a* have been found to exhibit much more stable characteristics than pure junction capacitors, that is, p—n junction capacitors.

Capacitors produced in the manner of Figure 2 are also diodes, and must therefore be properly polarized in the circuit. Non-polar capacitors may be made by connecting two such areas back-to-back. Although junction capacitors have a marked voltage dependence, such dependence is present to a lesser degree for low voltages in the non-polar configuration.

Resistor and capacitor designs may be combined to form a distributed R—C network. Such is shown in Figure 3, wherein a body comprising a region 20 of p-type conductivity has an n-type conductivity diffused region 21 formed therein. A broad area contact 22 is placed on the diffused region on one face of the body and spaced contacts 23 on the opposite face of the body. These networks are useful for low pass-filters, phase shift networks, coupling elements, etc. Their parameters may be calculated from the equations above. Other configurations of this general type are also possible.

As shown in Figures 4 and 5, transistors and diodes may be formed on or in a single wafer. In Fig. 4, the transistor has a collector region 25, a diffused p—n junction 26, a base layer 27, an emitter contact 28 forming a rectifying connection with base layer 27 and base and collector contacts 29 and 30, respectively. The base layer 27 is formed as a mesa of small cross section. A diode of similar design is shown in Figure 5, and consists of region 35 of one type conductivity, and a mesa region 36 of opposite conductivity-type with a p—n diffused junction formed therebetween and contacts 37 and 48 connected to each region.

Small inductances, suitable for high frequency use, may also be made by shaping the semiconductor as evidenced by Figure 5*a*, which shows a spiral of semiconductor material. It is also possible to prepare photosensitive devices, including photovoltoic cells, photoresistors, and solar cells and other like components utilizing the basic design considerations hereinbefore outlined.

Although all of the circuit elements have been described in terms of a single diffused layer, it is quite possible, where practical, to use a double diffused structure. Thus, double diffusion may be employed to form both n—p—n and p—n—p transistor structures, for example. Moreover, any suitable materials can be used for the semiconductor materials, conductivity producing impurities, and contact materials; and suitable and known processing can be exploited to produce circuit element designs.

Because all of the circuit element designs described above can be formed from a single material, a semiconductor, it is possible by shaping to integrate all of them into a single crystal semiconductor wafer and to process the wafer to provide the proper network and the correct circuit element values.

As will be apparent to one skilled in the art, circuit elements can be classified according to their circuit functions. Thus, circuit elements may be thought of as being either active or passive in nature. Active elements are those which in an impedance network act as current generators; whereas passive elements do not so act, and the term "active element(s)" and "passive element(s)" where used hereinafter and in the claims are to be construed in this sense. Example of active elements are photovoltoic cells and transistors, and examples of passive elements are resistors, capacitors and inductors. Elements which fall into the general category of diodes and are normally employed as passive elements, may if suitably biased and energized, function in an active nature.

A specific illustration of an electronic circuit is shown in Figure 6*a*. As shown, a thin wafer of single crystal semiconductor material contains a p—n junction formed between two monocrystalline layers, which wafer has been processed and shaped to include discrete areas adapted to provide the electrical properties of circuit elements forming a complete and integrated multivibrator electronic circuit closely adjacent one major wafer face. The regions of the wafer have been marked with symbols representative of the circuit element functions that are performed in the various regions. Figure 6*b* shows a wiring diagram of the various circuit functions in the relationship which they occupy in the wafer of Figure 6*a*. A more conventionally drawn circuit diagram is shown in Figure 7 with the circuit values actually used. The multivibrator circuit shown in Figures 6*a*, 6*b* and 7 will be described as illustrative of the processing techniques required. First, a wafer of single crystal semiconductor material, preferably silicon or germanium, of the proper resistivity is lapped and polished on one side. For this design, 3 ohm—cm p-type germanium was used. The wafer was then subjected to an antimony diffusion process which produced a monocrystalline n-type layer on the surface about 0.7 mils deep. The wafer was then cut to the proper size, 0.200 × 080 inches, and the unpolished surface lapped to give a wafer thickness of 0.0025 inches.

Gold plated Kovar (Registered Trade Mark) leads 50 were attached by alloying to the wafer in the proper positions. Kovar is a trade name for an iron-nickel-cobalt alloy. Gold was then evaporated through a mask to provide the areas 51—54 which provide ohmic contact with the n region, such as the transistor base connections and the capacitor contacts. Aluminium was evaporated through a properly shaped mask to provide the transistor emitter areas 56, which form rectifying contacts with the n layer. Alternatively a p-type conductivity producing ingredient may be diffused through a properly shaped mask to provide the transistor emitter areas 56. Suitable ohmic contacts may be secured to the emitter areas in the same manner as the securing of contacts 53 and 54 to base areas of transistors T_2 and T_1. When the emitter area is formed either by diffusion or alloying a monocrystalline layer of conductivity type opposite to that of the base region is provided. The monocrystalline layers of the base and emitter regions are contiguous and form therebetween a p—n junction extending to the major wafer face and there defining an enclosed area of semiconductor material.

In the completed device the p—n junction formed between the collector and base regions also extends to the major wafer face and there defines an enclosed area of semiconductor material surrounding the first mentioned enclosed area.

The wafer was then coated with a photosensitive resist or lacquer, such as Eastman (Registered Trade Mark) Photo Resist, supplied by Eastman Kodak Company, and exposed through a negative to a light. The lacquer image remaining after development was used as a resist for etching the wafer to the proper shape. In particular, this etching forms a slot through the wafer to provide an isolation volume between R_1 and R_2 thereby electrically isolating R_1 and R_2 from each other along at least a major part of their lengths and from the rest of the circuit elements. This etching also shapes all of the resistor areas to the previously calculated configuration. Either chemical etching or electrolytic etching may be used, although electrolytic etching appears to be preferable.

After this step, the photoresist was removed with a solvent, and the areas 60, and such other areas as necessary, were masked by the same photographic process. The wafer was again immersed in etchant, and the n layer completely removed in the exposed areas thereby forming the mesa shapes. A chemical etch is considered preferable. The photoresist was then removed.

Gold wires 70 were then thermally bonded to the appropriate areas to complete the connections, and a final clean up etch given. Instead of using the gold wires 70 in making electrical connections, they may be provided in other ways.

One way, according to this invention, is illustrated in Figs. 9 and 10. Referring now to Fig. 9, there is illustrated the device of Fig. 6*a* including corresponding reference numerals where appropriate to show the comparison. An insulating and inert material such as silicon oxide is evaporated through a mask either to cover the major wafer face completely except at points where electrical contact is to be made, or to cover only selected positions joining the points to be electrically connected. Fig. 9 illustrates the insulation material completely covering the major wafer face except for exposed areas on the contacts 51 and 52 of the capacitors C_2 and C_1, and exposed areas on the base regions 60 and emitter regions 56 of the transistors T_2 and T_1. Electrically conducting material such as gold is then laid down on the insulating material to make the necessary electrical circuit connections which are illustrated by connections 80, 81 and 82 extending from their respective contacts over the insulating material thereby insulating said conductive material from the p—n junctions at the major wafer face. Additionally, gold wires 70 are provided to complete the desired circuit connections.

Fig. 10 illustrating a cross-sectional view of Fig. 9 taken along the line A—A, shows

the wafer, insulating material 85 and the conductive material 80, 81 and 82.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors, and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable, as well as compact.

A further illustration of a semiconductor device which may be modified in accordance with the present invention is shown in Figures 8*a* to 8*c*. Each area of the single crystal semiconductor wafer has been marked with a symbol for the circuit element which it represents. This unit illustrates the use of resistors, transistors, and a distributed R—C network to form a complete phase shift oscillator.

Specifically, Fig. 8*a* shows three resistance-exhibiting areas R_1, R_2 and R_3, these areas being defined by several tabs or contacts which are located on the semiconductor wafer. The resistor R_1 is defined by the contacts marked "−V" and "output", the resistor R_2 by the contact marked "output" and the contact not marked, and the resistance R_3 by the latter contact and that marked "+V". The layer defined just above the resistor R_2 and lying on the semiconductor wafer includes the dielectric layer for the capacitor C_1 and includes a metallic plate positioned thereon, this resulting in a distributed capacitance element. The transistor Q_1 is located in the semiconductor wafer at the junction of the resistors R_1 and R_2 and has its collector electrode internally connected at the junction of R_1 and R_2. The base electrode of the transistor Q_1 is coupled externally to the junction of the resistors R_2 and R_3, the emitter electrode of the transistor Q_1 is coupled to the source of positive voltage by an external connection, and the capacitor plate C_1 is coupled to the source of positive voltage by an external connection. The end result is the network represented schematically in Fig. 8*c*, which is a complete phase shift oscillator circuit.

It must be emphasized that the embodiments described above are merely examples of innumerable networks in a semiconductor body that may be employed with the present invention.

Reference is additionally made to our co-pending patent applications nos. 27542/63; 27196/63; 27195/63; 27326/63; 27197/63; 28004/63; 27198/63; 28005/63; 27540/63; 32744/63; and 27541/63 (Serial Nos. 945,746, 945,740, 945,739, 945,743, 945,741, 945,747, 945,742, 945,748, 945,744, 945,749, 945,745, and 945,734), also divided from application No. 3633/60 (Serial No. 945,734).

Terms indicative of position, such as "on", "overlying" and "underlying", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a body of semiconductor material containing first and second regions of opposite conductivity-types forming therebetween a first P—N junction extending to one surface of said body and there defining a first enclosed area of semiconductor material, said second region underlying said first region, the region immediately underlying said second region being of a conductivity-type opposite to that of said second region to form therewith a second P—N junction extending to said surface and there defining a second enclosed area of semiconductor material surrounding said first enclosed area, first and second contacts secured to said one surface upon opposite sides of said first P—N junction, said first and second contacts being ohmically connected respectively to said first and second enclosed areas, insulation material composed of a silicon oxide on said surface, a first electrical connection to said first contact including conductive material extending from said first contact over said insulation material and being positioned on said insulation material, and a second electrical connection to said second contact including conductive material extending from said second contact over said insulation material and being positioned on said insulation material.

2. A semiconductor device according to claim 1, wherein said first contact is a metal contact secured to said surface within said first enclosed area and spaced from said first P—N junction, said second contact is a generally C-shaped metal contact extending partially around said first contact and being outside of said first enclosed area and spaced from said first P—N junction, said second contact has two ends defining a gap therebetween, said insulation material extending through said gap.

3. A semiconductor device according to claim 2, wherein said first and second regions are emitter and base regions of a transistor and said first and second contacts are emitter and base contacts.

4. A semiconductor device according to claim 1, including a third contact ohmically connected to the region immediately underlying said second region.

5. A semiconductor device according to claim 1, wherein said insulation material extends across said second P—N junction and the conductive material extending from said first and second contacts extends across said second P—N junction.

6. A semiconductor device according to any preceding claim, wherein said body is of ex-

* C L M S *

the wafer, insulating material 85 and the conductive material 80, 81 and 82.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors, and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable, as well as compact.

A further illustration of a semiconductor device which may be modified in accordance with the present invention is shown in Figures 8*a* to 8*c*. Each area of the single crystal semiconductor wafer has been marked with a symbol for the circuit element which it represents. This unit illustrates the use of resistors, transistors, and a distributed R—C network to form a complete phase shift oscillator.

Specifically, Fig. 8*a* shows three resistance-exhibiting areas R_1, R_2 and R_3, these areas being defined by several tabs or contacts which are located on the semiconductor wafer. The resistor R_1 is defined by the contacts marked "−V" and "output", the resistor R_2 by the contact marked "output" and the contact not marked, and the resistance R_3 by the latter contact and that marked "+V". The layer defined just above the resistor R_2 and lying on the semiconductor wafer includes the dielectric layer for the capacitor C_1 and includes a metallic plate positioned thereon, this resulting in a distributed capacitance element. The transistor Q_1 is located in the semiconductor wafer at the junction of the resistors R_1 and R_2 and has its collector electrode internally connected at the junction of R_1 and R_2. The base electrode of the transistor Q_1 is coupled externally to the junction of the resistors R_2 and R_3, the emitter electrode of the transistor Q_1 is coupled to the source of positive voltage by an external connection, and the capacitor plate C_1 is coupled to the source of positive voltage by an external connection. The end result is the network represented schematically in Fig. 8*c*, which is a complete phase shift oscillator circuit.

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2. A semiconductor device according to claim 1, wherein said first contact is a metal contact secured to said surface within said first enclosed area and spaced from said first P—N junction, said second contact is a generally C-shaped metal contact extending partially around said first contact and being outside of said first enclosed area and spaced from said first P—N junction, said second contact has two ends defining a gap therebetween, said insulation material extending through said gap.

3. A semiconductor device according to claim 2, wherein said first and second regions are emitter and base regions of a transistor and said first and second contacts are emitter and base contacts.

4. A semiconductor device according to claim 1, including a third contact ohmically connected to the region immediately underlying said second region.

5. A semiconductor device according to claim 1, wherein said insulation material extends across said second P—N junction and the conductive material extending from said first and second contacts extends across said second P—N junction.

6. A semiconductor device according to any preceding claim, wherein said body is of ex-

trinsic semiconductor material throughout.

7. A semiconductor device according to any preceding claim, where said insulation material extends across substantially the entire portion of said second P—N junction which extends to said one surface.

8. A semiconductor device according to any preceding claim, wherein said body is silicon.

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ERRATA

SPECIFICATION No. 945,738
Amendment No. 1

Page 2, line 76, *for* "suitable" *read* "available"
Page 3, line 85, *for* "photovoltoice" *read* "photovoltaic"
Page 3, lines 118 and 119, *for* "photovoltoice" *read* "photovoltaic"

THE PATENT OFFICE
19th May 1965

PATENTS ACT, 1949

SPECIFICATION NO. 945,738

In accordance with the Decision of the Superintending Examiner, acting for the Comptroller-General, dated the 17th day of August, 1965 this Specification has been amended under Section 29 in the following manner:-

Page 1, in the title, *delete* "and methods of producing same"

THE PATENT OFFICE,
6th October, 1965

D 44722/6