SPACER PROCESS FOR ON PITCH CONTACTS AND RELATED STRUCTURES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention relate to semiconductor processing and, more particularly, to masking techniques.

Description of the Related Art

[0002] There is a constant demand to decrease the sizes of integrated circuits. This decrease can be facilitated by reducing the sizes and separation distances between the individual elements or electronic devices forming the integrated circuits. This process of reducing the sizes of features and the separation distances between features can increase the density of circuit elements across a substrate and is typically referred to as "scaling." As a result of the continuing demand for smaller integrated circuits, there is a constant need for methods and structures for scaling.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The appended drawings are schematic, not necessarily drawn to scale, and are meant to illustrate and not to limit embodiments of the invention.

[0004] Figure 1 is a flow chart illustrating a process in accordance with embodiments of the invention.

[0005] Figure 2 illustrates a cross-sectional side view of a partially formed integrated circuit having a stack of masking layers overlying a substrate in accordance with embodiments of the invention.

[0006] Figure 3A illustrates a top view of a partially formed integrated circuit, having a pattern of mandrels in accordance with embodiments of the invention.

[0007] Figure 3B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 3A along the sectional line 3B shown in Figure 3A in accordance with embodiments of the invention.

[0008] Figure 4A illustrates a top view of the partially formed integrated circuit of Figure 3A after the pattern of mandrels has been trimmed in accordance with embodiments of the invention.

[0009] Figure 4B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 4A along the sectional line 4B shown in Figure 4A in accordance with embodiments of the invention.

[0010] Figure 5A illustrates a top view of the partially formed integrated circuit of Figure 4A during deposition of a spacer material on pillars in accordance with embodiments of the invention.

[0011] Figure 5B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 5A along the sectional line 5B shown in Figure 5A in accordance with embodiments of the invention.

[0012] Figure 6A illustrates a top view of the partially formed integrated circuit of Figure 5A after etching the spacer material in accordance with embodiments of the invention.

[0013] Figure 6B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 6A along the sectional line 6B shown in Figure 6A in accordance with embodiments of the invention.

[0014] Figure 7A illustrates a top view of the partially formed integrated circuit of Figure 6A after etching mandrels in accordance with embodiments of the invention.

[0015] Figure 7B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 7A along the sectional line 7B shown in Figure 7A in accordance with embodiments of the invention.

[0016] Figure 8A illustrates a top view of the partially formed integrated circuit of Figure 8A after forming a secondary mask in accordance with embodiments of the invention.

[0017] Figure 8B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 8A along the sectional line 8B shown in Figure 8A in accordance with embodiments of the invention.

[0018] Figure 9 illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 8A after a pattern transfer to an underlying layer in accordance with embodiments of the invention.

[0019] Figure 10 illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 9 after another pattern transfer to a primary masking layer in accordance with embodiments of the invention.

[0020] Figure 11 illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 10 after a pattern transfer to the substrate in accordance with embodiments of the invention.

[0021] Figure 12 illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 11 after removing masking layers overlying the substrate in accordance with embodiments of the invention.

[0022] Figure 13 is a flow chart illustrating processes in accordance with other embodiments of the invention.

[0023] Figure 14A illustrates a top view of a partially formed integrated circuit after forming a pattern of mandrels in accordance with embodiments of the invention.

[0024] Figure 14B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 14A along the sectional line 14B shown in Figure 14A in accordance with embodiments of the invention.

[0025] Figure 15A illustrates a top view of the partially formed integrated circuit of Figure 15A after the pattern of mandrels has been trimmed in accordance with embodiments of the invention.

[0026] Figure 15B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 15A along the sectional line 15B shown in Figure 15A in accordance with embodiments of the invention.

[0027] Figure 16A illustrates a top view of the partially formed integrated circuit of Figure 15A after deposition of a spacer material on pillars in accordance with embodiments of the invention.

[0028] Figure 16B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 16A along the sectional line 16B shown in Figure 16A in accordance with embodiments of the invention.

[0029] Figure 17A illustrates a top view of the partially formed integrated circuit of Figure 16A after etching the spacer material in accordance with embodiments of the invention.

[0030] Figure 17B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 17A along the sectional line 17B shown in Figure 17A in accordance with embodiments of the invention.

[0031] Figure 18A illustrates a top view of the partially formed integrated circuit of Figure 17A after etching the pillars to leave a pattern defined by the spacer material in accordance with embodiments of the invention.

[0032] Figure 18B illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 18A along the sectional line 18B shown in Figure 18A in accordance with embodiments of the invention.

[0033] Figure 19 illustrates a cross-sectional side view of the partially formed integrated circuit of Figure 18A after transferring the pattern defined by the spacer material to the substrate in accordance with embodiments of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0034] Embodiments of the invention provide methods of forming patterns of isolated features, such as holes or isolated pillars, having a high density. Advantageously, the holes or isolated pillars can be used to form conductive contacts to various features in integrated circuits. For example, contacts can be made to conductive interconnects having a close spacing, or small pitch, *e.g.*, a pitch of about 60 nm or less, or about 30 nm or less. It will be appreciated that pitch is defined as the distance between an identical point in two neighboring interconnects, which are typically spaced apart by a material, such as an insulator. As a result, pitch may be viewed as the sum of the width of a feature and of the width of the space on one side of the feature separating that feature from a neighboring feature.

[0035] It will also be appreciated that interconnects with a small pitch present difficulties for forming contacts. Interconnects with small pitches can be formed by pitch multiplication, such as described in U.S. Patent No. 7,253,118, issued August 7, 2007, entitled PITCH REDUCED PATTERNS RELATIVE TO PHOTOLITHOGRAPHY FEATURES, the entire disclosure of which is incorporated by reference herein. Because of the close spacing between interconnects with small pitches, relatively large contacts can cause shorts between neighboring interconnects. Moreover, the relatively large cross-sectional areas of some contacts make difficult the formation of "on pitch" contacts, that is, contacts with the same pitch as the interconnects. Instead, contacts are typically formed staggered, with odd numbered contacts forming one row and even numbered contacts forming another row of contacts. These staggered contacts use space inefficiently due to their staggered nature and, as a result, present an obstacle to further integrated circuit miniaturization and scaling.

[0036] Advantageously, one or more embodiments of the invention allow the formation of contacts that are on pitch. The on pitch contacts advantageously are aligned in a row, allowing for a more efficient use of space. Moreover, the advantageously small sizes of the contacts decrease the occurrence of electrical shorts between neighboring interconnects and neighboring contacts.

[0037] The contacts can be patterned using a mask defined or derived from spacers. In some embodiments of the invention, a method is provided for increasing the density of patterned features by a multiple of about 1.5 or more. A row of sacrificial mandrels is formed having a linear density Z. The mandrels can be, *e.g.*, free-standing spacers formed in, *e.g.*, a photoresist layer. Additional mask features are defined between the mandrels by forming spacers at sides of the mandrels. The spacers can be formed by blanket depositing spacer material over the mandrels and then etching the spacer material, thereby forming the spacers at the sides of the mandrels. The mandrels are removed, thereby forming a mask pattern using the spacers, the mask pattern having a density of holes of about 1.5Z or more. The contacts are advantageously transferred to a substrate, to, *e.g.*, define conductive contacts to electrical features such as interconnects. It will be appreciated that the substrate

can form various electronic devices, including integrated circuits such as memory devices, including nonvolatile memory such as flash memory.

[0038] Reference will now be made to the Figures, in which like numerals refer to like parts throughout.

[0039] Figure 1 illustrates a general sequence of process steps according to some embodiments of the invention. In step 1 of Figure 1, a substrate is provided. The substrate can comprise a plurality of different materials, including insulating, semiconducting and conducting materials, which can be etched through an overlying mask. A masking stack comprising a first selectively definable layer is provided overlying the substrate.

[0040] With continued reference to Figure 1, in step 3, a pattern is formed in the first selectively definable layer. In some embodiments, a plurality of mandrels, such as pillars, are in a row in the first selectively definable layer. The mandrels can be formed by photolithography, by selectively exposing photoresist to light and then developing the photoresist to leave a pattern of pillars composed of the photoresist. As used herein, "forming" a structure includes performing steps to make the structure or providing the structure already premade. In step 5, the features defining the pattern in the first selectively definable layer are optionally trimmed to a desired size. In step 7, spacer material is formed on and around the mandrels while leaving a pattern of openings between the mandrels. In step 9, the spacer material is etched to form a pattern of holes completely open to an underlying material. In step 11, the mandrels and, optionally, the entirety of the first selectively definable layer, are removed to form further holes, thus providing a pattern of holes with a density greater than the mandrels originally formed in the first selectively definable layer.

[0041] In step 13, a second selectively definable layer is provided. The second selectively definable layer can be formed over the spacers and then patterned. It will be appreciated that forming contacts typically entails forming a row of contact features. As a result, in some embodiments, only a row of holes formed by the spacers is transferred to an underlying substrate. The second selectively definable layer is used to block pattern transfer of particular parts of the spacer pattern. For example, the second selectively definable layer

can be patterned such that only a single row of holes defined be spacers is exposed for pattern transfer to underlying materials.

[0042] With continued reference to Figure 1, in step 15, the pattern formed by the combination of the spacer material and the second selectively definable layer is transferred to an underlying material. It will be appreciated that the underlying material may be the substrate, or, in some embodiments, may be additional masking layers. If additional masking layers are present, the pattern may be transferred to the underlying substrate after transfer to the additional masking layers.

[0043] The sequence of Figure 1 will now be described in greater detail with reference to cross-sectional and top plan views, in accordance with some embodiments of the invention. With reference to Figures 1 and 2, in step 1, a substrate 100 is provided and a masking stack, including layers 120-130 is provided thereover. The substrate 100 and the masking stack form a partially formed integrated circuit 200. The substrate 100 may include one or more of a variety of suitable workpieces for semiconductor processing. For example, the substrate 100 can include a silicon wafer. As illustrated, the substrate 100 can include various layers of materials, including the layers 100a and 100b. Layer 100a can be a dielectric, in which contacts can be formed. The layer 100b can include a single material, or can include various other materials and features, such as pitch-multiplied interconnects, to which contacts in the layer 100a can electrically contact.

[0044] In one or more embodiments, the first hard mask layer 120, also referred to as the primary mask layer, is formed of amorphous carbon, *e.g.*, transparent carbon, which has been found to have excellent etch selectivity with other materials of the illustrated imaging or masking stack. Methods for forming amorphous carbon are disclosed in A. Helmbold, D. Meissner, Thin Solid Films, 283 (1996) 196-203, the entire disclosures of which are hereby incorporated herein by reference. In the illustrated embodiment, a second hard mask layer 122 is also formed over the first hard mask layer 120 to protect the first hard mask layer 120 during etching in later steps and/or to enhance the accuracy of forming patterns by photolithography. In one or more embodiments, the second hard mask layer 122 includes an anti-reflective coating (ARC), such as DARC or BARC/DARC, which can aid photolithography by preventing undesired light reflections.

[0045] With continued reference to Figure 2, a selectively definable layer 130 is formed on the second hard mask layer 122. The selectively definable layer 130 can be formed using a photoresist in accordance with well-known processes for providing masks in semiconductor fabrication. For example, the photoresist can be any photoresist compatible with 157 nm, 193 nm, 248 nm or 365 nm wavelength systems, 193 nm wavelength immersion systems, extreme ultraviolet systems (including 13.7 nm wavelength systems) or electron beam lithographic systems. In addition, maskless lithography, or maskless photolithography, can be used to define the selectively definable layer 120. Examples of preferred photoresist materials include argon fluoride (ArF) sensitive photoresist, *i.e.*, photoresist suitable for use with an ArF light source, and krypton fluoride (KrF) sensitive photoresist, *i.e.*, photoresist suitable for use with a KrF light source. ArF photoresists are preferably used with photolithography systems utilizing relatively short wavelength light, *e.g.*, 193 nm. KrF photoresists are preferably used with longer wavelength photolithography systems, such as 248 nm systems. In other embodiments, the selectively definable layer 130 and any subsequent resist layers can be formed of a resist that can be patterned by nano-imprint lithography, *e.g.*, by using a mold or mechanical force to pattern the resist.

[0046] With reference to Figures 3A and 3B, a partially formed integrated circuit 200 is illustrated after step 3 (Figure 1) has been carried out. As shown in Figures 3A and 3B, the selectively definable layer 130 is patterned to expose parts of the second hard mask layer 122. The pattern in the selectively definable layer 130 includes a plurality of mandrels 131, first and second blocks 132, 133 on either side of the mandrels 131, and sacrificial features 134 in contact with and extending from the first and second blocks 132, 133 to the mandrels 131. Thus, as illustrated, the mandrels 131 and features 134 are aligned in rows and form a checkerboard pattern between the first and second blocks 132, 133. The features 134 in contact with the first block 132 may be considered to form a first row of the checkerboard pattern, the features 134 in contact with the second block 133 may be considered to form a second row, and the mandrels 131 may be considered to form a third row of the checkerboard pattern.

[0047] The selectively definable layer 130 can be patterned using photolithography. Due to limitations of typical optical systems, it will be appreciated that

conventional photolithographic methods can have difficulties forming free-standing mandrels 131 in isolation. Advantageously, in some embodiments, the first and second blocks 132, 133 and the features 134 can be used to facilitate formation of the mandrels 131.

[0048] In some embodiments, the sizes of the mandrels 131 are substantially equal to the minimum feature size formable using the lithographic technique used to pattern the layer 130. In some other embodiments, the mandrels 131 can be formed larger than the minimum feature size formed by photolithography, in order to enhance the accuracy of the patterns formed by photolithography. It will be appreciated that photolithographic techniques typically can more easily and accurately form features having sizes above the size limit of the technique.

[0049] Where the sizes and/or shapes of the mandrels 131 are larger or different from that desired, the mandrels 131 are optionally trimmed. The trim reduces the sizes of the mandrels, in addition to rounding the corners of the mandrels. Figures 4A and 4B illustrate the partially formed integrated circuit 200 after step 5 of Figure 1 has been carried out. In step 5, the selectively definable layer 130 is trimmed, such as by subjecting the selectively definable layer 130 to O_2/Cl_2 or O_2/HBr plasma, to form trimmed mandrels 131a. It will be appreciated that the trim also trims the features 134 to form trimmed features 134a and also trims the blocks 132, 133 to form trimmed blocks 132a, 133a. Thus, the trimming step 5 can advantageously provide a feature size that is less than the minimum feature size formable using the lithographic technique used to pattern the selectively definable layer 130. In some embodiments, the mandrels 131 are trimmed to a size substantially equal to the size of the holes 150 (Figures 6A and 6B) that will later be formed. In the illustrated embodiments, the trim leaves the mandrels 131a with a circular cross-sectional shape, as seen from the top down view in Figure 4A. Advantageously, in some embodiments, the mandrels 131a have a width of about 60 nm or less, or about 30 nm or less, and are spaced by about 60 nm or less, or about 30 nm or less.

[0050] With reference to Figures 5A and 5B, in step 7 of Figure 1, a layer 140 of spacer material is blanket deposited on the mandrels 131a, sacrificial features 134a, and first and second blocks 132a, 133a. The spacer material is selectively etchable with respect to the material of the mandrels 131a and other exposed surfaces. In some embodiments, the spacer

material is an oxide such as silicon oxide. Examples of other spacer materials include silicon nitride, Al_2O_3, TiN, etc. In one or more embodiments, deposition of the spacer material is accomplished by chemical vapor deposition. In other embodiments, particularly where selectively definable layer 130 is formed of photoresist or other material sensitive to high temperature, the spacer material layer 140 is deposited by atomic layer deposition, which can be performed at relatively low temperatures. It will be appreciated that photoresist can be damaged or deformed by exposure to high temperatures and atomic layer deposition can be performed at temperatures compatible with photoresist.

[0051] In some embodiments, the pattern in the selectively definable layer 130 can be transferred to one or more underlying layers before depositing the layer 140 of spacer material. For example, in embodiments where exposure and resistance to high temperatures is desired (*e.g.*, where the material for the layer 140 requires a high temperature deposition), the pattern in the selectively definable layer 130 can be transferred to a more high temperature resistant material before deposition of the layer 140. For example, the pattern can be transferred to an additional underlying layer of sufficiently temperature resistant material.

[0052] With continued reference to Figures 5A and 5B, it will be appreciated that the layer 140 is preferably conformal and assumes the general contours of the underlying topology. Thus, indentations 147 are formed between mandrels 131a.

[0053] In step 9 of Figure 1, the layer 140 of spacer material is etched, preferably anisotropically etched, to expose the upper surfaces of the mandrels 131a and the second hard mask layer 122, as shown in Figures 6A and 6B. Thus, spacers 145 are formed at the sides of mandrels 131a. The spacers 145 define holes 150, which expose the second hard mask layer 122.

[0054] In step 11 of Figure 1, the mandrels 131a are removed by selectively etching the selectively definable layer 130 (Figure 6A and 6B) relative to the spacers 145 as shown in Figures 7A and 7B. Thus, holes 152 are formed at the locations formerly occupied by the mandrels 131a. At this stage, a pattern of holes 150, 152 have been formed. It will be appreciated that the mandrels 131a, formed in a row, had a linear density of Z. The spacers 145 define holes 150 between themselves. Thus, for every two mandrels 131a, a hole 150 is

formed. As a result, the linear density of the holes is preferably at least 1.5Z. It will be appreciated that the multiplier 1.5 increases as the number of mandrels 131a increase. For example, six mandrels 131a will result in at least five holes 150, such that the multiplier approaches or is about two as the Z increases.

[0055] In step 13 of Figure 1, a second selectively definable layer 160 is formed over and around the spacers 145. The second selectively definable layer 160 is then patterned, as shown in Figures 8A and 8B. In some embodiments, the second selectively definable layer 160 is formed of photoresist. The second selectively definable layer can be formed of the same types of materials as the first selectively definable layer 130, including the same photoresist. In other embodiments, a material different from that of the layer 130 may be used.

[0056] In some embodiments, only a single row of holes 150, 152 is desired to form on pitch contacts. As a result, the second selectively definable layer 160 is patterned to allow transfer of only the row of holes 150, 152 to underlying layers. As illustrated, the patterned layer 160 leaves the row of holes 150, 152 exposed for pattern transfer.

[0057] In step 15, the pattern defined by the spacers 145 and the second selectively definable layer 160 is transferred to underlying materials, *e.g.*, using anisotropic etches selective for the material forming an underling layer relative to other exposed materials. With reference to Figure 9, the pattern is transferred to the second hard mask layer 122.

[0058] With reference to Figure 10, the pattern is then transferred to the first, or primary, hard mask layer 120. As noted above, the primary hard mask layer 120 is preferably formed of amorphous carbon, which has particular advantages in offering high etch selectivity relative to various silicon-containing materials, such as those of the partially formed integrated circuit 200. The primary masking layer 120 provides a robust mask for etching the underlying substrate 100.

[0059] With reference to Figure 11, the pattern originally defined by the spacers 145 and the second selectively definable layer 160 is transferred to layer 100a in the substrate 100. Depending upon the etch used and the identity of materials, the anisotropic etch used in some embodiments of the pattern transfer may remove some of the overlying materials, such

as the spacers 145 and/or the second hard mask layer 122. In some embodiments, the layer 100a is formed of a dielectric, *e.g.*, silicon oxide and transferring the holes 150, 152 to that layer 100a forms contacts vias. The holes 150, 152 expose conductive interconnects in some embodiments. The holes 150, 152 may be filled with conducting or semiconducting material to form contacts to the conductive interconnects (not shown).

[0060] Optionally, before the pattern transfer to the layer 100a, the mask formed by the primary hard mask layer 120 is cleaned. It will be appreciated that the etch used to transfer the pattern of holes 150, 152 to the primary hard mask layer 120 can cause undesired residue or polymerization. A wet organic strip etch can be used to clean the mask formed by the layer 120 by removing the residue or polymerization product before the pattern transfer to the underlying layer 100a.

[0061] It will be appreciated that wet organic strip etches may advantageously be applied to remove various exposed materials, such as carbon-based materials. As discussed herein, these organic strip etches include solvent based chemistries. In other embodiments, the strip etches or cleaning steps may include acidic or basic chemistries, as appropriate for the particular materials present and desired for removal, as known in the art.

[0062] With reference to Figure 12, the overlying masking stack is removed. For example, in embodiments where the primary masking layer 120 is formed of amorphous carbon, the amorphous carbon can be stripped using a wet organic strip etch. Thus, a pattern of openings 110 are formed in the layer 110a. In some embodiments, material is subsequently deposited into the openings 110 to form, *e.g.*, conductive contacts.

[0063] Figure 13 and the ensuing figures illustrate another sequence of process steps according to some other embodiments of the invention. It will be appreciated that the materials, etches and other details of the steps discussed above have application to this sequence.

[0064] In step 21 of Figure 13, a substrate with an overlying masking stack is provided. The substrate is similar to that described above with reference to Figure 2. In the illustrated embodiment, the substrate 100 includes a plurality of layers 100a, 100b of different materials, including a dielectric layer 100a. The overlying masking stack includes a plurality of layers to facilitate spacer formation and pattern transfer to the substrate 100. As

illustrated, the masking stack includes a first, or primary, hard mask layer 120, a second hard mask layer 122 and a selectively definable layer 130.

[0065] In step 23 (Figure 13), a pattern is formed in the first selectively definable layer, as illustrated in Figures 14A and 14B. A plurality of mandrels 131b is formed in a row in the first selectively definable layer 130 to expose parts of the second hard mask layer 122. In some embodiments, the mandrels 131b are formed by photolithography. The mandrels 131b can include end sections 131c, which are in contact with the first and second blocks 132, 133. The mid-sections of the mandrels 131b are wider than the end sections 131c, to facilitate photolithographic patterning of mandrels 131b which allow the formation of rounded mask holes 200 (Figure 17A). Advantageously, formation of only a single row of features 131b allows formation of a row of on pitch contacts without use of a second selectively definable layer, such as the layer 160 (Figure 8A), to block the transfer of neighboring mask features to underlying materials.

[0066] In step 25 (Figure 13), the pattern formed in the first selectively definable layer is optionally trimmed, as illustrated in Figures 15A and 15B. As noted above, the trim is advantageously applied where the sizes and/or shapes of the mandrels 131b are larger or different from that desired, since the trim reduces the sizes of the mandrels 131b, in addition to rounding the corners of the mandrels. The trim removes the end sections 131c, leaving trimmed mandrels 131d and trimmed first and second blocks 132d, 133d. The trim leaves the mandrels 131d with an oval cross-sectional shape, as seen from the top down view in Figure 15A.

[0067] With reference to Figures 16A and 16B, in step 27 of Figure 13, spacer material layer 140 is blanket deposited on the mandrels 131d and on the first and second blocks 132d, 133d. In some other embodiments, the pattern in the selectively definable layer 130 can be transferred to one or more underlying layers before depositing the layer 140 of spacer material.

[0068] In the illustrated embodiment, with continued reference to Figures 16A and 16B, the layer 140 is conformal and assumes the general contours of the underlying topology, thereby forming indentations 201 between mandrels 131a.

[0069] In step 29 of Figure 13, the layer 140 of spacer material is etched, preferably anisotropically etched. The upper surfaces of the mandrels 131d and the second hard mask layer 122 are exposed, as shown in Figures 17A and 17B. Spacers 146 are formed at the sides of mandrels 131d. The spacers 146 define holes 202.

[0070] In step 31 of Figure 13, the mandrels 131d are removed by a selective etch. With reference to Figures 18A and 18B, the selective etch preferentially removes the selectively definable layer 130 (Figure 17A and 17B) relative to the spacers 146. As a result, holes 204 are formed at the locations formerly occupied by the mandrels 131d. It will be appreciated that, taking the linear density of the mandrels 131d as Z, the linear density of the holes is at least 1.5Z.

[0071] In step 33 of Figure 13, the pattern defined by the spacers 146 is transferred to underlying materials. With reference to Figure 18B, the pattern is transferred successively to underlying second hard mask layer 122, primary hard mask layer 120 and dielectric layer 100a. The transfer can be accomplished as described above with respect to step 15 of Figure 1. In some embodiments, a wet organic strip etch may be used to clean the mask before transfer to the substrate 100, as discussed herein.

[0072] With reference to Figure 19, the overlying masking stack is removed. Where the primary masking layer 120 is formed of amorphous carbon, the amorphous carbon can be stripped using, *e.g.*, a wet organic strip etch. Thus, a pattern of openings 112 are formed in the layer 110a. In some embodiments, the openings 112 are contact vias, which may be filled to form conductive contacts to underlying electrical features.

[0073] Thus, it will be appreciated that, in accordance with the embodiments described above, a method for semiconductor processing is provided. The method comprises providing a row of laterally separated mandrels formed of a mandrel material. The row extends along a first axis. First and second laterally spaced blocks of mandrel material are provided on a same plane as the mandrels. The first and second blocks extend a length of the row, and the mandrels are disposed between the first and second blocks. A layer of spacer material is blanket deposited over the mandrels. The layer of spacer material is anisotropically etched to form spacers on sides of the mandrels. The mandrels are selectively

removed relative to the spacer material and the remaining spacer material forms a mask pattern. The mask pattern to the substrate to forms a row of contact vias in the substrate.

[0074] In other embodiments, a method for integrated circuit fabrication is provided. The method comprises providing a row of pillars on a level above a substrate. The pillars have a linear density Z. The row of pillars is replaced with a mask having a row of holes. The mask and holes are disposed on the same level as the pillars. The holes have a width of about 60 nm or less. At least some of the holes are disposed at a location formerly occupied by a pillar. The holes having a linear density at least about 1.5 times Z.

[0075] In other embodiments, a partially fabricated integrated circuit is provided. The partially fabricated integrated circuit comprises a plurality of pillars extending on a first axis. First and second laterally spaced blocks formed of the same material as the pillars are provided extending at least between a first and a last of the pillars on the first axis. The pillars are disposed between the first and second blocks. Spacers are disposed on sides of the pillars and on sides of the first and the second blocks.

[0076] It will be appreciated by those skilled in the art that various omissions, additions, and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such changes are intended to fall within the scope of the invention, as defined by the appended claims.

WE CLAIM:

1. A method for semiconductor processing, comprising:

providing a row of laterally separated mandrels formed of a mandrel material, the row extending along a first axis;

providing first and second laterally spaced blocks of mandrel material on a same plane as the mandrels, the first and second blocks extending a length of the row, wherein the mandrels are disposed between the first and second blocks;

blanket depositing a layer of spacer material over the mandrels;

anisotropically etching the layer of spacer material to form spacers on sides of the mandrels;

selectively removing the mandrels relative to the spacer material, wherein remaining spacer material forms a mask pattern; and

transferring the mask pattern to the substrate to form a row of contact vias in the substrate.

2. The method of Claim 1, wherein the mandrel material is photoresist, wherein providing the row of laterally separated mandrels and providing first and second laterally spaced blocks of mandrel material comprises photolithographically defining the row of laterally separated mandrels and the first and second laterally spaced blocks.

3. The method of Claim 1, wherein transferring the mask pattern to the substrate comprises:

transferring the mask pattern to a primary masking layer; and

etching the substrate through the primary masking layer to etch the mask pattern into the substrate.

4. The method of Claim 3, wherein transferring the mask pattern to the substrate comprises transferring the mask pattern to an anti-reflective coating before transferring the mask pattern to the primary masking layer.

5. The method of Claim 3, wherein the primary masking layer comprises amorphous carbon.

6. The method of Claim 3, further comprising performing a carbon strip after transferring the mask pattern to the primary masking layer and before etching the substrate.

7. The method of Claim 3, further comprising selectively removing the primary masking layer after etching the substrate.

8. The method of Claim 1, wherein the first and second blocks extend along a second axis substantially transverse to the first axis.

9. The method of Claim 1, wherein the mandrels contact the first and second blocks.

10. The method of Claim 9, wherein the mandrels are provided with a mid-section wider than ends of the mandrels in contact with the first and second blocks.

11. The method of Claim 1, wherein the mandrels form a checkerboard pattern with sacrificial features in contact with the first and second blocks.

12. The method of Claim 11, wherein mandrels and the sacrificial features are arranged in three substantially parallel rows, wherein a first row of sacrificial features contacts the first block, a second row of sacrificial features contacts the second block and the mandrels form the third row.

13. The method of Claim 1, wherein the mandrels have an oval cross-sectional shape, as observed from a top down view.

14. The method of Claim 1, wherein transferring the mask pattern to the substrate exposes conductive interconnects in the substrate.

15. A method for integrated circuit fabrication, comprising:

providing a row of pillars on a level above a substrate, the pillars having a linear density Z; and

replacing the row of pillars with a mask having a row of holes, the mask and holes disposed on the level, the holes having a width of about 60 nm or less, at least some of the holes disposed at a location formerly occupied by a pillar, the holes having a linear density at least about 1.5 times Z.

16. The method of Claim 15, wherein the linear density of the holes is about 2 times Z.

17. The method of Claim 15, wherein the pillars are formed of photoresist, wherein providing the row of pillars comprises:

photolithographically forming features in the photoresist; and

trimming the photoresist features to form the pillars.

18. The method of Claim 15, wherein replacing the row of pillars with the mask having the row of holes comprises:

depositing spacer material on the pillars;

etching the spacer material to form spacers on sides of the pillars; and

selectively removing the pillars.

19. A partially fabricated integrated circuit, comprising:

a plurality of pillars extending on a first axis;

first and second laterally spaced blocks formed of the same material as the pillars, the first and second blocks extending at least between a first and a last of the pillars on the first axis, wherein the pillars are disposed between the first and second blocks; and

spacers disposed on sides of the pillars and on sides of the first and the second blocks.

20. The partially fabricated integrated circuit of Claim 19, wherein only one row of pillars is disposed between the first and second blocks.

21. The partially fabricated integrated circuit of Claim 19, wherein the pillars comprise photoresist.

22. The partially fabricated integrated circuit of Claim 21, wherein the width is about 30 nm or less.

23. The partially fabricated integrated circuit of Claim 21, wherein a distance between the spacers at the sides of the pillars is about 50 nm or less.

24. The partially fabricated integrated circuit of Claim 19, further comprising a plurality of conductive interconnects below the spacers and the pillars, the pillars vertically aligned with at least some of the conductive interconnects.

25. The partially fabricated integrated circuit of Claim 19, wherein the partially fabricated integrated circuit is a partially fabricated memory device.