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(54) PULSE GENERATOR FOR TELEVISION FOR GENERATING AT LEAST ONE PULSE SERIES HAVING PULSES OF DIFFERENT DURATION AND REPETITION PERIOD

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 The invention relates to a method of generating a television synchronising and/or blanking pulse signal for a television standard which signal has at least one repeating pulse series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values. The invention also relates to a television synchronising and/or blanking pulse generator for generating such a signal.

15 It has already been proposed to derive such a signal from a series of clock pulses whose frequency is higher than that of the line frequency for the television standard. An object of the invention is to provide such a method and a television pulse generator in which the clock pulse frequency has a specific relationship to the line frequency which greatly assists in the production of the various pulses and spacings in the signal.

20 The invention provides a method of generating a synchronising and/or blanking pulse signal for a television standard which signal has at least one repeating pulse series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, the method comprising generating a clock pulse train whose period is such that each of said different duration and different values is substantially an integral multiple of the clock pulse period, the frequency of the clock pulse train being substantially equal to or an integral multiple of eighty times the line frequency for the

television standard, dividing the clock pulse train to produce therefrom frequency divided clock pulse trains, producing generated pulse trains from the divided clock pulse trains, and combining the divided clock pulse trains and the generated pulse trains in such manner as to produce the synchronising and/or blanking pulse signal.

50 The invention also provides a television synchronising and/or blanking pulse generator for generating for a television standard at least one repeating pulse series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, the television pulse generator comprising a clock pulse generator having a period such that each of said different durations and different values is substantially an integral multiple of the clock pulse period, the clock pulse generator having a frequency which is substantially equal to or an integral multiple of eighty times the line frequency for the television standard, a circuit of frequency dividers connected to the clock pulse generator, pulse generators controlled by the dividers, and a signal generator controlled by the dividers and the pulse generators, the signal generator being provided with an output which forms an output of the television pulse generator and from which may be derived the repeating pulse series.

55 The television pulse generator may be provided with a second signal generator which is also controlled by the circuit of frequency dividers and pulse generators, the first mentioned and second signal generators generating respectively said one and a second differing repeating pulse series which are related in time.

60 The circuit of frequency dividers may divide the clock pulses to produce pulses of line frequency, which circuit is also connected to said one or to both of the signal generators to determine the precise timing of

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at least some of the pulse edges in the synchronising and/or blanking signal.

With a television pulse generator for use with different television standards each having specified line and field frequencies, the circuit of frequency dividers may have a first circuit which divides by a constant divisor to produce pulses of line frequency and a second circuit which divides to produce pulses of field frequency, the second circuit being switchable in divisor to produce pulses of field frequency appropriate to the television standard. The first circuit may be switchable between different circuit configurations so as to obtain a displacement of the precisely timed pulse edges controlled thereby for the different television standards. The divisor of the first circuit may be made to be larger than the ratio between the clock pulse generator frequency and the line frequency save for the first circuit being provided with switchable feedback paths to obtain the correct ratio and the said pulse edge displacement. The second circuit which produces pulses of field frequency may include a divider stage having a nominal divisor set by the internal connections of the divider stage, an output of one of the pulse generators controlled by the circuit of frequency dividers being connected to a blocking input of the divider stage to increase the nominal divisor of the divider stage.

The circuit of frequency dividers may divide to produce pulses of line frequency and of field frequency, the pulses of line and field frequency being applied to an auxiliary pulse generator for producing auxiliary pulses at line frequency and twice line frequency, which auxiliary generator is connected to the signal generator or signal generators for control purposes and to determine the occurrence of at least some of the pulse edges in the synchronising and/or blanking signals. The auxiliary pulse generator may be directly connected to the circuit of frequency dividers, and may be additionally connected to the circuit of frequency dividers through one of the pulse generators, which pulse generator produces a pulse at field frequency having a period equal to the equalising and field synchronising periods. The signal generator may comprise a J.K flip-flop having a set input S_1 and a reset input S_2 which inputs are connected to outputs conveying inverted signals of the auxiliary pulse generator providing auxiliary pulses at line frequency and at double line frequency, the auxiliary pulse generator comprising a delay times between its inputs and outputs.

The circuit of frequency dividers may divide to produce pulses at field frequency and may be provided with an input for receiving synchronising signals at field frequency, the clock pulse generator being connected to a phase discriminator which phase discriminator has an input for receiving line frequency syn-

chronising signals for controlling the frequency of the clock pulse generator. The field frequency synchronising input of the circuit of frequency dividers may be coupled to a synchronising circuit is additionally coupled to a further pulse generator whose output conveys pulses at field frequency, the output of the further pulse generator forming a supply for the synchronising circuit.

The television pulse generator when for use with the PAL colour television standard may be provided with a PAL chrominance sub-carrier gating signal generator to which are applied pulses at line frequency from the circuit of frequency dividers and pulses from the clock pulse generator to determine the timing of pulse edges in the gating signal, the gating signal generator incorporating a blocking signal generator for providing a blocking pulse of nine line periods duration occurring at field frequency the blocking pulse being shifted over cycles of four field periods to accommodate quarter line offset, the blocking signal generator receiving pulses at field frequency from one of the pulse generators connected to the circuit of frequency dividers and pulses of a higher frequency from the circuit of frequency dividers, the subcarrier gating signal generator also receiving pulses at half line frequency. The gating signal generator may comprise first and second J.K flip-flop each having a command input T and a reset input S_2 , the command input T of the second flip-flop being coupled to the clock pulse generator whilst that of the first flip-flop is connected to the line frequency circuit of frequency dividers, an output of the first flip-flop being connected to the reset input S_2 of the second flip-flop which flip-flop provides the gating signal at an output, the reset input S_2 of the first flip-flop being connected to an output of the blocking signal generator. The gating signal generator may alternatively comprise a first J.K flip-flop a preparatory input of which is connected to the blocking signal generator, a command input of the flip-flop being connected to an auxiliary generator providing an auxiliary pulse of line frequency whilst the reset input of the flip-flop is connected to the line frequency circuit of frequency dividers, an output of the flip-flop being connected to a reset input of a second J.K flip-flop an output of which provides the gating signal and whose command input is connected to the clock-pulse generator. The said blocking signal generator may comprise a J.K flip-flop of the type having a trigger action on all J.K inputs which inputs are multiple preparatory inputs some of which receive auxiliary pulses at half line frequency.

The pulse generators and circuit of frequency dividers may incorporate J.K flip-flops which flip-flops may have given propagation delay times. In one arrangement a

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first input of one J.K flip-flop may be connected to the output of the clock pulse generator whilst a second input may be connected to the output of a further J.K flip-flop positioned n th in series from the first J.K flip-flop, the propagation delay time from the first input to the output being less than n times the propagation delay time of each J.K flip-flop. When one of the J.K flip-flops has a trigger action on its J and K inputs, and a trigger action on its J.K inputs, and in order to determine the timing of pulse edges generated by the flip-flop with a delay of the order of the propagation delay time a first command input of this flip-flop may be connected to receive divided clock pulses from a second J.K flip-flop provided in the circuit of frequency dividers, the second command input of the first mentioned flip-flop being connected to an output of a further J.K flip-flop which succeeds the second J.K flip-flop. The synchronising signal generator may include a J.K flip-flop provided with T, K, J and S₂ inputs each input having a trigger action.

The television pulse generator when for use with the N.T.S.C. colour television standard may be provided with a N.T.S.C. chrominance subcarrier gating signal generator comprising a J.K flip-flop a command input of which is coupled to the clock pulse generator, a first preparatory input of the flip-flop being coupled through a differentiating circuit to the synchronising signal generator, a second preparatory input of the flip-flop being connected to the circuit of frequency dividers whilst a reset input of the flip-flop is coupled for blocking purposes to one of the pulse generators providing an auxiliary pulse of field frequency.

One of the pulse generators may supply pulses of relatively short duration at field frequency which pulse generator comprises a gate an input of which is coupled to a generator supplying pulses of relatively long duration at field frequency and to the field frequency circuit of frequency dividers.

In order that the invention may be readily carried into effect, embodiments thereof will now be described in detail, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of a television pulse generator according to the invention.

Figure 2 shows the television pulse generator of Figure 1 in greater detail.

Figures 3 and 4 show the relation of time between signals occurring in the television pulse generator.

Figure 5 serves to explain the generation of signals having pulses of field frequency.

Figures 6 and 7 serve to explain the generation and the influence of a signal with auxiliary

pulses occurring at line frequency and at double line frequency.

Figure 8 shows the pulses occurring in a blanking signal generator of the television pulse generator of Figures 1 and 2.

Figure 9 relates, similarly as Figure 8, to a synchronizing signal generator in the television pulse generator.

Figure 10 shows a detail of a pulse generator suitable for generating a PAL chrominance subcarrier gating signal.

Figure 11 serves to explain the generation of the PAL gating signal occurring at the line frequency.

Figure 12 shows a few auxiliary pulses.

Figure 13 serves to explain the generation of a field-shifted PAL blocking signal of nine line periods.

Figure 14 shows a block diagram of a television pulse generator switchable between a plurality of television standards according to the invention, shown in the position for the RTMA standard (R).

Figure 15 shows the television pulse generator according to Figure 14 in greater detail.

Figure 16 serves to determine the relationship between some signals laid down in accordance with the RTMA standard for colour television and generated with the aid of the television pulse generator according to Figures 14 and 15.

Figures 17 and 18 show the time relation between signals occurring in the television pulse generator according to Figures 14 and 15.

Figure 19 serves to explain the generation of signals having pulses of field frequency.

Figures 20 and 21 serve to explain the generation and the influence of a signal with pulses occurring at line frequency and at double line frequency.

Figure 22 shows the pulses for the RTMA standard occurring in a blanking signal generator of the television pulse generator of Figures 14 and 15.

Figure 23 shows, similarly as Figure 22, a synchronizing signal generator in the television pulse generator.

Figure 24 shows in greater detail a generator which can be connected to the television pulse generator of Figures 14 and 15, and which is suitable for generating an NTSC or PAL chrominance subcarrier gating signal for the RTMA or CCIR standard.

Figure 25 serves to explain the generation of the NTSC gating signal occurring at the line frequency and of an auxiliary pulse to be used for generating the PAL gating signal.

Figure 26 shows the time relation between signals in the television pulse generator of Figures 14 and 15, used in the position for the CCIR standard (C), and

Figure 27 serves to explain the generation

of signals with pulses of field frequency for the CCIR standard.

In Figure 1 the reference A denotes a clock pulse generator an input of which is connected to a phase discriminator B for the purpose of synchronisation. A generator is denoted by the general reference G. An output of the clock pulse generator A is connected to a circuit of frequency dividers D, E and F. The frequency divider F which provides a signal f at a frequency of ν_H which represents the line frequency in a television system is connected to an input of the phase discriminator B to another input of which an external synchronizing signal of the frequency ν_H (not shown) is applied. For a choice of the clock pulse frequency of $80 \nu_H$, which choice has been made in the manner to be hereinafter described, the signal a provided by the generator A undergoes a division by 5, 8 and 2, respectively, by the frequency dividers D, E and F, respectively.

An output of the divider E conveying a signal at double the line frequency is connected to a circuit of frequency dividers L and M having a dividend of 5 and 125, respectively. For a 625-line system employing interlacing the frequency divider M provides a signal of a frequency ν_V which represents the field frequency. The dividers L and M are provided with an input to which an external synchronizing signal s_{VHS} may be applied for purposes of synchronisation. In the signals shown in Figure 1 a line period T_H and a field period T_V are shown in the signals occurring at the line and field frequencies, respectively.

Outputs of various divider stages of the frequency dividers L and M are connected to pulse generators denoted by the references, X, Y and Z, which are also mutually coupled. Under the influence of output signals from the dividers L and M, which signals will be further referred to hereinafter, the pulse generators X, Y and Z provide signals x , y and z including pulses occurring at the field frequency and having a pulse duration of $20 T_H$, $7.5 T_H$ and $2.5 T_H$, respectively. These pulse periods in the signals x , y and z laid down in the CCIR standard provide approximately the field blanking period, the equalizing and field synchronizing period and exclusively the field synchronizing period, respectively.

The signals y and z and the signal x are applied to a synchronizing signal generator P and to a blanking signal generator W, respectively, other inputs of which are coupled to divider stages of the frequency dividers in the circuit D, E, F. The outputs of the generators P and W convey signals p and w which correspond to a different pulse series including pulses of different duration and repetition period.

In addition to a certain choice of coupling the circuits D, E, F and L, M with the pulse generators X, Y, Z and the signal generators P and W, the pulse generator of Figure 1 is provided with a pulse generator I forming part of the said coupling. The pulse generator I provides a signal i shown in Figure 1,

(and the inverse thereof $\bar{i}$) which beyond the equalising and field synchronizing period of $7.5 T_H$ laid down by signal y has auxiliary pulses occurring at the line frequency, which auxiliary pulses occur within this period at double the line frequency.

To explain the importance of the choice of the frequency of $80 \nu_H$ of the clock pulse generator A and of the choice of coupling comprising the pulse generator I, Figure 1 will be further described in combination with the detailed embodiment of Figure 2, and the signals shown in the following Figures. In Figure 2 some components of Figure 1 are not shown, whereas other components, such as for example the divider stages of the frequency dividers of the circuits D, E, F and L, M are shown separately. In Figure 1 the direction of signal transmission in a general sense is denoted by a single arrow head, whereas, as will be apparent, signal paths giving an important trigger action on the generators X, Y, Z, I, P and W are provided with double arrow heads. On the other hand the corresponding signal paths giving a trigger action are shown in Figure 2 with single arrow heads for the sake of simplicity.

Generator Z shown in Figure 1 is formed in Figure 2 as a NAND gate and the frequency dividers D, E, F, L and M, and the generators X, Y, I, P and W are formed with JK flip-flops in Figure 2. These digital circuit elements are bulk-manufactured and have a great accuracy and a long lifetime as is required for use in computers. In the description of Figure 2 the flip-flop indication will be used instead of the divider and generator indication. For the chosen type all single-fold inputs and outputs of the flip-flop Y are used, so that this will be described in general in order to explain the operation of a JK flip-flop. As used in an embodiment of the pulse generator of Figure 2, two JK flip-flops may constitute one component such as, for example, in the type FCJ 121 one flip-flop of which is denoted by $\frac{1}{2}$ FCJ 121. The JK flip-flop Y has a command input denoted by the reference T and an arrow head and two preparatory inputs denoted by the references J and K and determining whether the flip-flop changes over or does not change over. A reset input is denoted by the reference S_2 . Two outputs Q_1 and Q_2 convey inverse signals which are denoted by y and $\bar{y}$, respectively, for the flip-flop Y. Two combined flip-flops in one FCJ 121 have

only a common reset input S_2 . The inputs J and K may alternatively be formed in a multifold manner through an AND gate such as is shown for the J inputs J_1 and J_2 of the flip-flops I and W and in which it applies that $J = J_1 \cdot J_2$.

Generally the following applies for a JK flip-flop while starting from the so-called positive logic having a high potential corresponding to a logic 1 and a low potential corresponding to a logic 0, while an unconnected input conveys a logic 1 through internal couplings.

If a logic 1 is impressed on the S_2 input of the flip-flop Y or if it is not connected ($S_2(Y) = 1$), then it does not exert influence. If a variation from a logic 1 to 0 ($S_2(Y) = 1 \rightarrow 0$) at the S_2 input or if there is a logic 0 ($S_2(Y) = 0$), the Q_1 output must pass from the logic 1 to 0 ($Q_1(Y) = 1 \rightarrow 0$) or the Q_1 output remains 0 ($Q_1(Y) = 0$). For the inverse Q_2 output it follows that Q_2

(Y) $0 \rightarrow 1$ or $Q_2(Y) = 1$. The JK flip-flop Y changes over under the influence of the signals at the J and K inputs only when a logic 1 becomes a 0 at the T input ($T(Y) = 1 \rightarrow 0$). For a logic 0 at the T input ($T(Y) = 0$) the signals at the J and K inputs do not exert influence and may vary arbitrarily.

For a logic 1 at the T input ($T(Y) = 1$) the signal at the J and K inputs constitute the basis for causing the flip-flop to either change over or not when $T(Y) = 1 \rightarrow 0$, in which a logic 1 is predominant relative to a 0, that is to say, a logic 1 occurring for a short instant at the J or K input during $T(Y) = 1$ determines if the flip-flop either changes over or not rather than does a logic 0 which is present for a long period.

Taking the foregoing into account and using the introduced notation, the following applies generally for a JK flip-flop.

TABLE 1

For $T = 1 \rightarrow 0$

J	K	Q_1	Q_2
0	0	Q_1 remains Q_1	Q_2 remains Q_2
0	1	0	1
1	0	1	0
1	1	Q_1 changes over	Q_2 changes over

In the description of Figure 9 and Table 5 reference will be made to the flip-flop P having 3 J and K inputs (type FCJ 201) which may alternatively serve as command or trigger inputs when $T = 1$.

The inputs and outputs which are connected to other outputs and inputs are shown for the JK flip-flops of Figure 2. For connections which are important for the invention, Figures 1 and 2 show the output signals which are partly plotted as a function of time in Figures 3—9. Since the inverse signals of the Q_2 outputs only differ in polarity from the signals of the Q_1 outputs, only the latter are plotted in Figures 3 and 4.

Starting from the clock pulse signal a , Figure 3 shows the signals $d1$, $d2$ and $d3$ of the 5-to-1 divider D consisting of 3 flip-flops D1, D2 and D3, the signals $e1$, $e2$ and $e3$ of the 8-to-1 divider E consisting of 3 flip-flops E1, E2 and E3 and the signal f of the flip-flop F acting as a 2-to-1 divider. Furthermore Figure 3 shows a few signals including pulses occurring at the line frequency and at the double line frequency which are in a close relation with the clock pulses in the signal a such as: in the signal i the auxiliary pulses occurring at the line frequency and during the $7.5 T_H$ period at the double line frequency; a line synchronizing pulse shown in signal s_{RP} ; two equalizing pulses occurring at the double line frequency shown in signal s_{RP} ; two raster serrations occurring in signal s_{RS} at the double line frequency and a line blanking pulse occurring in signal s_{RW} .

Figure 3 shows by way of the instant t_0 the commencement of one line period and t_{80} shows the end which corresponds to the instant t_0 of a subsequent line period. Clock pulses occur in the signal a between t_0 and t_{80} so that the difference between two successive instants ($t_0, t_{15}, t_{30}, \dots, t_{80}$) corresponds to one clock pulse period. Figure 2 shows that the clock pulses of signal a are applied to the T input of the flip-flops D1 and D2, that is to say, to both inputs T(D1) and T(D2). Negatively directed edges

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in the signal a and other signals which are active as trigger edges and cause a flip-flop to change over are partially provided with arrow heads. To explain the operation of the 5-to-1 divider D including the 3 flip-

flops D1, D2 and D3 and to give the mutual connections a Table 2 follows in which the variations shown in the signals d_1 , d_2 and d_3 of Figure 3 are derived with the aid of Table 1.

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TABLE 2

Frequency Divider D					D2			D3		
D1 K = 1					J = 1			J = K = 1		
Table 1 $\rightarrow \begin{cases} J = 0 \rightarrow Q_1 = 0 \\ J = 1 \rightarrow \text{change-over} \end{cases}$					$K = 0 \rightarrow Q_1 = 1$ $K = 1 \rightarrow \text{change-over}$			change-over		
Signal t $\downarrow$	T a	J d3	Q ₁ d1	Q ₂ $\bar{d}1$	K $\bar{d}1$	Q ₁ d2	Q ₂ $\bar{d}2$	T d2	Q ₁ d3	Q ₂ $\bar{d}3$
$t_0 - \Delta t$	1	1	0	1	1	0	1	0	1	0
t_0	1 $\rightarrow$ 0	1	1	0	0	1	0	1	1	0
t_1	1 $\rightarrow$ 0	1	0	1	1	1	0	1	1	0
t_2	1 $\rightarrow$ 0	0	1	0	0	0	1	0	0	1
t_3	1 $\rightarrow$ 0	0	0	1	1	1	0	1	0	1
t_4	1 $\rightarrow$ 0	1	0	1	1	0	1	0	1	0
t_5	1 $\rightarrow$ 0	1	1	0	0	1	0	1	1	0
t_6	1 $\rightarrow$ 0	1	0	1	1	1	0	1	1	0
t_7	1 $\rightarrow$ 0	0	1	0	0	0	1	0	0	1
t_8	1 $\rightarrow$ 0	0	0	1	1	1	0	1	0	1
t_9	1 $\rightarrow$ 0	1	0	1	1	0	1	0	1	0
t_{10}	1 $\rightarrow$ 0	1	1	0	0	1	0	1	1	0

In Table 2 delays occurring in the flip-flop D1, D2 and D3 are not taken into account. For the purpose of further explanation of Table 2 the following applies:

The reference $t_0 - \Delta t$ denotes at instant which lies just before the instant t_0 . At the instant $t_0 - \Delta t$ the signal a has the value 1. It is desirable for the 5-to-1 divider D that at the instant t_0 when there applies that $T(D1) = T(D2) = 1 \rightarrow 0$, the flip-flop D1 and D2 change over so that $t_0 - \Delta t$ $J(D1) = 1$ and $K(D2) = 1$. It follows therefrom that at $t_0 - \Delta t$ $Q_2(D1) = K(D2) = 1$ and $Q_1(D3) = J(D1) = 1$. To ensure that D3 certainly does not change over at the instant t_0 , $T(D3) = 0 = Q_1(D2)$ at $t_0 - \Delta t$. The rows and columns shown in Table 2 can subse-

quently be derived in a simple manner by considering for a certain instant the value of $J(D1) = d3$ of a previous instant.

Table 2 shows that the rows at the instants $t_0, t_5, t_{10} \dots; t_1, t_6 \dots$ etc. are the same. In Figure 3 it can be seen from signal $d3$ that the divider D thus dividing by five is active as an asymmetrical divider, while the edges are indicated over one arbitrary period at the instants t_2, t_4 to t_7 .

In Table 2 it has been stipulated that delays in the JK flip-flops D1, D2 and D3 have not been taken into account. It is found from data in the Handbooks that a JK flip-flop FCJ 121 has an average propagation delay time t_{pd} of 105 ns as a maximum between a T input and a Q output. Measure-

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ments yielded a t_{pd} of 70 ns as an average. For the sake of simplicity Figure 3 mentions the propagation delay time t_{pd} as t_0 . As a reference value, relative to which the successive propagation delay times of the JK flip-flops will be considered, the edges in the signals $d1$ and $d2$ are taken which coincide with the instants t_0, t_1, t_2, t_3 , etc. As a result the trigger edges, which are sometimes denoted by arrow heads, occur in the signal a in Figure 3 at a time t_0 before the instants t_0, t_1, t_2 , etc. As is indicated at the instant t_0 in signal d_3 , the pulse edges in this signal have a delay time t_0 .

After the detailed description of the frequency divider D including the flip-flops D1, D2 and D3 only the following connections are given for the following asymmetrical frequency dividers E, F, L and M:

$T(E1)=Q_2(D1)$ $J(E1)=K(E1)=Q_2(D3)$
 $T(E2)=Q_{11}(E1)$ $T(E3)=Q_1(E2)$
 $T(F)=Q_2(E3)$
 $T(L1)=T(L2)=Q_1(E3)$ $K(L1)=Q_2(L2)$
 $J(L2)=Q_1(L3)$ $K(L2)=Q_1(L1)$
 $T(L3)=Q_2(L1)$ $T(M1)=Q_2(L2)$
 $T(M2)=Q_2(M1)$ $T(M3)=Q_2(M2)$
 $T(M4)=Q_1(M3) \dots T(M7)=Q_1(M6)$
 $S_2(M1)=S_2(M2)=Q_2(M7)$ via differentiation.

Some important points are the following: As it applies for the JK flip-flop E1 that

$T(E1)=\bar{d1}$ the signal $e1$ only has a delay time of $1t_0$ while the subsequent successively connected flip-flops E2, E3 and F have a delay time of $2t_0, 3t_0$ and $4t_0$.

Figure 4 shows the result of the connection of the divider E3 with a trigger signal $e3$ to the 5-to-1 divider L (Figure 1) consisting of three JK flip-flops L1, L2 and L3. The signals $m1$ to $m7$ inclusive are also shown, which signals are associated with seven JK flip-flops M1 to M7 inclusive which constitute the 125-to-1 divider M.

The propagation delay times then range from $3t_0$ to $11t_0$ inclusive. The propagation delay time corresponds to a sequential number of the JK flip-flop calculated on the flip-flops D1 and D2 which determine the time scale $t_0 \dots t_{80}$ and are therefore also calculated on the clock pulse generator A.

In the signal $e3$ of Figure 4 a line period T_H has been shown from an instant t_0 occurring periodically at the line frequency (the delay time $3t_0$ is left out of consideration). For obtaining in a similar manner a time scale of field frequency an instant t_{100} is shown at the signal $m1$ which gives the periodical instant of commencement of a field time scale calculated on the signal $m1$. The edges occurring in the signal $e3$ determine approximately the successive instants $t_{101}, t_{102} \dots t_{110} \dots t_{120} \dots t_{130}, t_{131} \dots t_{1350}=t_{100}$ which apply to

two different time scales for the signals $e3, l1, l2, l3$ and $m1 \dots m7$.

Since the divider M consisting of seven divider stages in Figure 2 would divide further steps by $2^7=128$ instead of to 125,

the output $Q_2(M7)$ with the signal $\bar{m7}$ is coupled for an internal resetting at the instant t_{740} to the reset inputs $S_2(M1)$ and $S_2(M2)$. This coupling is effected through a differentiating circuit which includes a capacitor C_1 and two resistors R_1 and R_2 arranged in series between ground and a potential U. The junction of the resistors R_1 and R_2 is coupled through a diode T_1 blocking the internal reset pulse to the reset inputs of the flip-flops L1, L2, L3, M3 $\dots$ M7, the purpose (synchronizing purposes) being further referred to hereinafter. Either the complete potential U or a portion thereof corresponds to the already mentioned logic 1 while the ground potential corresponds to the logic 0.

As in Figure 1, Figure 4 shows the signals x, y and z , but in relation to the signals $e3, l1 \dots l3, m1 \dots m7$. The external synchronizing signal s_{ves} is also shown.

Starting from the values already given for the pulse duration in the signals x, y and z for a certain television standard, namely the CCIR standard, these values may be produced with the connections shown in Figure 2 by means of two JK flip-flops X and Y and one NAND gate Z, while Figure 5 shows the signal variation.

Figure 2 shows that the T input of flip-flop X is connected to the Q_1 output of flip-flop M2 and that the J input is connected to the Q_1 output of M4.

The K input of flip-flop X is connected to a differentiating circuit including a resistor R_3 to ground and a capacitor C_2 to the Q_2 output of flip-flop M7. The signals shown in Figure 5 occur at the inputs of flip-flop

X, in which $T=m2, J=m4$ and $K=\bar{m7}$. The index notation relates to a differentiated signal.

In Figure 5 the propagation delay times (a number of times t_0) shown in Figure 4 are included in the graphic representation. As compared with the time scale with the instant t_{100} calculated on the signal $m1$, the edges of signals $m2, m4$ and $m7$ have a delay time of $1t_0, 3t_0$ and $6t_0$. At the instant

$t_{100}+6t_0$ the signal $\bar{m7}$ has the logic 1 for a short moment, which value as given with reference to the general description and Table 1 of the JK flip-flop Y is predominant relative to the logic 0. The flip-flop X therefore assumes the state at which $J(X)=0, K(X)=1$, so that it follows with the aid of Table 1 that the Q_1 output of X must convey the logic 0 after the instant $t_{120}+1t_0$ at which $T(X)1 \rightarrow 0$. At the instant $t_{120}+2t_0$,

the flip-flop X changes over and the logic 1 information on the K input is lost due to internal couplings. A subsequent trigger edge in the signal $m2$ occurs shortly after the instant t_{180} . Then, however, $J(X)=K(X)=0$ and the flip-flop X remains in the same state. For the trigger edge shortly after the instant t_{200} , the J input of flip-flop X has gone from the logic 0 to 1. At the instant $t_{200}+1t_Q$ there applies that $J(X)=1$ and $K(X)=0$ so that the Q_1 output must convey the logic 1. For the remaining period of a field period T_V there continues to apply that $K(X)=0$ while $J(X)$ may be either 0 or 1. It follows from Table 1 that when $Q_1(X)=1$, the flip-flop X does not change over. The negatively

directed edge in the signal $m7$ (not shown) occurring at the instant t_{740} (see Figure 4) has no influence on the flip-flop X; the logic 0 remains present.

According to Figure 2 the connections for the flip-flop Y are as follows:

$T(Y)=Q_2(L_2)$, $J(Y)=Q_1(M_2)$ and $K(Y)$ to ground while the S_2 input is connected to the Q_1 output of the flip-flop X through a differentiating circuit which comprises two resistors R_4 and R_5 arranged in series between ground and the potential U, and a capacitor C_3 .

The signals shown in Figure 5 occur at the inputs of the flip-flop Y at which $T=\overline{12}$, $J=m2$, $K=0$ and $S2=x'$ (signal x differentiated). Likewise, as in the signals associated with the flip-flop X, a few propagation delay times are mentioned.

It follows with the aid of Table 1 for the flip-flop Y that for $K=0$ and $J=0$ or 1, the stable state of the flip-flop corresponds to a logic 1 on the Q_1 output. At the instant $t_{120}+2t_Q$ an edge $1 \rightarrow 0$ appears in the signal x' at the S_2 input so that in accordance with the description with reference to Table 1

the Q_1 output must assume the logic 0. At the instants t_{180} and t_{140} negatively directed edges occur at the T input neither of which edges influence the state of the flip-flop Y. Particularly at the instant $t_{140}-1t_Q$ there is shown that for $J=K=0$ the flip-flop does not change over. At the instant $t_{180}-1t_Q$, however, $J=1$, $K=0$ so that at the instant t_{180} the Q_1 output conveys the logic 1. The flip-flop Y remains in this state until an edge $1 \rightarrow 0$ active as a trigger edge occurs in the signal x' during a subsequent field period T_V .

Figure 2 shows the NAND gate Z whose inputs are connected in a manner not shown to $Q_2(M1)$ and $Q_2(Y)$. The output of the

gate Z thus conveys a signal $z=y.m1=\overline{y+m1}$ which is shown in Figure 5. Before further describing the generation of the signal i (Figure 3) including auxiliary pulses occurring at the line frequency and at the double line frequency, the requirements which are imposed on the signals generated by a pulse generator which is suitable for the CCIR standard according to the embodiment shown in Figures 1 and 2 will first be dealt with so as to explain certain choices made in accordance with the invention. Already shown are a field synchronizing period of $2.5 T_H$ (signal x) an equalizing and field synchronizing period of $7.5 T_H$ (signal y) and a field blanking period of approximately $20 T_H$ (signal x). In this case it is prescribed that 5 equalizing pulses of the double line frequency must precede and follow 5 field synchronizing pulses of the double line frequency. The duration of the field blanking period in the composite blanking signal must then be $20 T_H \pm 2 T_H + 1$ line blanking pulse duration. Furthermore, the requirements mentioned in the following Table 3 apply, which requirements are derived from the signals shown in Figure 3.

TABLE 3

(Figure 3)

CCIR-standard

Signal s_{HP} , line synchronising pulse duration:	$4.7 \pm 0.2 \mu s.$
Signal s_{EP} , equalizing pulse duration:	$2.3 \pm 0.1 \mu s.$
Signal s_{VS} , raster serration duration:	$4.7 \pm 0.2 \mu s.$
Signal s_{HW} , line blanking pulse duration:	$12.05 \pm 0.25 \mu s.$
Front porch = time difference pulse leading edges in signals s_{HW} and s_{HP} :	$1.55 \pm 0.25 \mu s.$

Such a number of requirements may be met in a simple manner by the embodiment of a pulse generator according to the invention shown in Figures 1 and 2. Here the recognition becomes manifest to determine the Highest Common Factor (H.C.F.) of the different pulse periods and time differences between the pulse leading edges and to relate the H.C.F. to the smallest pulse edge spacing. As a result correctly chosen edges of the pulses in the frequency divider stages connected to the clock pulse generator A can determine in a direct manner the pulse edges accurately laid down in the standard in the signals to be generated.

A H.C.F. of the numbers 1.55; 2.3; 4.7 and 12.05 or an approximation thereof is to be found which H.C.F. must be a factor of the smallest pulse repetition period, which is half a line period $\frac{1}{2}T_H = 32 \mu s$. The reason thereof is that the smallest pulse repetition period imposes the most stringent requirements on a smooth periodicity in the gener-

tion of signals. It follows that the number 0.8 reasonably satisfies as a precise factor of 32 while being a factor of the relevant numbers: 1.6; 2.4; 4.8 and 12.0. A period of $0.8 \mu s$ and a frequency of 1.25 MHz (80 times line frequency) corresponds thereto for the clock pulse generator A. Other possible values could be 0.4; 0.2; $0.1 \dots \mu s$ with a frequency of 2.5; 5; $10 \dots MHz$.

Both in Table 3 and in practice stringent requirements are imposed on the accuracy of the line synchronising pulse duration in the signal s_{HP} and particularly the equalizing pulse duration in the signal s_{EP} . By using the propagation delay time t_{pd} ($=t_0$ in the Figures) occurring in the JK flip-flops of Figure 2 and being 70 ns at an average, this time may be deducted from the pulse duration in the generated signals. Table 4 shows the pulse periods prescribed by the CCIR standard and reached in practice in a pulse generator according to the invention.

TABLE 4

	CCIR standard	In practice
s_{EP}	$4.7 \pm 0.2 \mu s$	4.73
s_{EP}	$2.3 \pm 0.1 \mu s$	2.33
s_{VS}	$4.7 \pm 0.2 \mu s$	4.80
s_{HW}	$12.05 \pm 0.25 \mu s$	12.00
Front porch	$1.55 \pm 0.25 \mu s$	1.60

To determine a few pulse edges the signal i is generated which includes auxiliary pulses of line frequency and double line frequency. Figure 2 shows the JK flip-flop I for which the associated signals are shown in Figure 6.

In Figure 2 the T input of the flip-flop I is connected to $Q_2(D_2)$ and the K input is connected to $Q_1(E_2)$. A J_1 input of the J input formed in a two-fold manner through an AND gate is connected to the output of a NAND gate N_1 whose inputs are connected to $Q_1(F)$ and $Q_1(Y)$. A J_2 input of flip-flop I is coupled through a differentiating circuit including a resistor R_4 to ground and a capacitor C_4 to $Q_2(E_3)$.

In Figure 6 the signals $T = \bar{d}2$, $J_1 = f + y$ are shown for the flip-flop I, for $J_1 = f, y =$

$\bar{f} + y$, $J_2 = \bar{e}3'$ and $K = e2$. In the first instance it is assumed that $y = 1$, that is to say, the operation of flip-flop I will be considered outside the equalizing and field synchronizing

period of $7.5 T_H$. The J_1 input then conveys

the signal $\bar{f}$ (solid lines). The time scale

$t_0 \dots t_{80}$ is derived from the signal $\bar{d}2$.

The edges in the signals $\bar{f}$, $\bar{e}3'$ and $e2$ have delay times $4t_0$, $3t_0$ and $2t_0$. Further reference is made to Table 1 for the explanation of the operation of the JK flip-flop I.

At the instant t_0 of Figure 6 the J input has a logic 0 because $J_2 = 0$. For $K = 1$ there applies for the stable state that $Q_1 = i = 0$. At the instant t_2 a negatively directed edge occurs on the T input. Meanwhile the J_2 input has received a logic 1 so that for $J_1 = J_2 = 1 = J$ $K = 0$ there applies that Q_1 must assume a logic 1. At the instant $t_6 + 1t_0$, Q_1 has become $i = 1$. The negatively directed edges in

the signal $T = \bar{d}2$ at the instants t_6 , t_8 and t_{10} do not result in variations of the flip-flop I because for $K = e2 = 0$ there applies that $Q_1 = i = 1$ is a stable state even when J_1 and J_2 vary between 0 and 1. At the instant

t_{13} , however, a trigger edge occurs when K has already previously become $e_2=1$. It follows that the flip-flop I must change over which happens at the instant $t_{13}+1t_0$ and at which Q_1 has become $i=0$.

Due to the choice of $K=e_2$ with a guaranteed delay time of $2t_0$ relative to the edges

in signal $T=d_2$, it has been achieved that at the instant t_{10} the flip-flop I certainly cannot change over, while it changes over as soon as possible after the instant t_{13} .

Certain requirements are to be imposed

on the signal $\bar{e}3'$ for the J_2 input. Due to the

choice of $\bar{e}3'$ it has been achieved by the delay time $3t_0$ after the instant t_0 that the flip-flop I at the instant t_0 is certainly not changed over. The differentiated pulse in

signal $\bar{e}3'$, which pulse is shown in a flattened manner and which may extend without any consequence to well above the value indicated by the logic 1, must not stop before the instant t_2 , for the predominant logic 1 is to occur between the instants t_2 and t_3

when $T=d_2=1$. Before the instant t_{15} the

pulse in signal $\bar{e}3'$ must have disappeared so as to avoid the predominant influence after

the instant t_{15} . The pulse in the signal $\bar{e}3'$ may thus vary between the broken lines in Figure 6.

At the instant t_{20} a negatively directed

pulse in the signal $J_2=\bar{e}3'$ occurs, which signal continues to represent the logic 0 and which does not exert influence on the action of flip-flop I .

Shortly after the instant t_{40} a following pulse

occurs in the signal $J_2=\bar{e}3'$. However, the

signal $\bar{f}$ at the J_1 input has the logic 0 so that for $J=0$ and $K=0$ or 1 there applies that $Q_1=i=0$ is the stable state.

The action of the flip-flop I in Figure 2 during the equalizing and field synchronizing period of $7.5 T_H$ may be explained by way of a combined consideration of Figures 6 and 7.

In Figure 7a the signal y is shown in relation to the field time scale $t_{100} \dots t_{1350}$ given in Figure 4. Figures 7b and 7c apply for two successive fields, while Figure 7b applies for a field ending at a half line and Figure 7c for a field ending at a full line. The signal $\bar{f}$

and for the flip-flop I the signals $J_1=\bar{f}+y$,

$J_2=\bar{e}3'$ and $Q_1=i$ are shown. The nega-

tively directed pulses without any influence

in the signal $J_2=\bar{e}3'$ of Figure 6 have been omitted in Figures 7b and 7c for the sake of simplicity.

For Figure 7b there applies that the instant t_{120} corresponds to the instant $t_{40}+5t_0$ in Figure 6. In Figure 6 it has already been explained what happens before the instant t_{120} . At the instant $t_{120}+3t_0$ in Figure 7b, which is the instant $t_{40}+8t_0$ in Figure 6, the edge occurs which is shown in a broken line in Figure 6. In the same manner as described in Figure 6 for the pulse in signal $Q_1=i$ occurring between the instants t_3+1t_0 and $t_{13}+1t_0$, a pulse shown in a broken line is generated in the signal $Q_1=i$ between the instants $t_{43}+1t_0$ and $t_{53}+1t_0$. It is found that during the $7.5 T_H$ period the pulses in the signal i are generated at the double line frequency. All this has also been shown for the signal i in Figure 3.

After the description of Figure 7b, Figure 7c is self-evident.

The influence of the auxiliary pulses in the signal i is found in a simple manner with reference to the description of the action of the JK flip-flop W in Figure 2. The signals for the flip-flop W which as a signal generator must provide the signal with a series of line and field blanking pulses are shown in Figure 8. Figure 8a shows the signals which are the same for each field and Figures 8b and 8c show in accordance with Figures 7b and 7c the signals which are different for successive fields.

In Figure 2 the connections of the inputs of the flip-flop W are as follows:

$$\begin{aligned} T(W) &= Q_1(D3), J_1(W) = Q_1(E3) \\ J_2(W) &= Q_1(X) \text{ and } K(W) = Q_1(I). \end{aligned}$$

In Figure 8a the signal $T=d3$ is partially indicated on two scales which are both derived from the time scale $t_0 \dots t_{20}$ and which relative thereto have a delay time of $1t_0$ which is left out of consideration in Figure 8. For the two-fold J input having an AND gate function the signal J follows from the signals $J_1=e3$ and delay time $3t_0$ and $J_2=x$ with delay time $7t_0$.

In Figure 8b the signal $K=i$ is shown for one field in relation to Figure 8a. The period denoted by $7.5 T_H$ ($y=0$) is considered to end during the period of the time axis being shown interrupted. At the instant t_2 a negatively directed edge occurs in the signal $T=d3$. In that case $J=K=0$ so that in accordance with Table 1 the flip-flop W does not change over. If prior to the instant t_2 it were allowed that J varies between 0 and 1, while as a result thereof the flip-flop W should not change over even once, then it follows from Table 1 that at this stable state the Q_1 output must have the logic 1. This is the starting point.

At the instant t_i , a subsequent negatively directed edge occurs in the signal $T=d3$. Meanwhile the signal $K=i$ has received the logic 1 at the instant t_s so that for $J=0$, $K=1$, the flip-flop W changes over and $Q_1=w$ changes from the logic 1 to the logic 0. A negatively directed edge in the signal $T=d3$ at the instant t_{12} does not exert influence on the flip-flop W. At the instant t_{13} the signal $K=i$ changes back from the logic 1 to the logic 0. A negatively directed edge occurring at the instant t_{17} in the signal $T=d3$ has for $J=0$ and $K=0$ no influence on the flip-flop W. At the instant t_{20} the signal $J_1=e3$ receives the logic 1 and hence the signal J. At the negatively directed edge occurring at the instant t_{22} in the signal $T=d3$ there applies that $J=1$, $K=0$ whereafter the Q_1 output must start to convey the logic 1. In that case J may change between 0 and 1 for $K=0$ without the negatively directed edges in the signal $T=d3$ causing the flip-flop W to change over. This state was taken as a starting point.

In Figure 8b the reference s_{HW} indicates a second pulse following the described pulse in the signal $Q_1=w$ which second pulse is also generated in the manner described.

The generation of the pulse in the signal $Q_1=w$ and denoted by the reference s_{HW} follows in the same manner for the signal $K=i$ shown in Figure 8c. To emphasize the fact that Figure 8c is shifted relative to 8b over half a line period $T_{H/2}$, a few instants $t_{40}, \dots, t_{80}=t_0, \dots, t_7, \dots, t_{22}$ have been indicated.

The auxiliary pulses in the signal i occurring at the line frequency determine in one field or in the other field approximately the position of the line blanking pulses s_{HW} to be generated in the signal w according to Figures 8b and 8c. The exact position of the edges of the line blanking pulses s_{HW} in the signal w are determined by the trigger edges in the signal $d3$. In Figure 3 the instants t_7+2t_0 and $t_{22}+2t_0$ are shown for the signal s_{HW} for the edges. The line blanking pulses in the signal s_{HW} are found to have a pulse duration of $15 \times 0.8 \mu s = 12 \mu s$ and fall within the limits imposed by the CCIR standard (Tables 3 and 4).

In Figure 8a an instant t_{40} is indicated in the signal $J_1=e3$ with the signal having the logic 0 at the instant $t_{40}+3t_0$ which value becomes manifest in the signal J. At the instant $t_{40}+7t_0$ the logic 0 occurs in the signal $J_2=x$ from which instant the period $20 T_H$ begins. What has been described with reference to the instants t_2 and t_7 now applies for the instants t_{42} and t_{47} because in the signal $K=i$ of Figure 8b the first auxiliary pulses occurring at the double line frequency begins at the instant t_{40} . The previous auxiliary pulse in the signal $K=i$ is then considered to be the

last pulse normally occurring at the line frequency.

With respect to Figure 8c there applies that the first auxiliary pulse in the signal $K=i$ after the instant when $J_2=x$ receives the logic 0 appears as the last pulse occurring normally at the line frequency.

After the logic 0 has been obtained in the signal $Q_1=w$ the signal J of Figure 8a is found to maintain the logic 0 during a period of approximately $20 T_H$ while K changes between 0 and 1. It is found from Table 1 that the signal $Q_1=w$ of Figure 8b and 8c maintains the logic 0 because this represents the stable state.

The flip-flop W changes over at the first negatively directed edge in the signal $T=d3$ after the signal J receives the logic 1 under the influence of the signal $J_1=e3$. The subsequent occurrence of an auxiliary pulse in signal $K=i$ of Figures 8b or 8c provides the opportunity for some negatively directed edges in the signal $T=d3$ of Figure 8c to cause the line blanking pulses s_{HW} to be generated by the flip-flop W. The flip-flop W generates a field blanking pulse at a duration of $20 T_H$ plus one line blanking pulse duration ($t_{22}-t_7$ and $t_{62}-t_{47}$).

The JK flip-flop of Figure 2 generates a signal $Q_1=p$ shown in Figure 9, which includes a series of line synchronizing pulses s_{HP} , equalizing pulses s_{EP} and field synchronizing pulses s_{VP} , equalizing pulses s_{EP} and field synchronizing pulses s_{VP} . The number of field synchronizing pulses s_{VP} is constituted by a single long field pulse which is cut into pieces by means of the said raster serrations s_{VS} .

The flip-flop P is not of the type FCJ 121 described so far but is a JK flip-flop of the type FCJ 201 which is formed with three J and K inputs having an AND gate function on which a trigger action may be performed.

The connections of the flip-flop P (in Figure 2) are as follows: $T(P)=Q_2(D1)$, $J1(P)=Q_2(E1)$, $J_2(P)=Q_1(D3)$, $J_3(P)=Q_1(I)$ and $K_1(P)=Q_1(E2)$. The input $K_2(P)$ is connected to the output of a NAND gate N2 with $Q_1(I)$ and $Q_1(Y)$ being connected to inputs thereof. The input $K_3(P)$ is connected to the output of the NAND gate Z. The input $S_2(P)$ is coupled to $Q_2(I)$ through a differentiating circuit including a capacitor C_5 and two resistors R_7 and R_8 arranged in series between the potential U and ground.

In addition to the Table 1 for the trigger action on the input T(P) and the description given with reference thereto a Table 5 also applies for the JK flip-flop P of the type FCJ 201 in which Table for T(P)=1 a trigger action on the J and/or K-input may be performed in case of a transition from the logic 1 to the logic 0.

TABLE 5

For $T = 1$.

J	K	Q_1	Q_2
$1 \rightarrow 0$	0 or 1	1	0
0 or 1	$1 \rightarrow 0$	0	1
$1 \rightarrow 0$	$1 \rightarrow 0$	Q_1 changes over	Q_2 changes over

The influence of the input signals according to Figure 9 may be explained with the aid of Tables 1 and 5.

- 5 Figure 9 relates to 19 half line periods $T_H/2$ occurring in and near the equalizing and field synchronizing period. The periods 1, 2, 3, 4; 7, 8, 9; 12, 13 and 17, 18, 19 are shown for the numbered half line periods. Only the first $16 \times 8 \mu s = 12.8 \mu s$ are shown for each half line period $T_H/2$ of 32 μs . The time axis in the signal $J_1 = e1$ is interrupted after the instant t_{16} so as to show that the signal has the same periodical character after this instant. The time axis in the signal $J_3 = i$ is shown in a broken line after the instant t_{16} so as to show that the signal can occur once at a maximum during one of the periods of time 1...19, considering the fact that the signal i has pulses of line frequency and double line frequency. The

- 20 signal $J_2 = d3$ is shown near the signal J so as to emphasize that the signals $J_1 = e1$ and $J_3 = i$ exert an inaccurate place-determining influence while an edge in the signal

- 25 $J_2 = d3$ has an accuracy-determining influence. Due to the repetition nature of the two television fields the time scale $t_0, \dots, t_{40}, \dots, t_{80} = t_0$ given with signal J may alternatively be considered as $t_{40}, \dots, t_{80} = t_0, \dots, t_{40}$.

- 30 The signal $K_3 = z$ is shown in an uninterrupted manner so as to clarify that it includes a pulse of field frequency which has the logic 0 during the periods of time 8...12

- 35 (2.5 T_H). In the signal $K_2 = i$. $y = \overline{i+y}$ the same applies for the periods of

- 40 3...17 (7.5 T_H) in which the signal $\overline{y}$ has the logic 1. The total signal K is constituted through an AND function together with the signal $K_1 = e2$.

Analogously to the signal $J_3 = i$, signal $S_2 = i'$ (signal i differentiated) is shown. The signal $T = d1$ and the signal $S_2 = i'$ may be found to have an accuracy-determin-

ing influence while the signal K only has a choice influence. 45

During the periods 1, 2 and 18, 19 the

signals $J_3 = i$ and J , $K_2 = \overline{i+y}$ and K , and

the signal $S_2 = i'$ are shown with portions consisting of broken lines and chain-link lines as well as the portions in the signal $Q_1 = p$ resulting therefrom due to the action of the flip-flop P. The reason thereof resides in the repetitive nature of the two television fields. The chain-link line portion in the periods of time 1, 2 and 18, 19 is associated with the field which ends with a full line prior to the equalizing and field synchronizing period, as has been described with reference to Figures 7c and 8c. The broken line portion corresponds to the state described with reference to Figures 7b and 8b. 50 55 60

The consideration of the period 1 with the chain-link line portion in the signals of Figure 9 leads to the following: around the instant t_0 , $J = 0$ and K may have the logic 1 or 0. It follows from Table 1 that for the stable state of flip-flop P the requirement is that Q_1 has the logic 0. It follows from Table 5 that with a variation of K from 1 to 0 for $T = 1$, the stable state also occurs for $Q_1 = 0$. It is found that without a variation in J the flip-flop P cannot change over. 65 70

At the instant t_3 the logic 1 occurs in the signal $J_3 = i$, whereafter the signal $J_1 = e1$ follows at the instant t_6 . The result is that 75

a logic 1 in the signal $J_2 = d3$ becomes manifest between the instants t_7 and t_8 in the signal J . At the instant t_8 an edge going from the logic 1 to 0 occurs in the signal J 80

while at the same time the signal $T = d1$ has the value 1. It follows from Table 5 that the flip-flop P will change over because the signal $Q_1 = p$ must assume the logic 1. 85

The reset pulse at the instant t_8 occurring in signal $S_2 = i'$ does not exert any influence because the signal $Q_1 = p$ has the logic 0 at t_8 .

After the instant t_0 , the signal K may exert influence on the flip-flop P . At the instant t_{12} the signal K assumes the logic 1 under the influence of the then occurring logic 1 in

5 the signal $K_3 = \bar{i} + y$.

After the instant t_0 , two negatively directed edges occur in the signal $T = \bar{d}1$, the instant t_{12} being denoted at the second edge. At the instant t_{12} there applies that $J = K = 0$ so that it follows from Table 1 that the flip-flop P does not change over. The subsequent

10 negatively directed edge in the signal $T = \bar{d}1$ occurs at the instant t_{15} . Now, however, $J = 0$ and $K = 1$ so that according to Table 1 the output $Q_1(P)$ must convey the logic 0 so that the flip-flop P changes over at the instant t_{15} .

During the rest of the period of time 1 and the entire period of time 2, J remains 0 which follows from the chain-link line portion in the signal $J_3 = \bar{i}$. As a result the flip-flop P remains in the same state as has been seen at the instant t_0 .

25 Comparison of Figures 3 and 9 shows that the periods 1 and 2 in Figure 9 correspond to the two half line periods $T_H/2$ of Figure 3. The signal s_{HP} in Figure 3 corresponds to the pulse s_{HP} in Figure 9. It is found from Figure 9 that a trigger edge in the signal

30 $J_3 = \bar{d}3$ (having a delay time of $1t_0$ relative to the time scale $t_0 \dots t_{30}$) determines the leading edge of the pulse s_{HP} while the trailing edge is determined by a trigger edge in

35 the signal $T = \bar{d}1$ (without delay time relative to the time scale $t_0 \dots t_{30}$). The result is shown in Figure 3 in which the leading edge in the signal s_{HP} is located at the instant $t_0 + 2t_0$ while the trailing edge is located at the instant $t_{15} + 1t_0$. The line synchronizing pulse s_{HP} therefore has an accurately determined pulse duration of $6 \times 0.8 \mu s$ minus approximately 70 ns, that is to say, $4.73 \mu s$.

40 What has been described for the period 1 in Figure 9 likewise applies to the period 2 for the signals which are shown by means of broken lines so that a detailed description is omitted.

45 It is to be noted that the signal $J_3 = \bar{i}$ has a keying function for generating or not generating a line synchronizing pulse s_{HP} during half a line period. The presence of the

50 signal i in the signal $K_3 = \bar{i} + y$ becomes manifest in the signal K by giving an edge at the instant t_{15} instead of an edge at t_{10} under the influence of $K_1 = e2$. The edge in the signal K occurring at the instant t_{10} does not exert any influence on the generation of the pulses s_{HP} occurring at the line frequency.

During the periods 3...17 of Figure 9 60 constituting the equalizing and field synchronizing period ($7.5 T_H$) the auxiliary pulses occur each period in the signal $J_3 = \bar{i}$ and then provide in signal J the pulse keyed from

65 the signal $J_3 = \bar{d}3$. The signal K is determined in the periods 3...7 and 13...17 by the signal $K_1 = e2$ because only the component $y = 1$ becomes manifest in the signal $K_3 = \bar{i} + y$. During the periods of time 8...12 (the field synchronizing period of $2.5 T_H$) the signal 70 $K_3 = x = 0$ is predominant in the signal K .

Analogously as described with reference to the period 1, the flip-flop P changes over during the period 3 at the instant t_0 . Subsequently, at the instant t_{10} , a negatively directed 75

edge occurs in the signal $T = \bar{d}1$. At the instant t_{10} the signal K still has the logic 0 whereafter it obtains the logic 1 at the instant $t_{10} + 2t_0$ due to the signal $K_1 = e2$. The subsequent negatively directed 80

edge in the signal $T = \bar{d}1$ at the instant t_{12} causes the flip-flop P to change over. The same is effected during the periods 4...7 and 13...17. The result is that the equalizing pulse s_{HP} is generated in the signal 85 $Q_1 = p$. The edges of the equalizing pulse s_{HP} are determined in the same manner as those in the line synchronizing pulse s_{HP} . In Figure 3 two equalizing pulses occurring at double the line frequency are shown in the signal s_{HP} . The pulse duration of the first pulse ranges from $t_0 + 2t_0$ to $t_{12} + 1t_0$, that is to say, $3 \times 0.8 \mu s$ minus approximately 70 ns being $2.33 \mu s$ which value also applies 90 to the other pulse.

During the period 8 of Figure 9 the flip-flop P changes over at the instant t_0 analogously as described with reference to the period 1. The signal $K_3 = x$ results in the signal K having the logic 0 during the periods 8...12. It follows from the foregoing that consequently the signal K during these periods does not exert influence on the state of the flip-flop P . From the instant t_0 the signal 100 $Q_1 = p$ continues to convey the logic 1 throughout the period 8 and even up to the period 9.

During the period 9 a reset pulse going from the logic 1 to 0 occurs at the instant

105 t_0 in the signal $S = \bar{i}'$. It follows from Table 1 that this reset pulse gives the output $Q_1(P)$ the logic 0. Subsequently the signal J results in a change-over of the flip-flop P at the instant t_0 . The same is repeated in the periods 10, 11 and 12. A pulse generated in this manner in the signal $Q_1 = p$ is denoted by 115 s_{VS} . The pulse s_{VS} occurring at the double line frequency and being devoted as a raster

serration has its leading edge at the instant t_s determined by the signal i and its trailing edge at the instant t_s is determined by the

5 signal $d3$. In Figure 3 the instants $t_s + 2t_q$ and $t_s + 2t_q$ are denoted in the signal s_{VS} and the pulse duration is $6 \times 0.8 \mu s = 4.8 \mu s$.

During the period 13 of Figure 9 the flip-flop P is reset to the input $S_2(P)$ of Figure 2 at the instant t_s whereafter the equalizing pulses are generated during the periods 13...17 as described with reference to the periods 3...7.

10 It is to be noted that during the period 13 an edge $1 \rightarrow 0$ occurs at the instant $t_s + 2t_q$ in the signal $K_1 = e_2$. Subsequently, an edge $0 \rightarrow 1$ occurs at the instant $t_s + 5t_q$ in the signal $K_3 = z$. The result is that the signal K maintains the logic 0 until the instant $t_{10} + 2t_q$. This result has been achieved by the choice that the K_1 and K_3 inputs of the flip-flop P are connected to the flip-flop E2 and through the NAND gate Z to the flip-flop M1 each having a different added propagation delay time ($2t_q$ relative to $5t_q$).

15 This added propagation delay time depends on the sequential number of the JK flip-flop calculated relative to the clock pulse generator A or, considering the introduced time scale of line frequency, relative to the flip-flops D1 and D2. Such a choice ensuring satisfactory operation has also been made for other connections in the pulse generator according to Figure 2 such as has been described with reference to Figure 6 at the instant t_{10} for the flip-flop J with $K(J) = Q_1(E2)$ (delay time $2t_q$) and $T(J) = Q_2(D2)$ (no delay time).

20 The description of the periods 18 and 19 corresponds to that of the periods 2 and 1, respectively, so that further description is unnecessary.

In the pulse series generated by the flip-flops P and W of Figure 2 the line synchronizing pulse in one series occurs *inter alia* in the signal s_{HP} of Figure 3 and the line blanking pulse in the other series occurs in the signal s_{HW} of Figure 3.

25 The front porch is the time difference between the instants when the leading edges of the pulses occur in the signals s_{HW} and s_{HP} , that is to say, between $t_s + 2t_q$ and $t_s + 2t_q$ which is a time difference of $2 \times 0.8 \mu s = 1.6 \mu s$.

30 It is found that pulse series can be generated with the pulse generator according to Figures 1 and 2 which series include pulses of different duration and having a determined time difference between the series which satisfy the limits given in Table 4 for the CCIR standard.

35 In Figure 1 the phase discriminator B is shown for synchronizing the clock pulse generator A at the line frequency. The 5-to-1 dividers and the 125-to-1 dividers L and M

may be synchronized at the field frequency by the external field synchronizing signal s_{VES} if this is present. In Figure 2, a synchronizing circuit is shown in detail for the signal s_{VES} which will be described in combination with the signals given in Figure 4.

40 The external field synchronizing signal s_{VES} is applied through an isolating capacitor C_6 and a resistor R_9 in series to the base electrode of an npn-transistor T_2 , which base electrode is connected through a resistor R_{10} to the potential U. The base electrode of a second npn-transistor T_3 is connected to the collector electrode of the transistor T_2 while the two emitter electrodes are connected to ground. The collector electrode of transistor T_2 is directly connected to the S_2 inputs of the flip-flops L1...L3, M3...M7 and is indirectly connected through the diode T_1 to the inputs of the flip-flops M1 and M2. The collector electrode of transistor T_2 is connected to ground through a capacitor C_7 and to the output of a NAND gate N_3 through a resistor R_{11} . The inputs of the gate

45 N_3 receive the signals $m1$ and y so that the output conveys a potential corresponding to the signal z of Figure 4.

50 Starting from the assumption that the supply for the synchronizing circuit (T_2 , T_3) is provided through the gate N_3 and that the signal s_{VES} is absent or that no synchronizing pulse occurs in the signal s_{VES} , the transistor T_2 is conducting. Approximately ground potential is impressed on the base electrode of the transistor T_3 so that transistor T_3 is cut off. The S_2 inputs of the flip-flops L1...L3, M1...M7 convey the logic 1 due to internal couplings and due to the resistor R_2 being connected to potential U.

55 If in the presence of the supply through the gate N_3 a negatively directed edge of a synchronizing pulse occurs in the signal s_{VES} , the transistor T_2 is cut off while transistor T_3 becomes conducting so that ground potential occurs at its collector electrode. As a result a pulse going from the logic 1 to the logic 0 occurs at the S_2 inputs of the flip-flops L1...L3, M1...M7. The result is that all Q_1 outputs of the flip-flops L1...L3, M1...M7 should convey the logic 0. A consideration of the signal s_{VES} in relation to the signals $l1...l3$, $m1...m7$ of Figure 4 leads to the conclusion that the negatively directed resetting edge in the signal s_{VES} can only occur between the instants t_{13a} and t_{13b} without exerting influence, which corresponds to the synchronized state. If the resetting edge occurs in the signal s_{VES} beyond the instants t_{13a} and t_{13b} , the circuit of frequency dividers including the flip-flops L1...L3, M1...M7 is brought into the said synchronized state. The time difference between the instants t_{13a} and t_{13b} corresponds to a half line period

within which synchronisation is ensured by the phase discriminator B of Figure 1.

The supply for the transistor T_2 through the gate N_3 whereby the signal x of Figure 4 is impressed on the collector electrode results in the supply dropping out during the period between the instants t_{130} and t_{140} in the synchronized state of the circuit of frequency dividers including flip-flops $L1 \dots L3$, $M1 \dots M7$. The transistor T_2 of Figure 2 then remains cut off, even when the resetting edge occurs in the signal s_{VBS} . It has been achieved that in the synchronized state the then superfluous signal s_{VBS} does not result in needless switching on the S_2 inputs of the flip-flops $L1 \dots L3$, $M1 \dots M7$ and through the resistor R_2 on potential U.

In a practical embodiment the pulse generator of Figure 2, the components were formed as follows:

Dual JK flip-flops of the type FCJ 121 for the combinations: D1—D2, D3—E1, E2—E3, F—I, L1—L2, L3—W, M1—M2, M3—M4, M5—M6, X—Y, M7 $\frac{1}{2}$ FCJ 121.

A JK flip-flop of the type FCJ 201 for P.

A quadruple NAND gate of the type FCH 191 for the gates Z, N_1 , N_2 and N_3 .

A diode BAX 13 for T_1 .

Two transistors BSY 39 for T_2 and T_3 .

A potential U of +6V.

$R_1, R_4, R_7 = 2.2 \text{ k } \Omega$

$R_2, R_5, R_8 = 3.9 \text{ k } \Omega$

$R_3, R_6 = 1 \text{ k } \Omega$

$R_9 = 330 \text{ k } \Omega$

$R_{10} = 10 \text{ k } \Omega$

$R_{11} = 4.7 \text{ k } \Omega$

$C_1, C_5, C_6 = 1 \text{ nF.}$

$C_2, C_3 = 2.2 \text{ nF.}$

$C_4 = 4.7 \text{ nF.}$

$C_7 = 10 \text{ nF.}$

In the combination of the flip-flops X and Y it is noted that the S_2 input which is common for both flip-flops influences with the signal x' the action of Y but not the action of the flip-flop X, which may be derived from Figure 5.

It will be evident that the invention is not restricted to the embodiment of a pulse generator suitable for the CCIR standard and shown in Figures 1 and 2. The H.C.F. of the pulse periods in and the time differences between the synchronizing and blanking signals in relation to a half line period may be determined for any other television standard. The connections for the generator I of the auxiliary pulses of line frequency and double line frequency may be chosen in a simple manner dependent on the desired pulse period with its keying influence.

Figure 10 shows a PAL chrominance sub-carrier gating signal generator formed with five JK flip-flops denoted by the references

FF_1 to FF_5 . Arrow heads are shown for some of the T, J, K and S_2 inputs of the flip-flops $FF_1 \dots FF_5$ on which a trigger action is performed. For some inputs of the flip-flops $FF_1 \dots FF_5$ signals are shown which occur in the pulse generator which is shown in detail in a block-schematic diagram in Figures 1 and 2. These signals are derived from the circuits of frequency dividers (D, E, F or L, M) dividing to the line or field frequency, the pulse generators I and Y and the clock pulse generator A. The time relation between the different signals follows from the time diagrams given in Figures 3 to 7. The flip-flops FF_1 and FF_2 of Figure 10 will be described in combination with the signals shown in Figure 11 after the commencing instant t_0 of a line period T_H . As indicated in Figure 11, the starting point in this case is the state at which the S_2 input of the flip-flop FF_1 has the logic 1 ($S_2 = 1$).

The signal $\bar{i}$ is applied through a capacitor C_8 to the J-input of the flip-flop FF_1 coupled to ground through a resistor R_{12} . The capacitor C_8 and the resistor R_{12} constitute a differentiating circuit whose action follows from

the signal $J = \bar{i}'$ shown in Figure 11. The connected K input which is not shown has the logic 1 ($K = 1$) due to internal couplings. The T input of the flip-flop FF_1 receives the signal $d1$.

With the aid of Table 1 regarding the action of a JK flip-flop, the signal Q_2 of Figure 11 follows at the output Q_2 (FF_1). For $J = 0$ and $K = 1$ it follows that $Q_2 = 1$ provides the stable state of the flip-flop FF_1 . A negatively directed edge in the signal

$J = \bar{i}'$ at the instant t_3 does not have any influence, the logic 0 remains present. After the instant t_{13} a positively directed edge occurs at a propagation delay time of $1t_q$ in the

signal $J = \bar{i}'$. The logic 1 occurs in the signal

$J = \bar{i}'$ until after the instant t_{15} when the signal $T = d1$ has an edge $0 \rightarrow 1$. At the instant t_{16} , with an edge $1 \rightarrow 0$ in the signal $T = d1$, there consequently applies that $J = K = 1$ so that the flip-flop FF_1 must change over. (Table 1). At the instant $t_{16} + 1t_q$ the signal Q_2 has the logic 0. In the signal $T = d1$ a subsequent negatively directed edge occurs at the instant t_{18} for which applies that $K = 1$ and $J = 0$ or 1. It follows from Table 1 in both cases that the flip-flop FF_1 changes

over again. The signal $J = \bar{i}'$ is accompanied by the tolerance within which the trailing edge of the positively directed pulse should be located, namely from and including the

instant t_{15} up to before the instant t_{20} . Negatively directed edges in the signal $T=d1$ occurring after the instant t_{20} therefore do not exert influence on the flip-flop FF_1 . A pulse having the logic 1 appears at the Q_2 output of the flip-flop FF_1 between instants $t_{16}+1t_0$ and $t_{18}+1t_0$.

The Q_2 output of flip-flop FF_1 is connected to the S_2 input of the flip-flop FF_2 . The input $T(FF_2)$ receives the signal a . The K input is connected to ground and the J input is floating so that $K=0$, $J=1$. For $J=1$, $K=0$ it follows from Table 1 that $Q_1=1$ and $Q_2=0$ is the stable state of the flip-flop FF_2 before the signal Q_2 of flip-flop FF_1 exerts a trigger action at the instant $t_{16}+1t_0$ on the input $S_2(FF_2)$. As a result the output $Q_1(FF_2)$ obtains the logic 0 at the instant $t_{16}+2t_0$. During the pulse in the signal Q_2 of the flip-flop FF_1 the signal $T=a$ does not exert influence on the flip-flop FF_2 , but the first occurring negatively directed edge at the instant $t_{16}-1t_0$ causes the flip-flop FF_2 to change over to the stable state. The output $Q_1(FF_2)$ therefore conveys a signal having a pulse ranging from the instant $t_{16}+2t_0$ to t_{18} which is indicated by means of signal $Q_1=s_{00}$ in Figure 11.

The signal s_{00} generated by means of the flip-flops FF_1 and FF_2 has a duration of $(t_{18}-t_{16})-2t_0=3 \times 0.8 \mu s - 2 \times 70 \text{ ns} = 2.26 \mu s$. The leading edge at the instant $t_{16}+2t_0$ is located $7 \times 0.8 \mu s = 5.6 \mu s$ later relative to the leading edge of the line synchronizing pulse s_{RP} shown in Figure 3 (occurring at the instant t_0+2t_0). The signal s_{00} is therefore the chrominance subcarrier gating signal described in the PAL standard which must start $5.6 \mu s$ after the leading edge of the line synchronizing pulse and has a duration of 10 periods of the chrominance subcarrier signal at a frequency of 4,433,618.75 Hz being $2.26 \mu s$. The PAL gating signal s_{00} generated by the flip-flops FF_1 and FF_2 may be applied to a gating circuit (not shown) another input of which may be connected to a chrominance subcarrier oscillator.

Without further steps a gating signal generator including only the flip-flops FF_1 and FF_2 would generate a gating pulse for each line period T_H in the signal s_{00} . However, the PAL standard stipulates that the gating pulse must not occur over a duration of nine line periods around the equalizing and field synchronizing period. The instants during which the beginning and ending of this blocking duration occur is different for successive fields and has a cycle of four field periods. This cycle will become clearly apparent from the following description. The action of the flip-flops FF_1 and FF_2 may be blocked by applying the required blocking pulse with the logic 0 to the S_2 input of the flip-flop FF_1 . During the pulse duration (logic 0) of the

blocking signal indicated by a signal s_0 at the input $S_2(FF_1)$ the output $Q_2(FF_1)$ maintains the logic 1 as well as $Q_1(FF_2)$.

The PAL blocking signal s_0 is generated at the Q_1 output of the flip-flop FF_3 . The flip-flop FF_3 is of the type using multiple formed command J and K inputs. The inputs J_1 and K_1 receive the signals y and z , respectively of Figure 4. The J_2 and J_3 inputs of the flip-flop FF_3 are connected to the Q_2 outputs of the flip-flops FF_4 and FF_5 , respectively. The K_1 and K_2 inputs of the flip-flop FF_3 are connected to the Q_1 outputs of the flip-flops FF_4 and FF_5 , respectively. The flip-flops FF_4 and FF_5 serve for generating auxiliary pulses for the flip-flop FF_3 and all three flip-flops combined constitute a blocking signal generator (FF_3 , FF_4 , FF_5). The interconnected J and K inputs

of the flip-flop FF_4 receive the signal f and the T input receiver the signal i . The input $T(FF_5)$ receives the signal $m1$. The input $J(FF_5)$ is connected to ground through a resistor R_{13} and receives the signal $m7$ ($m7'$) through a capacitor C_9 , which signal is differentiated.

In Figure 12 the signals are shown for the flip-flop FF_4 around the commencement of an equalizing and field synchronizing period. This is apparent from a comparison of the signal $T=i$ with the signals of Figure 7, particularly of Figure 7c. For the signal

$J=K=f$ with the logic 1 it follows from Table 1 that the negatively directed edge in the signal $T=i$ which is active as a trigger edge at the periodically occurring instants t_{13} causes the flip-flop FF_4 to change over. An

edge $1 \rightarrow 0$ in the signal $T=i$ when $J=K=f$ has the logic 0 has no influence as is shown in Figure 12 at the instant t_{63} . The signal

$J=K=f$ has a keying function while the signal $T=i$ gives exactly the instants of the edges. The flip-flop FF_4 which is active as an auxiliary pulse generator generates an auxiliary signal $Q_1=f_4$ shown in Figure 12, which signal is a blocking signal of half the line frequency.

In Figure 12 the signals for the flip-flop FF_5 are shown after the instant of commencement t_{100} of a field period T_V . The

signals $Tm1$ and $J=m7'$ follow from Figure 4. At the instant t_{100} a positively directed edge $0 \rightarrow 1$ occurs in the signal $T=m1$. Subsequently, an edge $0 \rightarrow 1$ occurs at a time difference of $6t_0$ in the signal $J=m7'$. As

has been described with reference to the flip-flop X in Figure 5 for $K(X)=m'$ the result is that due to the negatively directed edge $1 \rightarrow 0$ in the signal $T=m1$ at the instant t_{110} the flip-flop FF_s changes over because $J=K=1$. After the instant t_{110} there applies that $J=0$ and $K=1$ so that the next edge $1 \rightarrow 0$ causes the flip-flop FF_s to change over to its stable state at the instant t_{130} in the signal $t=m1$. The flip-flop FF_s generates a signal $Q_1=ff_s$ which shows a pulse at the field frequency between the instants t_{110} and t_{130} (+1t propagation delay time).

The operation of the flip-flop FF_s follows from the time diagrams of Figure 13. In Figure 13 the beginning of a field period T_V is shown from the instant t_{100} during fourteen line periods T_H . For the signal

$K_s=12$ a few periodically occurring instants $t_0 \dots t_{30} = t_0 \dots t_{40} \dots$ etc of the line frequency time scale are shown. A delay time of $4t_0$ relative to this time scale is not shown but the delay of $2t_0$ of the edges in the signal $K_s=ff_s$ is shown relative to that in the

signal $K_s=12$. In the signals $J_1=y$ and $J_s=ff_s$ the edges of the pulses occurring at the field frequency are also shown.

For the 625-line standard employing interlacing there applies that a field period T_V corresponds to 312.5 line periods T_H . The

signal $K_s=12$ has a period of $2.5 T_H$ so that in each field period

$$T_V = \frac{312.5}{2.5} = 125$$

periods of the signal $K_s=12$ occur. In Figure 12 the auxiliary signal $Q_1=ff_s$ is shown for the flip-flop FF_s as a blocking signal having a period which is equal to two line periods T_H . In a field period

$$T_V = \frac{312.5}{2} = 156.25$$

periods of the signal ff_s consequently occur so that the signal ff_s exhibits a phase shift in a cycle of four field periods T_V . In

Figure 13 the signals $K_1=ff_s$ and $J_s=ff_s$ are shown in a cycle of four field periods T_V by means of V_1, V_2, V_3 and V_4 . Calculated on the time scale determined at the signal

$K_s=12$ the edges in the signals $K_1=ff_s$ and

$J_s=ff_s$ are found to occur at the instants t_{53} and t_{13} in successive fields V_1, V_2 etc.

The signal $Q_1=ff_s$ of Figure 12 corresponds to the signal $K_1=ff_s$ of the flip-flop FF_s for the field V_2 .

The signals at the multiple J and K inputs of the flip-flop FF_s are combined through an AND gate function to form a signal J and a signal K, the fields V_1, V_2, V_3, V_4 being indicated. It is found from the signal K that the signal $K_s=ff_s$ has a keying function while the edges in the signal K are determined

by the signals $K_1=ff_s$ and $K_s=12$. The same applies to the signal J with the signal

$J_1=y$ and the signals $J_2=ff_s$ and $J_s=ff_s$.

The T input (not shown) of the flip-flop FF_s is not connected and conveys a logic 1. For the operation of the flip-flop FF_s Table 5 applies with reference to the action of a JK flip-flop having command J and K inputs for $T=1$.

It is found that prior to the instant t_{110} there applies for all fields $V_1 \dots V_4$ that $K=0$ and that J varies between 1 and 0. A stable state $Q_1=1$ (Table 5) is associated therewith such as is shown for the signal $Q_1=s_0$ with fields V_1, V_2, V_3 and V_4 . After the instant t_{110} pulses appear in the signal K up till the instant t_{130} while the signal J has the logic 0. For $J=0$ and $K=1 \rightarrow 0$ there follows that Q_1 must start to convey the logic 0. The first occurring edge $1 \rightarrow 0$ in the signal K is supplied for the fields V_1, V_2 and V_3 by the signal $K_1=ff_s$ (t_{53}, t_{13}) and is supplied for the field V_4

by the signal $K_s=12$ (t_0).

Up till the instant t_{150} (signal $J_1=y$) the signal J maintains the logic 0. After the instant t_{150} J pulses appear in the signal. For $K=0$ and $J=1 \rightarrow 0$ there follows that Q_1 must convey the logic 1 so that the first occurring edges $1 \rightarrow 0$ cause the flip-flop FF_s to change over. All these trigger edges are

supplied by the signal $J_s=ff_s$ with fields V_1, V_2, V_3 and V_4 and instants t_{13} and t_{53} .

It is found that the signal $Q_1=s_0$ conveys a pulse having a duration of $9 T_H$ in the fields V_1, V_2 and V_3 and of $9.16 T_H$ in the field V_4 . This difference of $0.16 T_H$ caused by $(t_{13}-t_0)$ has no detrimental influence on the signal path in a PAL colour television system and may therefore be allowed. The instant of commencement varies in a cycle of 4 fields in a manner as stipulated in the PAL standard for blocking over 9 line periods the series of chrominance subcarrier periods to be transmitted for burst purposes. The flip-flop FF_s in Figure 10 applies the PAL blocking signal s_0 to the S_2 input of the flip-flop FF_1 so that it must convey the

logic 1 at the Q_2 output during the period $9 T_H$ from an instant t_{13} , for, for example, the field V2. As a result no gating pulse ($t_{16} \dots t_{19}$) will occur in the signal $Q_1 = s_{co}$ of Figure 11 after this instant t_{13} in connection with the predominance of the signal at the S_2 input of the flip-flop FF_1 .

The gating signal s_{co} generated by the PAL chrominance subcarrier gating signal generator ($FF_1 \dots FF_6$) must have edges which are determined as accurately as possible. To this end it is favourable to take trigger signals for the flip-flops FF_1 and FF_2 at the highest possible frequency. Starting from the signal a provided by the clock pulse generator A as a trigger signal $T=a$ for a flip-flop FF_2 , the signal $d1$ directly derived from the signal a is taken for the flip-flop FF_1 so that for the gating pulse in the signal $Q1 = s_{co}$ a most accurately determined duration of 3 clock pulse periods minus 2 propagation delay times of the JK flip-flops FF_1 and FF_2 follows.

A practical embodiment of the PAL chrominance subcarrier gating signal generator according to the invention shown in Figure 10 is as follows.

$$\begin{aligned} FF_1, FF_2, FF_3, FF_4 &= \frac{1}{2} \text{ FCJ } 131 \\ FF_5 &= \text{FCJ } 201 \\ C_1, C_2 &= 2.2 \text{ nF.} \\ R_{12}, R_{13} &= 1 \text{ k } \Omega \end{aligned}$$

In the pulse generator according to Figures 14 and 15 the greater part of the components shown is denoted in a similar manner as in Figures 1 and 2. The block schematic diagram according to Figure 14 will be described in combination with the detailed circuit diagram according to Figure 15. In Figure 14 the direction of the signal transmission in a general sense is denoted by a single arrow head; signal paths having a considerable trigger action on generators still to be described are provided with double arrow heads.

An output of a clock pulse generator A in Figure 14 provides a signal a at a frequency of $80 \nu_H$ to a circuit of frequency dividers D, E and F11. The frequency F11 provides a signal $f11$ of the frequency ν_H to a phase discriminator B to which also an external synchronizing signal of the frequency ν_H is applied, while an output signal thereof synchronizes the clock pulse generator A. For the CCIR standard ν_H is the line frequency of 15,625 Hz and for the RTMA standard for colour and monochrome television ν_H is equal to 15,734.265 Hz. Dependent on the external synchronizing signal applied to the discriminator B for the CCIR or RTMA standard, the generator A is synchronized. When, as is shown in Figure 15 for the sake of simplicity, there is no external synchronisation, the generator A provided with two outputs may supply the signal a at the frequency of $80 \nu_H$ for the RTMA or CCIR standard at

an output indicated by R or C. The standard may be chosen by means of a selector switch not further shown. In Figures 14 and 15 more selector switches having an R and a C position are shown and on and off-switches R and C are shown. Since Figures 14 and 15 will be described in the first instance for the RTMA standard, the switches which are mutually coupled mechanically or in a different manner are shown in the position R applying to this standard. Further Figures, which provide signals occurring particularly in the RTMA or CCIR position of the pulse generator or are of importance are likewise denoted by R or C.

The frequency dividers D and E of Figure 14 are together active as a 40-to-1 divider which is built up from a 3-to-1 divider D and a 14-to-1 divider E from which the 40-to-1 divider is obtained by means of feedback. For the positions R and C a different switchable feedback is realized. As is shown in greater detail in Figure 15, the 3-to-1 divider D consists of two divider stages D11 and D12 and the 14-to-1 divider E consists of four divider stages E11, E12, E13 and E14. Each divider stage is formed as a JK flip-flop. For the RTMA standard the stage or flip-flop E13 is fed back to D11 and for the CCIR standard E14 is fed back to D12.

An output of the divider E conveying a signal $e14$ at double the line frequency is connected to a circuit of frequency dividers L and M operating to divide by 21 for the divider L for the RTMA standard, or by 25 for the CCIR standard and a fixed division of 25 for the divider M. For the RTMA standard employing $21 \times 25 = 525$ interlaced lines the frequency divider M provides a signal of the field frequency ν_v . For synchronisation purposes an external synchronizing signal s_{ves} is applied to the dividers L and M.

The divider L is built up from a 3-to-1 divider, a 2-to-1 divider and a 5-to-1 divider together including six divider stages which are denoted by means of JK flip-flops L11 ... L16 in Figure 15. The 21-to-1 divider is obtained by feed back from flip-flop L16 to the flip-flops L13 and L14, so that the 3-to-1 divider is combined with a 7-to-1 divider. The 25-to-1 divider is obtained by feed back from flip-flop L13 to L11 so that two 5-to-1 dividers are combined. The divider M consists of an 8-to-1 divider and a 3-to-1 divider consisting of five flip-flops M11 ... M15, the flip-flop M11 being switches in a particular manner and receiving at a blocking input an auxiliary pulse y of field frequency for realizing the 25-to-1 divider.

Outputs of the circuit of frequency dividers L and M are connected to pulse generators X, Y, Z and ZZ which provide signals x , y , z and zz or inverse values thereof (for example $\bar{zz}$). The signals x , y and z are already given

for the CCIR standard and in that case they include pulses occurring at the field frequency at a pulse duration of $20 T_H$, $7.5 T_H$ and $2.5 T_H$, respectively, in which T_H is the line period in the CCIR standard. It will be apparent that the additional signal zz in the CCIR standard also has a $2.5 T_H$ pulse of field frequency which, however, occurs at an earlier instant in a field period T_V than the pulse in the signal z . The pulse generator ZZ is of importance for generating the PAL gating signal and is also used for generating the signals x and y .

For the RTMA standard the pulse generators X , Y , Z and ZZ provide signals x , y , z and zz having pulses occurring at the field frequency at a pulse duration of $20 T_H$, $9 T_H$, $3 T_H$ and $1.5 T_H$, in which T_H is the line period in the RTMA standard. These signals are shown *inter alia* in Figure 18.

The pulse generators Y , Z and ZZ are controlled by the frequency dividers L and M without the interposition of change-over switches; in the generator X two coupled change-over switches having positions R and C are required.

A synchronizing signal generator P and a blanking signal generator W receive the signals y and z and the signal x respectively, while they are both connected to outputs of the circuit of frequency dividers D and E . The generator according to Figures 14 and 15 is provided with a pulse generator $I1$ controlled by the circuit D , E , $F11$, which

generator applies a signal $i1$ and/or $\bar{i}1$ to the generator P and W which exhibits auxiliary pulses occurring at the line frequency beyond the equalizing and field synchronizing period of $9 T_H$ (RTMA) or $7.5 T_H$ (CCIR) determined by the signal y , while the auxiliary pulses occur at the double line frequency within this period.

Prior to describing the signal path in the

pulse generator switched on according to Figures 14 and 15 for the RTMA standard with the aid of Figures 17 to 23, the requirements which are imposed on the blanking and synchronizing signals according to the RTMA standard will be described first with the aid of Figure 16.

Unlike the CCIR standard the steepness of the pulse edges are taken into account for the RTMA standard. The steepness of the edges must be smaller than or may be equal to $0.004 T_H$ at most. In practice a steepness of the edge of $0.002 T_H$ occurs generally. The pulse periods are then given between points on the edges which are located at 10% and 90% of the signal amplitude. For the sake of simplicity of Figure 16 the 0 and 100% values are taken in this case. Starting from infinitely steep edges shown in solid lines during and around the line blanking period, Figure 16 shows the possible steep edges by means of broken lines. The times laid down in the RTMA standard are shown by solid distance lines, while the chain-link distance lines indicate the times obtained in practice with the aid of the generator. The instants which are laid down in the generator and are also shown in Figures 17 are denoted by means of crosses.

For the RTMA standard there applies a field synchronizing period $3 T_H$ (signal z), an equalizing and field synchronizing period of $9 T_H$ (signal y) and a field blanking period of approximately $20 T_H$ (signal x). In this case it has been prescribed that 6 equalizing pulses of the double line frequency must precede and follow 6 field synchronizing pulses of the double line frequency. The duration of the field blanking period in the composite blanking signal must then be $20 T_H \pm 1 T_H + 1$ line blanking pulse duration. Furthermore the requirements imposed in the following Table 6, which requirements are derived from the signals shown in Figures 16 and 17, apply.

TABLE 6
(Figures 16,17)

RTMA-standard (colour)

1. Line blanking pulse duration, signal s_{HW} : $0.18 T_H$.
2. Front porch: $\geq 0.02 T_H$.
3. Line synchronizing pulse duration, signal s_{HP} : $0.075 \pm 0.005 T_H$.
4. Back porch to chrominance subcarrier gating signal $\geq 0.006 T_H$.
5. Chrominance subcarrier gating signal (burst gate), signal s_{CB} : ≥ 8 periods of chrominance subcarrier = $0.0352 T_H$.
6. Synchronizing pulse up to and including gating signal: $\leq 0.125 T_H$.
7. Synchronizing pulse up to and including blanking pulse: $\geq 0.145 T_H$.
8. Raster serration duration, signal s_{VS} : $0.07 \pm 0.01 T_H$.
9. Equalizing pulse duration/line synchronizing pulse duration: 0.45 to 0.50 T_H .

The following are applicable to the above table:

Chrominance subcarrier frequency:

$$5 \quad 3579545 \pm 10 \text{ Hz.}$$

Line frequency ν_H :

$$\frac{2}{455} \cdot 3579545 = 15734.265 \dots \text{ Hz.}$$

Line period T_H :

$$63.55 \dots \mu\text{s.}$$

- 10 Starting from the method of finding the Highest Common Factor H.C.F. for the determined pulse periods and the smallest pulse repetition period of $\frac{1}{2} T_H$, a lowest clock pulse frequency of 80 ν_H is found to be satisfactory

also for the RTMA standard. The clock pulse generator A then has a frequency of 12588441.2 Hz and a period of $0.79446 \mu\text{s} \approx 795 \text{ ns}$.

With reference to Figures 16 and 17 in which a time scale of line frequency $t_0, t_1, \dots$ $t_{80} \approx t_0, t_1, \dots$ derived from the clock pulse periods in the signal α is shown, in which t_0 indicates in accordance with the Handbooks the propagation delay time t_{PA} occurring in the JK flip-flops of Figure 15, a Table 7 is given. In this case a clock pulse period is equal to

$$\frac{T_H}{80} = 0.0125 T_H$$

and a number thereof is given while t_0 is rounded off to $0.001 T_H$ (63.5 ns) and the maximum steepness of the edges of $0.004 T_H$ is taken.

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TABLE 7

	RTMA-standard	In practice	Edge steepness
1 s_{HW}	$\leq 0.18 T_H$	$14 \times 0.0125 = 0.175 T_H$	$+0.004 T_H$
2 Front porch	$\geq 0.02 T_H$	$2 \times 0.0125 = 0.025 T_H$	$-0.004 T_H$
3 s_{HP}	$0.075 \pm 0.005 T_H$	$6 \times 0.0125 - 0.001 = 0.074 T_H$	$+0.004 T_H$
4 Back porch to gating signal	$\geq 0.006 T_H$	$1 \times 0.0125 - 0.001 = 0.0115 T_H$	$\frac{0.004}{2} T_H$
5 s_{CR}	≥ 8 periods	$3 \times 0.0125 = 0.0375 \times \frac{455}{2} = 8.5$ per.	
6 Sync. to gating signal incl.	$\leq 0.125 T_H$	$10 \times 0.0125 - 0.002 = 0.123 T_H$	$+\frac{0.004}{2} T_H$
7 Sync. to blanking signal incl.	$\geq 0.145 T_H$	$12 \times 0.0125 = 0.15 T_H$	
8 s_{VS}	$0.07 \pm 0.01 T_H$	$6 \times 0.0125 = 0.075 T_H$	$-0.004 T_H$
9 equal./sync.	0.45 ± 0.50	$\frac{3 \times 0.0125 - 0.001}{6 \times 0.0125 - 0.001} = 0.494$	

It is found that even with the maximum steepness of the edges all requirements are still satisfied, with the value of the synchronizing pulse and the synchronizing pulse up to and including the gating signal reaching the allowed limit value as mentioned under items 3 and 6 of Table 7. For the edge steepness of $0.002 T_H$ occurring in practice the requirements imposed are amply satisfied.

In a manner analogous to that of Figure 3, Figure 17 shows as a function of time a few signals having a logic 0 and 1 during one line period T_H which signals are associated with the generator according to Figure 15 in the RTMA position. The signals a , d_{11} , d_{12} , e_{11} , e_{12} , e_{13} , e_{14} and f_{11} follow with the aid of the description of Table 1 for the operation of a JK flip-flop in a simple manner from the circuit diagram according to Figure 15 with:

$$T(D_{11}) = T(D_{12}) = A$$

$$K(D_{11}) = Q_1(D_{12}) \quad K(D_{12}) = Q_2(D_{11})$$

$$T(E_{11}) = T(E_{12}) = T(E_{13}) = Q_2(D_{12})$$

$$J(E_{11}) = Q_1(E_{12})$$

$$K(E_{11}) = J(E_{12}) = Q_2(E_{13}) \quad K(E_{12}) = T(E_{14}) = Q_1(E_{11})$$

$$K(E_{13}) = Q_2(E_{12}) \quad J(E_{13}) = Q_2(E_{11}) \cdot Q_2(E_{12})$$

$$J(E_{14}) = K(E_{14}) = Q_1(E_{13})$$

$$T(F_{11}) = Q_2(E_{14})$$

In the RTMA position $S_2(D_{11})$ receives the signal e_{13}' because $Q_2(E_{13})$ is connected through a capacitor C_{10} and a resistor R_{14} to ground to an input of a NAND gate N_4 , a further input of which is free and conveys a logic 1 due to internal couplings, while the output is connected to the reset input S_2 of the flip-flop D_{11} . If the free arranged input of the gate N_4 had been connected through a switch to ground with the logic 0, the output would convey a logic 1 independent of

the signal e_{13}' applied to the other input; the gate N_4 would then be blocked.

The line frequency time scale $t_0 \dots t_{40} \dots t_{80} = t_0 \dots$ shown in Figure 17 is calculated on the edges in the signals d_{11} and d_{12} . The

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edges in the signal a therefore occur $1t_Q$ earlier, while successive JK flip-flops each introduce an additional propagation delay time $1t_Q$.

- 5 When considering the 40-to-1 divider D, E over half a line period $T_H/2$ it is found that negatively directed edges occur in the signal $e13$ at two instants $t_{10} + 1t_Q$ and $t_{30} + 1t_Q$ (or $t_{50} + 1t_Q$ and $t_{70} + 1t_Q$) which are active in the signal $e13'$ at the reset input $S_2(D11)$. The result is that at these instants the divider D and the subsequent divider E go one pulse further, that is to say, they count one more pulse so that the circuit of dividers D, E
- 10 adapts a cycle of 40 pulses instead of having its own cycle of 42 pulses without feedback.

- 15 Due to a pulse edge displacement obtained the certain choice of the feedback is of importance for generating the trailing edge of the line blanking pulse in the signal s_{HW} at the instant $t_{21} + 2t_Q$. As is shown in Figures 14 and 15, edges may occur in the signal $e11$ as trigger edges for the blanking signal generator of flip-flop W. As will be apparent from the
- 20 description of Figure 22 these are the edges at the instants $t_i + 2t_Q$ and $t_{21} + 2t_Q$, the latter being obtained by the special feedback. Without the previously occurring feedback and the pulse edge displacement, the edge would have occurred at the instant $t_{22} + 2t_Q$ (as is necessary for the CCIR standard and as is apparent from Figure 3).

- Figure 17 shows a few signals described with reference to Figures 16 and Table 7 in a time relationship with the circuit of dividers D, E, F11 dividing to the line frequency. In addition to the signal s_{HW} the line synchronizing pulse occurring at the line frequency from $t_9 + 2t_Q$ to $t_{15} + 1t_Q$ in the signal s_{HP} and the chrominance subcarrier gating pulse occurring from t_{16} to t_{19} are shown in the signal s_{CR} . For generating the signal s_{CR} the pulse generator shown in Figures 14 and 15 is to be provided with an additional pulse generator which is shown in Figure 24 and which will be further described hereinafter.

- Furthermore Figure 17 shows pulses occurring at the double line frequency, namely the equalizing pulse from $t_9 + 2t_Q$ to $t_{12} + 1t_Q$ in the signal s_{EP} and the raster serration from $t_8 + 2t_Q$ to $t_9 + 2t_Q$ in the signal s_{VS} . Outside the equalizing and field synchronizing period of $9 T_H$ the signal $i1$ has a pulse occurring at the line frequency from $t_8 + 1t_Q$ to $t_9 + 1t_Q$ and a pulse occurring at double the line frequency within this period from $t_{28} + 1t_Q$ to $t_{29} + 1t_Q$. As compared with the auxiliary pulse in the signal i described with reference to Figure 3, the pulse in the signal $i1$ has been
- 50 chosen to be shorter so that, as will be apparent from the description of Figure 23, this pulse directly provides the raster serrations in the signal s_{VS} .

- The signal $e14$ of the circuit of dividers D, E is applied to the circuit L, M. In the

signal $e14$ negatively directed edges which are active as trigger edges for the divider L occur at the instants $t_1 + 2t_Q$ and $t_{41} + 2t_Q$ of each line period T_H .

Apart from connections of the reset input S_2 , the circuit diagram for the JK flip-flops L11 L16 in the divider L is as follows:

$$T(L11) = T(L12) = Q_1(E14)$$

$$K(L11) = Q_2(L12) \quad J(L12) = Q_2(L11)$$

$$T(L13) = Q_1(L12)$$

$$T(L14) = T(L15) = Q_2(L13)$$

$$K(L14) = Q_2(L15) \quad J(L14) = Q_2(L16)$$

$$T(L16) = Q_1(L15) \quad J(L15) = Q_2(L14)$$

In the RTMA standard $S_2(L13)$ and

$S_2(L14)$ receive the signal $i16'$ through feedback because $Q_1(L16)$ is connected through a capacitor C_{11} and a resistor R_{15} to ground to an input of a NAND gate N_5 another input of which is free and conveys a logic 1 due to internal couplings, while the output is connected to the reset inputs S_2 of the flip-flops L13 and L14.

The inputs $S_2(L13)$ and $S_2(L14)$ are additionally connected to the anode of a diode T_4 , while $S_2(L11)$ and $S_2(L12)$ are connected to the anode of a diode T_5 whose interconnected cathodes are connected to $S_2(L15)$ and $S_2(L16)$. The diode T_4 (and T_5 for the CCIR position to be described) blocks the negatively directed pulse obtained by the feedback so that it acts only on the inputs $S_2(L13)$ and $S_2(L14)$.

The divider M following the divider L has the following connection diagram:

$$T(M11) = Q_1(L14)$$

$$J_1(M11) = Q_2(L16) \text{ and } J_2(M11) = Q_1(Y)$$

$$T(M12) = Q_1(M11) \quad T(M13) = Q_1(M12)$$

$$T(M14) = T(M15) = Q_1(M13)$$

$$J(M14) = Q_2(M15) \quad J(M15) = Q_1(M14)$$

All reset inputs S_2 are interconnected and are connected to $S_2(L15)$ and $S_2(L16)$ and to the collector electrode of an npn -transistor T_3 whose emitter electrode is connected to ground.

Transistor T_3 forms part of an external synchronizing circuit which is formed in the same manner as the circuit described with reference to Figure 2, so that a further description thereof is not necessary. Normally the transistor T_3 is cut off during synchronization and the logic

1 is impressed on all the said S_2 inputs due to internal couplings.

In Figure 18 the passage of the signals is shown on two time scales through the circuit of frequency dividers L, M dividing to the field frequency and the signals zz , x , y , z and s_{VES} are shown for giving the time relation.

The signal $e14$ has a trigger edge at each line period T_H at the instants $t_1 + 2t_Q$ and $t_{41} + 2t_Q$ from which the signals $l11 \dots l16$ follow.

In Figure 4 a time scale t_{100} etc. of field frequency is introduced which has been derived from pulse edges having a propagation delay time of $5t_Q$ and, as seen in one line period, commencing at the instant $t_0 = t_{100}$ at which $t_{20} = t_{101}$, $t_{40} = t_{102}$, $t_{60} = t_{103}$, $t_{80} = t_{104}$ etc. up to $t_{180} = t_{100}$. In Figure 18 a time scale of field frequency is introduced in a similar manner, but a time index notation has been used only to emphasize that, as seen in one line period, the scale begins at t_1 under the influence of the signal $e14$. The instant t_{100}' of a field period T_V is the instant t_1 of a line period T_H in which t_{104}' is one line period later, etc. up to $t_{1150}' = t_{100}'$ for the end of a field period T_V in the RTMA standard employing 262.5 lines per field.

In the signal $l16$ some edges are denoted by way of arrow heads which influence the signals $l13$ and $l14$ directly through the signal $l16'$ (not shown) on the inputs $S_2(L13)$ and $S_2(L14)$.

The divider M controlled by signal $l14$, which divider is formed with the 8-to-1 divider M11, M12, M13 and 3-to-1 divider M14, M15 is active as a 25-to-1 divider due to

the signal $J(M11) = y.l16$. It has been achieved with this signal combination that the input $J(M11)$ between the instants t_{116}' and t_{152}' ($y=0$) has and maintains the logic 0. The flip-flop M11 will therefore not change over when at t_{152}' a negatively directed edge occurs in the signal $l14$. The input $J(M11)$ serves as a blocking input for the divider M so that an increase in the divisor is achieved. One pulse is skipped, as it were, in the signal $l14$ during counting, that is to say, the divider M is stopped during one pulse so that the counter or the divider M has a cycle of $8 \times 3 + 1 = 25$ pulses.

As has been explained in the description of the external synchronizing signal s_{VES} with reference to Figure 2, the negatively directed trigger edge in the signal s_{VES} in the synchronized state of the pulse generator can only occur around the instant t_{137}' (from t_{136}' to t_{138}') because then only all signals $l11 \dots l16$, $m11 \dots m15$ have the logic 0. If they were actually not synchronised, the dividers L and M would be forced to take up this state.

Figure 19 serves for illustrating the manner

in which flip-flop ZZ, Y, Z and X of Figure 15 are active.

The connection diagram of the flip-flop ZZ follows from Figure 15

$$T(ZZ) = Q_2(L15) \quad J(ZZ) = 1, \quad K(ZZ) = 0$$

and $S_2(ZZ)$ is connected to $Q_1(M15)$ through a differentiating circuit which includes two resistors R_{16} and R_{17} arranged in series between ground and potential U, and a capacitor C_{12} .

It follows from Table 1 regarding the action of a JK flip-flop in general that for $J=1$ and $K=0$ the flip-flop ZZ in the stable state conveys the logic 1 at the Q_1 output and conveys the logic 0 at the inverse Q_2 output. The stable state means that a negatively directed edge at the T-input which edge may be active as a trigger does not change over the flip-flop. As in the generator according

to Figures 14 and 15 only the signal $Q_2 = \bar{zz}$ is used, this signal is shown in Figure 19.

At the instant t_{100}' the flip-flop ZZ is in its stable state with the logic 0 in the signal

$Q_2 = \bar{zz}$. It follows from Figure 18 that at the instant $t_{110}' + 4t_Q$ a negatively directed edge occurs in the signal $m15$ which, while occurring in the signal $S_2 = m15'$ causes the flipflop ZZ, to change over. The signal $Q_2 =$

$\bar{zz}$ has obtained the logic 1 at the instant $t_{110}' + 5t_Q$. Since the condition $J=1$, $K=0$ has not changed, the result is that the next negatively directed edge (t_{116}') in the signal

$T = l15$ causes the flip-flop ZZ to change back again. At the instant $t_{116}' + 1t_Q$ the logic

0 is present again in the signal $Q_2 = \bar{zz}$, which 0 is maintained until the next field period with a new cycle. A signal zz has been generated with a pulse lasting 1.5 line periods T_H and occurring after 2.5 line periods T_H from the commencement of a field period T_V .

The connection diagram for the flip-flop Y is: $T(Y) = Q_2(L16)$, $J(Y) = 1$, $K(Y) = 0$ and $S_2(Y)$ connected to $Q_2(ZZ)$ through a differentiating circuit which includes two resistors R_{18} and R_{19} arranged in series between ground and potential U, and a capacitor C_{13} .

The same stable state as described for the flip-flop ZZ applies to the flip-flop Y with $J=1$ and $K=0$ so that the signal $Q_1 = y$ has the logic 1 at the instant t_{100}' . After the

instant t_{110}' the signal $S_2 = \bar{zz}'$ has a positively directed edge and at the instant $t_{116}' + 1t_Q$ it has a negatively directed edge to the logic 0 so that the flip-flop Y changes over. From the instant $t_{116}' + 2t_Q$ until the instant of occurrence of the next negatively directed edge ($t_{132}' + 1t_Q$) in the signal $T = l16$ the

signal $Q_1=y$ maintains the logic 0. In the signal $Q_1=y$ a pulse appears from $t_{116}+2t_Q$ to $t_{152}'+2t_Q$ which pulse thus lasts

$$\frac{152-116}{4}$$

$$=9 \text{ line periods } T_H$$

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5 and commences a 4 line periods T_H after the commencement of a field period T_V .

The generator Z in Figure 15 is formed as a NAND gate whose inputs are connected to $Q_2(Y)$ and $Q_2(L15)$. The output of the

10 gate Z therefore conveys a signal $z=\bar{y} \cdot \bar{l15}=y+l15$. The signal z has a pulse lasting three line periods T_H which is desired as is shown in Figure 18, and which pulse lasts from t_{128}' to t_{140}' but has an unwanted additional pulse in Figure 19, but as will be apparent this additional pulse is harmless for the action of the pulse generator. Since a negatively directed edge occurs in the signal $l15$ at the instant t_{152}' , while in the signal y the positively directed edges does not occur until the instant $t_{152}'+2t_Q$, a narrow pulse of $2t_Q$ (for example, of 140 ns) appears in the signal z .

20 The generator X in Figure 14 is formed with switchable inputs to which end NAND gates are connected to the flip-flop X in Figure 15. Two inputs of two NAND gates N_6 and N_7 are interconnected which are free for the position R, but are connected to ground through a change-over switch in the position C. In the position R the gates N_6 and N_7 provide the signals $l11$ and $m11$ to the inputs $T(X)$ and $J(X)$, respectively.

25 For the position R the effective connection diagram of the flip-flop X, in which the inverting action of the gates N_6 and N_7 is taken into account would be:

$$T(X)=Q_1(L11), J(X)=Q_1(M11), K(X)=0$$

and $S_2(X)$ connected to $Q_2(ZZ)$ through the differentiating circuit (R_{18} , R_{19} and C_{18}).

40 Since in the signal $J=m11$ of Figure 19 the logic 1 occurs until the instant t_{110}' and $K=0$, the signal $Q_1=x$ in the stable state of the flip-flop X has the logic 1 before this instant. The logic 0 appearing in the signal $J=m11$ does not give the negatively directed edges in the signal $T=l11$ any opportunity to change over the flip-flop X because for $J=0$ and $K=0$ the flip-flop X is never changed over through signals on the T-input. At the instant $t_{116}'+1t_Q$ the flip-flop X changes over under the influence of the negatively directed

55 pulse in the signal $S_2=zz'$. As long as the signal $J=m11$ maintains the logic 0, the flip-flop X in the signal $Q_1=x$ also maintains the logic 0. In the signal $J=m11$ the logic 1 occurs at the instant $t_{144}'+2t_Q$ so that the edge in the signal $T=l11$ occurring at the

instant $t_{196}'-2t_Q$ is active as a trigger edge so as to bring the flip-flop X in the stable state associated with $J=1$ and $K=0$. A signal x is generated with a pulse of 20 line periods T_H and occurring from $t_{116}'+2t_Q$ until $t_{196}'-1t_Q$.

For the flip-flop I1 in Figure 15 there applies that:

$$T(I1)=Q_2(D11), K(I1)=Q_2(E12), J_1(I1)$$

is connected to $Q_2(E14)$ through a differentiating circuit including a resistor R_{20} to ground and a capacitor C_{14} , and $J_2(I1)$ connected to the output of a NAND gate N_8 whose inputs are connected to $Q_1(F11)$ and $Q_1(Y)$.

In Figure 20 the signals $T=\bar{d}11$, $J_1=\bar{e}14'$, $J_2=\bar{f}11 \cdot y=\bar{f}11+\bar{y}$ and $K=\bar{e}12$ are shown for the flip-flop I1. These signals are comparable with those given in Figure 6 because the action of the flip-flop I1 is in principle not different, even if a different signal choice has been made. A considerable difference is, however, that in the signal $Q_1=i1$ the pulses are shorter than in the case of the pulse generator according to Figures 1 and 2 which is of importance for the signals present at the synchronizing signal generator P.

Since the pulses in the signal $i1$ have the same number of clock pulses of the signal a , in the RTMA and CCIR standards, which clock pulses are, however, of different duration the R-notation in Figure 20 has been omitted.

Briefly, the following applies to the signals in Figure 20:

During each line period T_H the signal $J_1=\bar{e}14'$ has two pulses with the logic 1 obtained by differentiation, the first pulse occurring from t_1+2t_Q to t_2 at a minimum and t_{11} at a maximum and the second pulse occurring from $t_{41}+2t_Q$, etc. Beyond the equalizing and field synchronizing period with $y=1$, the

signal $\bar{f}11$ in the signal $J_2=\bar{f}11+y$ only has the logic 1 during the first pulse so that only

this first pulse in the signal $J_1=\bar{e}14'$ provides the logic 1 at the input $J(I1)$. For $J=0$ and

$K=0$ or 1, caused by the signal $K=\bar{e}12$, the stable state of the flip-flop I1 is that the Q_1 output conveys the logic 0 as is shown at the instant t_0 .

After the logic 1 has appeared at the input

$J(I1)$ in the signal $J_1=\bar{e}14'$ at t_1+2t_Q the next negatively directed edge in the signal

$T=\bar{d}11$ causes the flip-flop I1 to change over

at t_3 . A subsequent negatively directed edge in the signal $T=\bar{d}11$ at the instant t_4 does not have any influence because for $K=0$ and $J=1$ or 0 the Q_1 output conveys the logic 1 in the stable state. Before the edge in the signal $T=\bar{d}11$ at t_4 , the condition $K=1$ is

given by the signal $K=\bar{e}12$ while $J=1$ or 0 . For $K=1$ and $J=1$ a change-over is effected at each trigger edge while for $K=1$ and $J=0$ there applies for the stable state that the Q_1 output must convey the logic 0. In both cases a change-over of the flip-flop 11 is effected and a pulse is thus generated in the signal

$Q_1=\bar{i}1$ between the instants t_3+1t_0 and t_4+1t_0 .

During the equalizing and field synchronizing period with $y=0$ during $9 T_H$ both

pulses in the signal $J_1=\bar{e}14'$ become manifest at the input $J(11)$ and a pulse between the instants $t_{43}+1t_0$ and $t_{49}+1t_0$ is generated during the second half of one line period T_H

in the signal $Q_1=\bar{i}1$.

For the sake of simplicity of Figure 20 the pulses produced by differentiation in the sig-

nal $J_1=\bar{e}14'$ at the instants t_{21} and t_{61} which continue to represent the logic 0 and do not exert any influence on the flip-flop 11 are only shown incompletely in broken lines.

Figure 21 serves for illustrating the operation of the flipflop 11 at and near the equalizing and field synchronizing period of $9 T_H$ for the RTMA standard. Figure 21a shows the signal y in relation to the field time scale $t_{100}, \dots, t_{1150}$ given in Figure 18. Figures 21b and 21c apply to two successive fields in which Figure 21b applies to the field ending in a full line and Figure 21c applies to the field ending in a half line. The signals

$f11, J_2=\bar{f}11+y, J_1=\bar{e}14'$ (without the superfluous negatively directed pulses) and $Q_1=\bar{i}1$ are shown for both fields. Figures 21b and 21c are selfevident, certainly after what has been described with reference to Figure 7.

Starting from the definition for a so-called first field for which there applies that the last occurring line synchronizing pulse occurs over an integral number of line periods, before the commencement of the field synchronizing period. Figure 21b is associated with the first field in accordance with the RTMA standard, while Figure 7b is associated with the first field in accordance with the CCIR standard.

The operation of the blanking signal generator or flip-flop W of Figure 15 is illustrated by way of Figure 22 in which Figure 22a shows the signals which are the same for each

field and Figures 22b and 22c shows signals which are different for successive fields.

For the connection diagram of the flip-flop W in Figure 15 active as a blanking signal generator there applies that

$$T(W)=Q_1(E11), K(W)=Q_1(I1),$$

$$J_1(W)=Q_1(E13) \text{ and } J_2(W)=Q_1(X).$$

In Figure 22a the signal $T=\bar{e}11$ is shown on two scales, negatively directed edges occurring with a delay of $1t_0$ after the instants $t_{13}, t_{73}, t_{213}, t_{413}, t_{473}$ and t_{613} . For the J input a signal J follows from the signals $J_1=\bar{e}13$ also having a delay time of $1t_0$ and $J_2=x$ at an instant $t_{41}+7t_0$ for the leading edge and $t_{41}+4t_0$ for the trailing edge of the pulse lasting $20 T_H$.

The signal $K=\bar{i}1$ in Figures 22b and 22c follows from Figures 21b and 21c with the signal $Q_1=\bar{i}1$. Since there is a shift of half a line period T_H between Figures 22b and 22c a few instants are shown in these Figures in which $t_{02}, \dots$ in one Figure corresponds to $t_{402}, \dots$ in the other.

For the flip-flop W there applies that for $K=0$ and $J=1$ or 0 the Q_1 output conveys the logic 1 in the stable state as may be derived from Table 1. When considering Figure 22c it is found that a pulse with the logic 1 occurs in the signal $K=\bar{i}1$ between the instants t_3 and t_9 while a negatively directed edge occurs at the instant t_7 in the signal $T=\bar{e}11$, which edge is active as a trigger edge. The signal $Q_1=w$ has obtained the logic 0 at the instant t_7+2t_0 . At the instant t_{13} the signal $T=\bar{e}11$ obtains the logic 1 while the logic 0 then occurs in the signal $K=\bar{i}1$ and the logic 1 occurs in the signal J. Associated therewith is a stable state with the logic 1 in the signal $Q_1=w$. Although under the influence of the signal $\bar{e}13$ of Figure 17 the logic 0 appears in the signal J at the instant t_{13} , the logic 1 information is maintained in the flip-flop W so that the negatively directed edge in the signal $T=\bar{e}11$ causes the flip-flop W to change over at the instant t_{21} . This mechanism is denoted by means of a dot in the signal J. The result is that a line blanking pulse denoted by s_{HW} appears in the signal $Q_1=w$ which pulse appears between t_7+2t_0 and $t_{21}+2t_0$, that is to say, a duration of 14 clock pulse periods of the signal a , hence $14 \times 0.0125 = 0.175 T_H$.

For Figure 22b there applies that the signal $K=\bar{i}1$ approximately determines the position of the leading edge in the same manner and the signal $J_1=\bar{e}13$ determines the position of the trailing edge, while the edges of the line blanking pulses s_{HW} are exactly determined by the signal $T=\bar{e}11$.

In Figures 22b and 22c the first pulse in the signal $K=\bar{i}1$ occurring after the signal $J_2=x$ in the signal J has given the logic 0 causes the flip-flop W to change over at the instant t_7 or t_{47} . Subsequently, the logic 0 in the signal J is maintained during approxi-

mately 20 line periods T_H . During the first 9 line periods T_H with $y=0$ pulses of double line frequency occur in the signal $K=i1$ and during the rest of the time with $y=1$ pulses of line frequency occur only so that $K=1$ or 0. For $J=0$ and $K=1$ or 0 the flip-flop W is in the stable state with the signal $Q_1=w$ conveying the logic 0.

At the end of the 20 line periods T_H the next pulse with the logic 1 in the signal $J_1=e13$ becomes manifest in the signal J. Due to the condition $J=1$ and $K=0$ the next negatively directed edge in the signal $T=e11$ occurring at the instant t_{e1} (Figure 22a) causes the flip-flop W to change over. The flip-flop W thus generates a field blanking pulse in Figure 22b lasts from t_1+2t_0 to $t_{e1}+2t_0$ and in Figure 22c from $t_{e1}+2t_0$ to $t_{e1}+2t_0$ plus 20 full line periods T_H . The field blanking pulse thus lasts 20 line periods T_H and 14 clock pulse periods of the signal a , that is to say, one line blanking period (s_{HW}).

Subsequently, the auxiliary pulses in the signal $K=i1$ of Figures 22b and 22c provide the opportunity for the negatively directed edges in the signal $T=e11$ of Figure 22a to generate the line blanking pulses s_{HW} by means of the flip-flop W, while these edges are active as trigger edges.

For the connection diagram of the flip-flop P of Figure 15 active as a synchronizing signal generator there applies that: $T(P)=Q_2D(11)$, $J_3(P)=Q_1(E13)$, $K=0$, $S_1(P)=Q_2(11)$, $S_2(P)$ connected to $Q_1(11)$ through a differentiating circuit having two resistors R_{21} and R_{22} arranged in series between ground and the potential U , and a capacitor C_{15} ; $J_2(P)$ connected to the output of a NAND gate N_5 to inputs of which $Q_2(E11)$ and $Q_1(Y)$ are connected, and $J_1(P)$ connected to the output of the NAND gate Z.

For the input S_1 of the JK flip-flop P there applies that for $S_1=0$, Q_1 must be 1. As already noted there applies for the reset input S_2 that for $S_2=0$, Q_1 must be 0.

Figure 23 shows that the signals for the flip-flop P and relates to 22 half line periods $T_H/2$ occurring during and near the equalizing and field synchronizing period. The periods of time 1, 2, 3; 8, 9, 10; 14, 15, 16 and 20, 21, 22 are shown for the numbered half line periods. Due to the repetitive nature of the signals in the half line periods, the time scale $t_0 \dots t_{40}$ is taken for each half line period $T_H/2$.

Since there applies for the flip-flop P that $K=0$, the signal J is of importance so as to enable the negatively directed edges in the

signal $T=d11$ to be active as trigger edges. For $K=0$ and $J=0$ there applies that the

signal $T=d11$ can never make the flip-flop P change over. If $J=1$ when $K=0$, there applies that $Q_1=1$ for the stable state of the flip-

flop P; if this state is not present, a change-over to this state is effected.

The signal J in Figure 23 causes the flip-flop P to generate other pulses in the synchronizing signal $Q_1=p$ during the field synchronizing period, the equalizing period and the period beyond these intended for the line synchronisation. The signal $J_1=z$ provides the logic 0 during the field synchronizing period of 3 T_H in the signal J so that the edges in the

signal $T=d11$ do not exert any influence. The

signal $J_2=e11+y$ together with $y=1$ cause the signal $J_3=e13$ to become manifest in the signal J during the equalizing and field synchronizing period of 9 T_H . Outside the period of 9 T_H a combination of the signals $e11$ (of

the signal $J_2=e11+y$ with $y=0$) and $J_3=e13$ becomes manifest in the signal J, the leading edges of the pulses in the signal J being determined by $e11$ (t_{18} relative to t_{10}).

The signals $S_1=i1$ and $S_2=i1'$ and the signal $Q_1=p$ derived therefrom are partly shown in solid, broken and chain-link lines so as to indicate periodically the results of the two television fields in one Figure. In Figures 21 and 22 the Figures 21b, 21c and 22b, 22c are given for this purpose. When a pulse denoted by chain-link lines occurs in the sig-

nal $S_1=i1$ as corresponds to Figures 21b and 22b during the period of time 1 of Figure 23 as well as in the signal $S_2=i1'$, the following is effected: starting from the stable state of the flip-flop P with $Q_1=1$ for the condition that $K=0$ and $J=1$ or 0, the pulse with the logic 0 occurring from t_8+1t_0 to t_9+1t_0

in the signal $S_1=i1$ will not cause the flip-flop P to change over because Q_1 is 1 already.

After the instant t_9 a pulse with the logic 0 obtained by differentiation occurs in the signal $S_2=i1'$ for which there applies that $Q_1=0$; the flip-flop P changes over and the logic 0 appears in the signal $Q_1=p$. The next nega-

tively directed edge in the signal $T=d11$ occurs at the instant t_{12} . The signal J has the logic 0 at the instant t_{12} under the influence

of the signal $e11$ in $J_2=e11+y$. Since the condition $K=0$ and $J=0$ applies, the flip-flop P cannot be changed over by the signal

$T=d11$. In the signal J a logic 1 occurs due to the signal $e11$ at the instant $t_{18}+1t_0$. A second negatively directed edge in the signal

$T=d11$ at the instant t_{18} causes the flip-flop P to change over to the stable state with $Q_1=1$ in case of the condition $J=1$ and $K=0$.

The same description applies to the period

of time 2 for the pulses shown in broken lines and associated with the signals of Figures 21c and 22c.

5 The result is that in the signal $Q_1=P$ line synchronizing pulses s_{EP} are generated which last from t_9+2t_Q to $t_{15}+1t_Q$, that is to say, $6 \times 0.0125 T_H - 0.001 T_H = 0.074 T_H$ as already given with reference to Figures 16 and 17 and Table 7.

10 During the period of time 1 a time variation δt has been given for the signals $S_1=i1$ and $S_2=i1'$ between the instant t_0 and the exact instant of occurrence of the negatively directed edge in the signal $S_2=i1'$ while the positively directed edge occurs in the signal

15 $S_1=i1$ within the time variation δt . Up till now the propagation delay time t_Q has been given to correspond with a propagation delay time t_{pd} of a JK flip-flop. There are flip-flops which have a difference in propagation delay time between an input and the two outputs Q for a positively or negatively directed edge occurring. The time t_{pd} is then distinguished in t_{pdr} (rise propagation delay time) and t_{pdt} (fall propagation delay time) in which t_{pdr} is generally smaller than t_{pdt} . The positively directed edge then commences at an earlier instant than the negatively directed edge which has, however, a steeper slope and which reaches the final value at a quicker rate than the positively directed edge, but relative to a measuring reference potential of 1.5 V the positively directed edge having a more gentle slope reaches this final value earlier than the negatively directed edge. For a JK flip-flop I1 of the type FCJ 121 the practical measurement was that $t_{pdr}=50$ ns and $t_{pdt}=70$ ns $=\delta t$ in Figure 23. The difference of 20 ns guarantees that the signals $S_1=i1$

40 $i1$ and $S_2=i1'$ having an opposite action at the instant t_0 do not yield any uncertainty for the flip-flop P, while this effect will be used in a positive manner in the field synchronizing period of $3 T_H$.

45 During the periods of time 3 8 the signal $J_3=e13$ becomes completely manifest in the signal J because the logic 1 is present

50 in both signals $J_1=z$ and $J_2=e11+y$. During the period of time 3 a short pulse of $1t_Q$ having the logic 0 occurs in the signal $J_2=e11+y$ because the negatively directed edge in the signal $e11$ occurs at t_1+1t_Q and the positively directed edge in the signal y occurs at t_1+2t_Q ; this pulse does not appear in the signal J.

55 When commencing with the period of time 3, the signal $S_2=i1'$ causes the flip-flop P to change over as has been described with refer-

ence to the period of time 1. Since a positively directed edge given by the signal $J_3=e13$ occurs in the signal J, at the instant $t_{10}+1t_Q$, the next negatively directed edge

in the signal $T=d11$ causes the flip-flop P to change over at t_{12} . In this manner an equalizing pulse is generated in the signal $Q_1=p$ in each of the periods of time 3 8, which equalizing pulse is denoted by s_{EP} . The equalizing pulses s_{EP} last from t_9+2t_Q to $t_{12}+1t_Q$ (Figure 17), that is to say, $3 \times 0.0125 T_H - 0.001 T_H = 0.0365 T_H$. Thus the calculation given in Table 7 under item 9 is satisfied by the six generated equalizing pulses s_{EP} .

During the periods of time 9 14 the signal $J_1=z$ with the logic 0 passes on this logic 0 to the signal J. For the condition $K=0$ and $J=0$ none of the negatively

directed edges in the signal $T=d11$ can be active as a trigger edge. The flip-flop P changes over at the instant t_0 under the influence of the signal $S_2=i1'$. During the remaining part of each of the periods of time 9 14 the signal $Q_1=p$ maintains the logic 0. At the instant t_0 in a next period of time, for example, period of time 10 relative to period of time 9, the negatively directed edge of the pulse with the logic 0 occurs in

the signal $S_1=i1$ so that the Q_1 output of P must convey the logic 1. The subsequent pulse with the logic 0 in the signal $S_2=i1'$ at the instant t_0 causes the flip-flop P to convey the logic 0 again at the Q_1 output.

The result is that the signals $S_1=i1$ and $S_2=i1'$ provide the raster serrations s_{VS} in the signal $Q_1=p$ from t_8+2t_Q to t_9+2t_Q (Figure 17) so that six field synchronizing pulses denoted by s_{VP} appear in the field synchronizing period of $3 T_H$. The raster serrations s_{VS} have a duration of six clock pulse periods, that is to say, they are $6 \times 0.0125 T_H = 0.0075 T_H$.

When generating the raster serrations s_{VS} and the field synchronizing pulses s_{VP} use was made of the property already mentioned that at the instant t_0 the positively directed edge

in the signal $S_1=i1$ at an earlier instant (approximately 20 ns) than the negatively directed edge in the signal $S_2=i1'$ so that at this instant t_0 there is no uncertainty about the state of the flip-flop P. To this end the flip-flop I1 is formed as an FCJ 121 having different propagation delay times from the pulse edges to the inverse outputs.

During the periods of time 15 20 six equalizing pulses are generated in the signal $Q_1=p$ in an analogous manner as described with reference to the periods of time 3 8.

The following applies for the transition between the periods of time 14 and 15. The signal $J_1=z$ maintains the logic 0 until the instant t_1 in the period of time 15. However, there is a requirement for the logic 0 in the signal J to be maintained until shortly after the instant t_0 . Due to the choice of the signal $J_3=e13$ with the logic 0 from $t_{10}+1t_0$ in the period of time 14 to $t_{10}+1t_0$ in the period of time 15 it is ensured that this requirement is satisfied.

The periods of time 21 and 22 correspond to the periods of time 1 and 2. For the period of time 21 in particular there applies that the short pulse of $2t_0$ described with reference to Figure 19, occurs in the signal $J_1=z$ after the instant t_1 . It is found that this impulse has no influence on the signal J .

In Figure 18 it is indicated that relative to Figure 4, the field time scale is one clock pulse period of the signal a later ($0.795 \mu s$). It is found that this does not make any difference for the generated pulses of line frequency and double line frequency, and the difference is negligibly small relative to the pulses occurring at the field frequency.

It is found that the pulse generator according to Figures 14 and 15 in the RTMA position generates some of the signals shown in Figures 16 and 17 and in Table 7, the front porch following from the time difference between the leading edges of the pulses $s_{BW}(t_r+2t_0)$ and $s_{HF}(t_0+2t_0)$.

For generating the NTSC chrominance subcarrier gating signal (burst gate) s_{OR} , Figure 24 shows in detail a generator which can be connected to the pulse generator according to Figures 14 and 15, which generator includes in principle one flip-flop FF_{16} . The other flip-flops shown in Figure 24 are required for generating a PAL-chrominance subcarrier gating signal s_{OC} . Figure 25 shows the signals associated with the flip-flop FF_{16} .

In Figure 24 the flip-flop FF_{16} receives the signal a at the T input, the signal $d12$ at the K input and the signal y at the S_2 input. The J input is connected to the collector electrode of an *npn*-transistor T_6 which is connected through a resistor R_{28} to a terminal of potential U. The emitter electrode of transistor T_6 is connected to ground and the base electrode is connected through a resistor R_{24} to the potential U and through a capacitor C_{16} to a terminal to which the

synchronizing signal p is applied. The transistor T_6 is normally conducting with $J=0$ applying for the flip-flop FF_{16} . A positively directed edge in the signal p does not influence the transistor T_6 , a negatively directed edge of a pulse renders the transistor T_6

instantaneously non-conducting for a duration which is determined by the time constant of the resistor R_{24} and the capacitor C_{16} which act as a differentiating circuit.

Figure 25 shows a signal p derived from Fig. 23 which provides the possibly occurring pulses over one line period T_H . Solid lines denote a line synchronizing pulse s_{HP} , thick broken lines denote two equalizing pulses s_{BP} and thin broken lines partially show two field synchronizing pulses s_{VP} . Negatively

directed edges in the signal p applied to transistor T_6 , which edges correspond to positively directed edges in signal p provide a

pulse having the logic 1 in the signal $J=p'$ to the J input of FF_{16} . Starting from the fact that the flip-flop FF_{16} was in its stable state at the instant t_0 in case of the condition $J=0$ and $K=1$ or 0, the Q_1 output conveys the logic 0 as is shown in the signal $Q_1=s_{OR}$. Since no gating signals must be generated during the equalizing and field synchronizing period of $9 T_H$ with $y=0$, the signal y is applied to the input S_2 (FF_{16}). In Figure 25 the signal $S_2=y$ is denoted by a solid (1) and a broken line (0) and it follows that for $y=0$ the predominant S_2 input maintains the output Q_1 at the logic 0 irrespective of what occurs at the T, J and K inputs.

Outside the equalizing and field synchronizing period, flip-flop FF_{16} may be changed over, because a pulse caused by the trailing edge of the pulse s_{HP} appears with the logic

1 at the instant $t_{15}+1t_0$ in the signal $J=p'$ while a negatively directed edge in the signal $T=a$ occurs at the instant $t_{16}-1t_0$. In this case K may be 0 or 1. The signal $Q_1=s_{OR}$ has the logic 1 at the instant t_{16} .

In the signal $K=d12$ the reference K_R denotes the signal which occurs in case of the RTMA standard. At the instants $t_{17}-1t_0$ and $t_{18}-1t_0$ having negatively directed edges in the signal $T=a$, $K=0$ so that for $J=1$ or 0 the Q_1 output maintains the logic 1.

At the instant t_{18} K_R in the signal $K=d12$ obtains the logic 1 so that the edge in the signal $T=a$ at the instant $t_{19}-1t_0$ may be active as a trigger edge for the condition $K=1$, $J=1$ or 0. At the instant t_{19} the logic 0 has appeared in signal $Q_1=s_{OR}$. After the instant t_{19} the logic 0 is to occur in the signal

$J=p'$ in order that the flip-flop FF_{16} does not change over again.

It is found that the flip-flop FF_{16} generates the chrominance subcarrier gate signal (burst gate) s_{OR} already shown in Figures 16 and 17 from the instant t_{18} to t_{19} , that is to say, at a duration of three clock pulse periods

of the signal a , being $3 \times 0.0125 T_H = 0.0375 T_H$. This corresponds to

$$\frac{455}{2} \cdot 0.0375 = 8.5 \text{ periods}$$

of the chrominance subcarrier.

The times given in Table 7 and shown in Figure 16 are self-evident.

So far the switchable pulse generator shown in Figures 14 to 15 has only been described as one acting for the RTMA standard. To achieve that the switchable generator according to Figures 14 and 15 can also be active for the CCIR standard, three switching operations are carried out as follows:

1. The flip-flop D11 in Figure 15 receives a logic 1 at the S_2 input because an input of the NAND gate N_4 is connected to ground with the logic 0; the gate N_4 is blocked.

Subsequently the signal $e14'$ is applied to the reset input S_2 of the flip-flop D12 because $Q_1(E14)$ is connected through a capacitor C_{17} and a resistor R_{25} to ground to an input of a NAND gate N_{10} another input of which is free and conveys a logic 1 due to internal couplings while the output is connected to $S_2(D12)$.

2. The flip-flops L13 and L14 receive the logic 1 at the S_2 input through the NAND gate N_5 with an input connected to ground with the logic 0. The signal $i13'$ is applied to the reset input S_2 of the flip-flop L11 because $Q_1(L13)$ is connected through a capacitor C_{18} and a resistor R_{26} to ground to an input of a NAND gate N_{11} another input of which is free and the output of which is connected to $S_2(L11)$.

3. The T and J inputs of the flip-flop X are switched over. To this end an input of the gates N_6 and N_7 is connected through a change-over switch to ground with the logic 0, position C, so that two other NAND gates N_{12} and N_{18} are released. Gate N_{12} having an input connected to $Q_1(L16)$ has its output connected to T(X) and gate N_{18} having an input connected to $Q_2(Y)$ has its output connected to J(X).

Although the output of the gate N_{11} is connected to both $S_2(L11)$ and $S_2(L12)$, the flip-flop L11 only is influenced by the feedback. The reason for the interconnection of $S_2(L11)$ and $S_2(L12)$ is that the flip-flops L11 and L12 can in practice be formed as one dual flip-flop FCJ 121 having one interconnected input S_2 .

To explain the simple switchability of the pulse generator according to Figure 15 and to illustrate a few important signal differences occurring between the R and C positions, a

few signals are partially plotted in Figure 26, which signals are associated with the frequency dividers D, E, F11 and L, and in Figure 27 associated with the generators ZZ, Y, Z and X. Figures 26 and 27 correspond for the position C to Figures 17, 18 and 19 for the position R.

The clock pulse period of the signal a of the 80-fold line frequency v_H is 800 ns in Figure 26. Until the instant t_{13} when the feedback is effected with the signal $e13'$ in Figure 17 for the position R, the signals $d11$, $d12$, $e11$, $e12$, $e13$, $e14$ and $f11$ in Figure 26 are identical to those in Figure 17. In this case the difference in the clock pulse period (795 relative to 800 ns) has been left out of consideration as well as in the calculated time scale $t_0 \dots t_{40} \dots t_{80} = t_0$. In the position C the feedback with the signal

$e14'$ in Figure 26 is effected at the instant $t_{22} + 2t_Q$. In the signal $d12$ a pulse having a duration of $3t_Q$ occurs. The result is that the dividers D and E now count two successive pulses more or skip them so that the original 42-to-1 divider becomes a 40-to-1 divider. It is of importance that in the signal $e11$ which may perform a trigger action on the flip-flop W for supplying the line blanking signal ($T(W) = Q_1(E11)$ according to Figure 15) a negatively directed edge active as a trigger edge occurs at the instant $t_{22} + 1t_Q$. This is in contrast with the trigger edge in the signal $T = e11$ at the instant $t_{21} + 1t_Q$ in Figure 22 for the position R. As is evident from Figure 3, a line blanking pulse in the signal s_{HW} is to be generated for the CCIR standard from $t_7 + 2t_Q$ to $t_{22} + 2t_Q$ having a duration of fifteen clock pulse periods, while for both standards the line synchronizing pulse in the signals s_{HP} , the equalizing pulse in the signal s_{RP} and the raster serration in the signal s_{VS} have the same number of clock pulse periods at the same relative instants.

The signal $e14$ with trigger edges at the instants t_1 and t_{41} determines the signal

$i11 \dots i16$ of which the signal $i13'$ provides the feedback to the flip-flop L11. The field frequency time scale calculated thereon is plotted for the signal $i15$ in which, as in Figure 18, the instant of commencement is t_{100}' and in which t_{101}' is one fourth of a line period T_H later etc. until $t_{1360}' = t_{100}'$.

Analogous to Figure 19, the result of the flip-flops ZZ, Y, X and the NAND gate Z is given in Figure 27. Starting from the signals $i15$ and $i16$ and the signal $m15$ of the divider M (Figure 18) shown in Figure 26 in which at the instant t_{110}' a negatively directed edge occurs, there simply follow the signals $Q_2 = zz$, $Q_1 = y$ and z having a pulse

duration of $2.5 T_H$, $7.5 T_H$ and $2.5 T_H$ respectively.

For the flip-flop X with $K=0$ Figure 27 shows the signals $T=\bar{1}16$, $J=y$, $S_2=\bar{z}z'$ and $Q_1=x$. The negatively directed pulse in the signal $S_2=\bar{z}z'$ at the instant t_{120}' causes the flip-flop X which is in the stable state with $Q_1=1$ at the condition $K=0$, $J=0$ or 1, to change over so that at the instant $t_{120}'+2t_Q$ the logic 0 appears in the signal $Q_1=x$. The next negatively directed edge in the signal

$T=\bar{1}16$ occurs at the instant $t_{150}'+1t_Q$ in which for $K=0$ and the logic 0 in the signal $J=y$ the flip-flop X is not changed over. At the instants $t_{150}'+2t_Q$, the logic 1 occurs in the signal $J=y$ so that the next negatively

directed edge in the signal $T=\bar{1}16$ at the instant $t_{200}'+1t_Q$ causes flip-flop X to change over to its stable state with $Q_1=1$ for $K=0$ and $J=1$.

In the CCIR standard the signal $\bar{i}1$, described in Figure 20 with reference to the RTMA standard, is generated in substantially the same manner. In fact, until the

instant t_{10} , the signals $\bar{d}11$, $\bar{e}14'$, $\bar{f}11$ and $\bar{e}12$ are identical in shape for both standards except for the difference in clock pulse period. Beyond the equalizing and field synchronizing period auxiliary pulses of line frequency and of double line frequency occurring there-within during the $7.5 T_H$ period with $y=0$ are generated in the signal $Q_1=\bar{i}1$.

The flip-flop W active as a blanking signal generator operates in the same manner for both standards, the only considerable difference being that a trigger edge occurs in the signal $T=\bar{e}11$ at the instant t_{22} for the CCIR standard instead of at t_{21} for the RTMA standard.

Apart from the different number of various pulses in the line synchronizing signal $Q_1=p$ generated by the flip-flop P, this operates in the same manner for both standards for generating the pulses s_{HP} , s_{EP} , s_{VP} and s_{VB} .

It is found in the pulse generator according to Figures 14 and 15 that there is only a small amount of switching required to make it switchable for use with the RTMA or CCIR standard. The switching of the division of the circuit of frequency dividers L, M dividing to the field frequency is evident. The choice of the clock pulse frequency of the generator A being the same number of times the line frequency in both positions, with the example of $80 v_H$, obviates a switching of the division of the circuit of dividers D, E, F11 dividing to the line frequency. A pulse displacement by switching in the divider D, E is found to be necessary so

as to generate the line blanking pulses s_{HW} of relatively different duration (14 relative to 15 clock pulses). A very simple pulse edge displacement is realized by forming the divider D, E, not as a 40-to-1 divider which is adaptable by means of switching, but in principle as a 42-to-1 divider the division of which is reduced to 40 by means of a switchable feedback while the desired pulse edge displacement is effected at the same time.

Figure 17 shows the NTSC chrominance subcarrier gating signal s_{CB} for the RTMA standard whose generation is described with reference to Figures 24 and 25. For a corresponding PAL chrominance subcarrier gating signal s_{CO} for the CCIR standard, two differences are of importance. In the first place, the instant of commencement and the pulse duration are different, namely for the CCIR standard 5.6μ after the leading edge of the line synchronizing pulse s_{HP} and a duration of 10 periods of the chrominance subcarrier signal at a frequency of 4433618.75 Hz being $2.26 \mu s$. In the line time scale this corresponds to an instant of commencement of t_9+2t_Q (leading edge s_{HP}) plus

$$5.6$$

$$= 7 \text{ clock pulse periods,}$$

$$0.8$$

that is to say, up to $t_{10}+2t_Q$. At a final instant t_{10} , the duration is $(t_{10}-t_{10})-2t_Q=3 \times 0.8 \mu s - 2 \times 70 \text{ ns} = 2.26 \mu s$ is required.

In the second place it is not sufficient, as in the RTMA standard, to discontinue the generation of the gating signal in the equalizing and field synchronizing period, but according to the PAL system a phase-shifted suppression of nine line periods is to be effected in a cycle of four fields. All this has already been described with reference to Figures 10 13.

For the explanation of the operation of the generator shown in Figure 24 for generating the PAL chrominance subcarrier gating signal s_{CO} reference is made to Figures 11, 12 and 13. As regards their operation the flip-flops FF₁₂, FF₁₃ and FF₁₄ shown in Figure 24 correspond to the flip-flops FF₂, FF₆ and FF₄, respectively, of Figure 10, the flip-flop FF₁₆ shown in Figure 24 and described with reference to generating the NTSC gating signal s_{CB} will be used when generating the PAL gating signal s_{CO} . To this end the input T of a flip-flop FF₁₇ is connected to $Q_2(\text{FF}_{16})$. The input J(FF₁₇) is connected to $Q_2(\text{FF}_{16})$. The flip-flops FF₁₃ and FF₁₄ are active as a blocking signal generator for generating a blocking pulse of nine line periods in the signal s_0 occurring phase-shifted in a cycle of four lines, while beyond this period there applies that $Q_1(\text{FF}_{16})=s_0=1$. The signal $\bar{d}12$ of Figure 26 is applied to the input $S_2(\text{FF}_{17})$. The output $Q_2(\text{FF}_{17})$ is connected to $S_2(\text{FF}_{12})$. For the flip-flop

FF₁₂, J=1, K=0 and T(FF₁₂) receives the signal *a* of Figure 26. In the position C of the pulse generator according to Figures 14 and 15, the output Q₁(FF₁₂) conveys the PAL chrominance subcarrier gating signal *s₀₀*.

For the stable state of the flip-flop FF₁₇ with S₂=d12=0 or 1, there applies that Q₂=1. For the stable state of the flip-flop FF₁₂ in which J=1, K=0 and S₂=1, Q₂(FF₁₇)=1 while T=*a* there applies that Q₁=*s₀₀*=1.

In the position C of the pulse generator according to Figures 14 and 15 there apply the signals shown in Figure 25 for the flip-

flop FF₁₆ in which for K=d12 the signal K₀ occurs. Since the signals K_R and K₀ are more or less identical in shape up to the instant *t₂₀*, the flip-flop FF₁₆ generates a signal at the Q₂ output which signal is the inverse of the shown signal Q₁=*s₀₀*. During each line period outside the equalizing and field synchronisation of 7.5 line period T_H a negatively directed edge occurs once at the input T(FF₁₇) at the instant *t₁₈*. At the instant *t₁₈*, S₂=d12=1 and J=K=1 so that the flip-flop FF₁₇ is changed over so that at *t₁₈*+1*t₀* the logic 0 appears at the output Q₂(FF₁₇) with the result that the flip-flop FF₁₂ is also changed over through the connection S₂(FF₁₂)=Q₂(FF₁₇). In the signal *s₀₀* at the output Q₁(FF₁₂) the logic 0 has appeared at the instant *t₁₈*+2*t₀*. A pulse having the logic 0 begins at the input S₂(FF₁₇) in the signal d12 at the instant *t₁₈* so that flip-flop FF₁₇ is changed back and conveys the logic 1 again at the Q₂ output after the instant *t₁₈*+1*t₀*. The next negatively directed edge active as a trigger edge at the input T(FF₁₂) at the instant *t₁₀*-1*t₀* will cause the flip-flop FF₁₂ to change over to the stable state associated with the condi-

tion J=1, K=0. At the instant *t₁₉* the logic 1 has appeared at the output Q₁(FF₁₂). The signal *s₀₀* has a gate pulse from *t₁₆*+2*t₀* to *t₁₉*, as is required.

If a pulse with the logic 0 is generated in the signal *s₀* by the flip-flops FF₁₃ and FF₁₄ and if this pulse is supplied to the input J(FF₁₇), the negatively directed edge will not cause the flip-flop FF₁₇ to change over at the instant *t₁₈* at the T input. For the condition that J=0, K=1 and S₂=0 or 1, the logic 1 is associated with the output Q₂(FF₁₇) in the stable state.

In the flip-flop FF₁₄ the signal *i1* is applied to the T input and the signal *i11* is applied to the interconnected J and K inputs. The operation of the flip-flop FF₁₄ is analogous to that of the flip-flop FF₄ of Figure 10, the signals being given in Figure 12. The flip-flop FF₁₄ generates a square-

wave signal *ff₁₄* and *ff₁₄* at the outputs Q₁ and Q₂ at half the line frequency, in which dependent on the field the edges are located near the instant *t₉* or *t₄₉*, under the influence of the trailing edge of the pulses in the signal *i1*.

The application of the signals at the inputs of the flip-flop FF₁₃ is as follows: J₁ signal *y*,

J₂ signal *ff₁₄*, J₃ signal *i14*, K₁ signal *i13*,

K₂ signal *ff₁₄* and K₃ signal *zz*. The signals

ff₁₄ and *ff₁₄* may be interchanged as has been done in Figure 10 which is changed for the sake of a simpler drawing.

In Figure 13 the signals are given for the flip-flop FF₃ which with small modifications also applies to the flip-flop FF₁₃ of Figure 24. A survey of the modification is as follows:

FF₃
K₁=*ff₄*
Edges at *t₁₃* and *t₃₃*
K₂=*ff₅*
Pulse *t₁₁₀* to *t₁₃₀*
K₃=*i2*
Edges at *t₀* and *t₄₀*
K
Pulses to *t₁₃₀*
J₂=*ff₄*
See K₁
J₃=*ff₅*
Pulse *t₁₁₀* to *t₁₃₀*
J₁=*y*
Pulse *t₁₂₀* to *t₁₅₀*

Q₁=*s₀*

FF₁₃
K₄=*ff₁₄* (or *ff₁₄*)
Edges at *t₉* and *t₄₉*
K₅=*zz*
Pulse *t₁₁₀*' to *t₁₂₀*'
K₁=*i13*
Edges at *t₁* and *t₄₁*
K
No pulses after *t₁₂₀*'
J₂=*ff₁₄* (or *ff₁₄*)
See K₂
J₃=*i14*
Pulse *t₁₁₀*' to *t₁₄₀*'
J₁=*y*
Pulse *t₁₂₀*' to *t₁₅₀*'

3 Fields one $9 T_H$ -pulse from
 t_{1s} or t_{2s} t_0 or t_{1s}

4th Field a longer pulse from
 t_0 to t_{1s} t_1 to t_2

$$5 \quad 9 T_H + \frac{13}{80} T_H = 9.16 T_H \quad 9 T_H + \frac{8}{80} T_H = 9.1 T_H$$

The slightly longer duration of the pulse in the blocking signal s_0 in the fourth field is allowed.

10 The pulse generator shown in Figure 24 or Figure 10 is easily connectable to a known PAL coder. This coder is provided with a so-called PAL switch so as to achieve that the polarity of the (R-Y) vector is changed every other line. It follows from the PAL standard that the position of the PAL switch must be such that the phase of the first formed burst of the chrominance subcarriers after the PAL gating signal s_0 of $9 T_H$ is 135° relative to the $+(B-Y)$ vector. To this end the switch must be driven at half the line frequency. Since in the signal s_0 the gating pulse of $9 T_H$ is determined by the

25 signals ff_{14} and $\overline{ff}_{14}$ of half the line frequency, a uniform relationship between these signals is guaranteed. The signals ff_{14} and $\overline{ff}_{14}$ may be used with this guarantee for switching the PAL switch in a coder.

WHAT WE CLAIM IS:—

30 1. A method of generating a synchronising and/or blanking pulse signal for a television standard which signal has at least one repeating pulse series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, said method comprising generating a clock pulse train whose period is such that each of said different durations and different values is substantially an integral multiple of the clock pulse period, the frequency of said clock pulse train being substantially equal to or an integral multiple of eighty times the line frequency for said television standard, dividing said clock pulse train to produce therefrom frequency divided clock pulse trains, producing generated pulse trains from said divided clock pulse trains, and combining said divided clock pulse trains and said generated pulse trains in such a manner as to produce said synchronising and/or blanking pulse signal.

50 2. A television synchronising and/or blanking pulse generator for generating for a television standard at least one repeating pulse

series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, said television pulse generator comprising a clock pulse generator having a period such that each of said different durations and different values is substantially an integral multiple of the clock pulse period, said clock pulse generator having a frequency which is substantially equal to or an integral multiple of eighty times the line frequency for said television standard, a circuit of frequency dividers connected to said clock pulse generator, pulse generators controlled by said dividers, and a signal generator controlled by said dividers and said pulse generators, and said signal generator being provided with an output which forms an output of said television pulse generator and from which may be derived said repeating pulse series.

3. A television pulse generator as claimed in Claim 2 provided with a second signal generator which is also controlled by said circuit of frequency dividers and said pulse generators, said first mentioned and said second signal generators generating respectively said one and a second differing repeating pulse series which are related in time.

4. A television pulse generator as claimed in Claim 2 or 3, in which said circuit of frequency dividers divides said clock pulses to produce pulses of line frequency, which circuit is also connected to said one or to both of said signal generators to determine the precise timing of at least some of the pulse edges in the synchronising and/or blanking signal.

5. A television pulse generator as claimed in Claim 2 or 3 suitable for use with different television standards each having specified line and field frequencies, said circuit of frequency dividers having a first circuit which divides by a constant divisor to produce pulses of line frequency and a second circuit which divides to produce pulses of field frequency, said second circuit being switchable in divisor to produce pulses of field frequency appropriate to the television standard.

6. A television pulse generator as claimed in Claim 5, in which said first circuit is

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3 Fields one $9 T_H$ -pulse from
 t_{13} or t_{38} t_9 or t_{49}

4th Field a longer pulse from
 t_0 to t_{13} t_1 to t_9

$$5 \quad 9 T_H + \frac{13}{80} T_H = 9.16 T_H \quad 9 T_H + \frac{8}{80} T_H = 9.1 T_H$$

The slightly longer duration of the pulse in the blocking signal s_0 in the fourth field is allowed.

10 The pulse generator shown in Figure 24 or Figure 10 is easily connectable to a known PAL coder. This coder is provided with a so-called PAL switch so as to achieve that the polarity of the (R-Y) vector is changed every other line. It follows from the PAL standard that the position of the PAL switch must be such that the phase of the first formed burst of the chrominance subcarriers after the PAL gating signal s_0 of $9 T_H$ is 135° relative to the + (B-Y) vector. To this end the switch must be driven at half the line frequency. Since in the signal s_0 the gating pulse of $9 T_H$ is determined by the

15 signals ff_{14} and $\overline{ff}_{14}$ of half the line frequency, a uniform relationship between these signals is guaranteed. The signals ff_{14} and $\overline{ff}_{14}$ may be used with this guarantee for switching the PAL switch in a coder.

WHAT WE CLAIM IS:—

30 1. A method of generating a synchronising and/or blanking pulse signal for a television standard which signal has at least one repeating pulse series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, said method comprising generating a clock pulse train whose period is such that each of said different durations and different values is substantially an integral multiple of the clock pulse period, the frequency of said clock pulse train being substantially equal to or an integral multiple of eighty times the line frequency for said television standard, dividing said clock pulse train to produce therefrom frequency divided clock pulse trains, producing generated pulse trains from said divided clock pulse trains, and combining said divided clock pulse trains and said generated pulse trains in such a manner as to produce said synchronising and/or blanking pulse signal.

50 2. A television synchronising and/or blanking pulse generator for generating for a television standard at least one repeating pulse

series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, said television pulse generator comprising a clock pulse generator having a period such that each of said different durations and different values is substantially an integral multiple of the clock pulse period, said clock pulse generator having a frequency which is substantially equal to or an integral multiple of eighty times the line frequency for said television standard, a circuit of frequency dividers connected to said clock pulse generator, pulse generators controlled by said dividers, and a signal generator controlled by said dividers and said pulse generators, and said signal generator being provided with an output which forms an output of said television pulse generator and from which may be derived said repeating pulse series.

3. A television pulse generator as claimed in Claim 2 provided with a second signal generator which is also controlled by said circuit of frequency dividers and said pulse generators, said first mentioned and said second signal generators generating respectively said one and a second differing repeating pulse series which are related in time.

4. A television pulse generator as claimed in Claim 2 or 3, in which said circuit of frequency dividers divides said clock pulses to produce pulses of line frequency, which circuit is also connected to said one or to both of said signal generators to determine the precise timing of at least some of the pulse edges in the synchronising and/or blanking signal.

5. A television pulse generator as claimed in Claim 2 or 3 suitable for use with different television standards each having specified line and field frequencies, said circuit of frequency dividers having a first circuit which divides by a constant divisor to produce pulses of line frequency and a second circuit which divides to produce pulses of field frequency, said second circuit being switchable in divisor to produce pulses of field frequency appropriate to the television standard.

6. A television pulse generator as claimed in Claim 5, in which said first circuit is



switchable between different circuit configurations so as to obtain a displacement of the precisely timed pulse edges controlled thereby for the different television standards.

5 7. A television pulse generator as claimed in Claim 6 in which the divisor of said first circuit would be larger than the ratio between the clock pulse generator frequency and the line frequency save for said first circuit
10 being provided with switchable feedback paths to obtain the correct ratio and the said pulse edge displacement.

8. A pulse generator as claimed in Claim 5, 6 or 7, in which said second circuit which produces pulses of field frequency includes a divider stage having a nominal divisor set by the internal connections of said divider stage, an output of one of said pulse generators controlled by said circuit of frequency
15 dividers being connected to a blocking input of said divider stage to increase the nominal divisor of said divider stage.

9. A television pulse generator as claimed in any of the preceding Claims 2 to 8, in which said circuit of frequency dividers divides to produce pulses of line frequency and of field frequency, said pulses of line and field frequency being applied to an auxiliary pulse generator for producing auxiliary
25 pulses at line frequency and twice line frequency, which auxiliary generator is connected to said signal generator or signal generators for control purposes and to determine the occurrence of at least some of the pulse edges in the synchronising and/or blanking signals.
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10. A television pulse generator as claimed in Claim 9, in which said auxiliary pulse generator is directly connected to said circuit of frequency dividers, and is additionally connected to said circuit of frequency dividers through one of said pulse generators, which pulse generator produces a pulse at field frequency having a period equal to the equalising and field synchronising periods.
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11. A television pulse generator as claimed in any of the preceding Claims 2 to 10 in which said circuit of frequency dividers divides to produce pulses at field frequency and is provided with an input for receiving
40 synchronising signals at field frequency, said clock pulse generator being connected to a phase discriminator which phase discriminator has an input for receiving line frequency synchronising signals for controlling the frequency of said clock pulse generator.
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12. A television pulse generator as claimed in Claim 11, in which the field frequency synchronising input of said circuit of frequency dividers is coupled to a synchronising circuit which synchronising circuit is additionally coupled to a further pulse generator whose output conveys pulses at field frequency, the output of said further pulse generator forming a supply for said synchronising circuit.
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13. A television pulse generator as claimed in any of the preceding Claims 2 to 12, suitable for use with the PAL colour television standard said television pulse generator being provided with a PAL chrominance subcarrier gating signal generator to which are applied
70 pulses at line frequency from said circuit of frequency dividers and pulses from said clock pulse generator to determine the timing of pulse edges in said gating signal, said gating signal generator incorporating a blocking signal generator for providing a blocking pulse of nine line periods duration occurring at field frequency said blocking pulse being shifted
75 over cycles of four field periods to accommodate quarter line offset, said blocking signal generator receiving pulses at field frequency from one of said pulse generators connected to said circuit of frequency dividers and pulses of a higher frequency from said circuit of frequency dividers, said subcarrier gating signal generator also receiving pulses at half line frequency.

14. A television pulse generator as claimed in any of the preceding Claims 2 to 13 in which said pulse generators and said circuit of frequency dividers incorporate J.K. flip-flops.
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15. A television pulse generator as claimed in Claim 14, in which said J.K. flip-flops have given propagation delay times, a first input of one J.K. flip-flop being connected to the output of said clock pulse generator whilst a second input is connected to the output of a further J.K. flip-flop positioned n th in series from said first J.K. flip-flop the propagation delay time from the said first input to the said output being less than n times the propagation delay time of each J.K. flip-flop.
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16. A television pulse generator as claimed in Claim 14, in which one of said J.K. flip-flops has a given propagation delay time and a trigger action on its J and K inputs, wherein in order to determine the timing of pulse edges generated by said flip-flop with a delay of the order of the propagation delay time a first command input of said flip-flop is connected to receive divided clock pulses from a second J.K. flip-flop provided in the circuit of frequency dividers, the second command input of the first mentioned flip-flop being connected to an output of a further J.K. flip-flop which succeeds said second J.K. flip-flop.
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17. A television pulse generator as claimed in Claim 14, 15 or 16, which said synchronising signal generator includes a J.K. flip-flop provided with T, K, J and S_2 inputs each input having a trigger action.
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18. A television pulse generator as claimed in Claim 14, when dependent upon Claims 9 or 10 in which said signal generator comprises a J.K. flip-flop having a set input S_1 and a reset input S_2 which inputs are connected to outputs conveying signals of said auxiliary pulse generator providing auxiliary
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pulses at line frequency and at double line frequency, said auxiliary pulse generator comprising a J.K flip-flop having differing propagation delay times between its inputs and outputs.

5 19. A television pulse generator as claimed in any of the preceding Claims 2 to 18, suitable for use with the N.T.S.C colour television standard, said television pulse generator being provided with a N.T.S.C chrominance subcarrier gating signal generator comprising a J.K flip-flop a command input of which is coupled to said clock pulse generator, a first preparatory input of said flip-flop being coupled through a differentiating circuit to said synchronising signal generator, a second preparatory input of said flip-flop being connected to said circuit of frequency dividers whilst a reset input of said flip-flop is coupled for blocking purposes to one of the pulse generators providing an auxiliary pulse of field frequency.

20. A television pulse generator as claimed in Claim 13, in which said gating signal generator comprises first and second J.K flip-flops each having a command input T and a reset input S₂, the command input T of said second flip-flop being coupled to said clock pulse generator whilst that of said first flip flop is connected to the line frequency circuit of frequency dividers, an output of said first flip-flop being connected to the reset input S₂ of said second flip-flop which flip-flop provides the said gating signal at an output, the reset input S₂ of said first flip-flop being connected to an output of the blocking signal generator.

21. A television pulse generator as claimed in Claim 13 in which said gating signal generator comprises a first J.K. flip-flop a preparatory input of which is connected to said blocking signal generator, a command input of said flip-flop being connected to an

auxiliary generator providing an auxiliary pulse of line frequency whilst the reset input of said flip-flop is connected to the line frequency circuit of frequency dividers, an output of the said flip-flop being connected to a reset input of a second J.K flip-flop an output of which provides the said gating signal and whose command input is connected to said clock-pulse generator.

22. A television pulse generator as claimed in Claim 13 or 21 in which said blocking signal generator comprises a J.K flip-flop of the type having a trigger action of all J.K. inputs, which inputs are multiple preparatory inputs some of which receive auxiliary pulses at half line frequency.

23. A television pulse generator as claimed in any of the preceding Claim 2 to 22 in which one of said pulse generators supplies pulses of relatively short duration at field frequency which pulse generator comprises a gate an input of which is coupled to a generator supplying pulses of relatively long duration at field frequency and to the field frequency circuit of frequency dividers.

24. Television equipment provided with a pulse generator as claimed in any of the preceding Claims.

25. A television synchronising and/or blanking pulse generator for generating at least one repeating pulse series comprising pulses of at least two different durations, the spacings between trailing and subsequent leading pulse edges having at least two different values, substantially as herein described with reference to the accompanying drawings.

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