WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first active pattern on a substrate, the first active pattern including a first lower pattern, which extends in a first direction, and first sheet patterns, which are on the first lower pattern;

a second active pattern on the substrate, the second active pattern including a second lower pattern, which is spaced apart from the first lower pattern in a second direction and second sheet patterns, which are on the second lower pattern, wherein the first lower pattern and the second lower pattern are separated by a fin trench;

a field insulating film disposed between the first and second lower patterns, the field insulating film being in contact with the first and second lower patterns;

a first gate structure on the substrate, the first gate structure intersecting the first active pattern;

a second gate structure on the substrate, the second gate structure intersecting the second active pattern; and

a gate separation pattern disposed on the field insulating film, the gate separation pattern being in contact with the first gate structure and second gate structure,

wherein

the first gate structure includes a first terminal region, which is disposed between the first active pattern and the gate separation pattern,

the second gate structure includes a second terminal region, which is disposed between the second active pattern and the gate separation pattern,

a distance between the gate separation pattern and the first sheet patterns is less than a distance between the gate separation pattern and the second sheet patterns, and

a first height from a vertical level of a bottom surface of the fin trench to a lowermost part of the first terminal region is greater than a second height from the vertical level of the bottom surface of the fin trench to a lowermost part of the second terminal region.

2. The semiconductor device of claim 1, wherein the first height is greater than a third height,

the third height is a height from the vertical level of the bottom surface of the fin trench to an upper surface of the first lower pattern.

3. The semiconductor device of claim 2, wherein the second height is greater than the third height.

4. The semiconductor device of any one of claims 1 to 3, further comprising:

a first separation sidewall pattern disposed between the gate separation pattern and the first sheet patterns,

wherein

the first separation sidewall pattern covers a portion of a sidewall of the gate separation pattern, and

the first gate structure covers an upper surface of the first separation sidewall pattern and is in contact with the upper surface of the first separation sidewall pattern.

5. The semiconductor device of any one of claims 1 to 3, further comprising:

a second separation sidewall pattern disposed between the gate separation pattern and the second sheet patterns,

wherein the second separation sidewall pattern covers a portion of a sidewall of the gate separation pattern.

6. The semiconductor device of any one of claims 1 to 5, wherein

the second gate structure further includes a gate insulating film,

the second sheet patterns include a lower second sheet pattern and an upper second sheet pattern on the lower second sheet pattern, and

the gate insulating film surrounds the upper second sheet pattern and does not surround the lower second sheet pattern.

7. The semiconductor device of any one of claims 4 to 6, wherein the first separation sidewall pattern is in contact with the first sheet patterns.

8. The semiconductor device of any one of claims 4 to 7, wherein the upper surface of the first separation sidewall pattern is lower than an upper surface of the first sheet patterns.

9. The semiconductor device of any one of claims 1 to 8, wherein

the first gate structure surrounds the first sheet patterns, and

the second gate structure surrounds the second sheet patterns.

10. The semiconductor device of any one of claims 1 to 3, wherein

the first gate structure includes a gate insulating film and a gate electrode on the gate insulating film, and

the gate insulating film extends along a sidewall of the gate separation pattern.

11. The semiconductor device of any one of claims 1 to 3, wherein

the first gate structure includes a gate insulating film and a gate electrode on the gate insulating film, and

the gate insulating film does not extend along a sidewall of the gate separation pattern.

12. The semiconductor device of any one of claims 1 to 3, further comprising:

a semiconductor material pattern disposed between the gate separation pattern and the first sheet patterns,

wherein

the semiconductor material pattern covers a portion of a sidewall of the gate separation pattern, and

an upper surface of the semiconductor material pattern is lower than an upper surface of the first sheet patterns.

13. A semiconductor device comprising:

a first active pattern on a substrate, the first active pattern including a first lower pattern, which extends in a first direction, and first sheet patterns, which are on the first lower pattern;

a second active pattern on the substrate, the second active pattern including a second lower pattern, which is spaced apart from the first lower pattern in a second direction, and second sheet patterns, which are on the second lower pattern, wherein the first lower pattern and the second lower pattern are separated by a fin trench;

a field insulating film disposed between the first lower pattern and the second lower pattern, the field insulating film being in contact with the first lower pattern and the second lower pattern;

a first gate structure on the substrate, the first gate structure intersecting the first active pattern;

a second gate structure on the substrate, the second gate structure intersecting the second active pattern;

a gate separation pattern disposed on the field insulating film, the gate separation pattern including a first sidewall, which faces the first sheet patterns, and a second sidewall, which faces the second sheet patterns; and

a first separation sidewall pattern disposed on a portion of the first sidewall of the gate separation pattern,

wherein an upper surface of the first separation sidewall pattern is lower than an upper surface of the first sheet patterns based on an upper surface of the first lower pattern,

the first gate structure includes a first terminal region, which is disposed between the first active pattern and the gate separation pattern,

the second gate structure includes a second terminal region, which is disposed between the second active pattern and the gate separation pattern, and

a first height from a vertical level of a bottom surface of the fin trench to a lowermost part of the first terminal region is greater than a second height from the vertical level of the bottom surface of the fin trench to a lowermost part of the second terminal region.

14. The semiconductor device of claim 13, wherein a first distance between the gate separation pattern and the first sheet patterns is less than a second distance between the gate separation pattern and the second sheet patterns.

15. The semiconductor device of claim 13 or claim 14, wherein the first gate structure covers the upper surface of the first separation sidewall pattern and is in contact with the first sidewall of the gate separation pattern.

16. The semiconductor device of any one of claims 13 to 15, wherein the second gate structure includes a gate insulating film, which surrounds the second sheet patterns, and a gate electrode, which is on the gate insulating film.

17. The semiconductor device of any one of claims 13 to 16, further comprising:

a second separation sidewall pattern disposed on a portion of the second sidewall of the gate separation pattern, the second separation sidewall pattern being in contact with the second sheet patterns.

18. The semiconductor device of claim 17, wherein a thickness, in the second direction, of the first separation sidewall pattern differs from a thickness, in the second direction, of the second separation sidewall pattern.

19. A semiconductor device comprising:

a first active pattern on a substrate, the first active pattern including a first lower pattern extending in a first direction and first sheet patterns on the first lower pattern;

a second active pattern on the substrate, the second active pattern including a second lower pattern spaced apart from the first lower pattern in a second direction and second sheet patterns on the second lower pattern, wherein the first lower pattern and the second lower pattern are separated by a fin trench;

a field insulating film disposed between the first lower pattern and the second lower pattern, the field insulating film being in contact with the first lower pattern and the second lower pattern;

a first gate structure on the substrate, the first gate structure intersecting the first active pattern and including a first gate insulating film and a first gate electrode;

a second gate structure on the substrate, the second gate structure intersecting the second active pattern and including a second gate insulating film and a second gate electrode; and

a gate separation structure disposed on the field insulating film, the gate separation structure being in contact with the first sheet patterns and the second sheet patterns,

wherein

the gate separation structure includes a lower part, which is disposed below an upper surface of the first sheet patterns, and an upper part, which is disposed above the upper surface of the first sheet patterns,

the gate separation structure includes a gate separation pattern,

the first gate structure and the second gate structure are in contact with sidewalls of the upper part of the gate separation structure,

the first gate insulating film and the second gate insulating film extend along the sidewalls of the upper part of the gate separation structure, and

a distance, in the second direction, between the upper part of the gate separation structure and the first sheet patterns is less than a distance, in the second direction, between the upper part of the gate separation structure and the second sheet patterns,

the first gate structure includes a first terminal region, which is disposed between the first active pattern and the gate separation pattern,

the second gate structure includes a second terminal region, which is disposed between the second active pattern and the gate separation pattern, and

a first height from a vertical level of a bottom surface of the fin trench to a lowermost part of the first terminal region is greater than a second height from the vertical level of the bottom surface of the fin trench to a lowermost part of the second terminal region.

20. The semiconductor device of claim 19, wherein

the gate separation structure further includes a first separation sidewall pattern, and a second separation sidewall pattern,

the gate separation structure has a first sidewall, which faces the first sheet patterns, and a second sidewall, which faces the second sheet patterns,

the first separation sidewall pattern is disposed on part of the first sidewall of the gate separation pattern, and

the second separation sidewall pattern is disposed on part of the second sidewall of the gate separation pattern.