

SPECIFICATION

DELTA SIGMA D/A CONVERTER

BACKGROUND OF THE INVENTION

The present invention relates to a delta sigma (modulation) A/D converter for digital audio equipment with a low distortion factor and a high S/N (signal to noise) ratio, particularly to a constitution from a quantizer to a local DAC (digital-to-analog converter) of a delta sigma D/A converter having three or more quantizing levels.

The delta sigma (modulation) converter is widely used as one of D/A converters for audio equipment. The performance of the D/A converter for the audio equipment is principally represented by factors such as a distortion factor (a ratio of a harmonic component to a signal) and an S/N (signal to noise) ratio. The performance of a D/A converter of related art largely depends on absolute and relative variations in characteristics of analog elements such as resistors and capacitors rather than circuit types, which variations are difficult to reduce in recent extremely finer elements. Compared with this, in the delta sigma converter for which quantizing levels ranging only from two (1 bit) to several are required, the variations among analog elements did not become a problem as those in a related art converter. In recent years, however, a high performance has been required for a D/A converter in audio equipment so as to

comply with a 24 bit format of DVD (Digital Versatile Disc) from a prior 16 bit format of CD (Compact Disc).

In order to improve the distortion factor and S/N ratio, it is theoretically necessary to increase any of an order of a delta sigma modulator, a sampling frequency or the number of quantized levels (or the number of bits) ("An oversampling A-D/D-A conversion technique (2)", Nikkei Electronics 1988. 8. 8, No.453, pp 211-221)

An excessive increase in the order of the delta sigma modulator, however, is unsuitable for ensuring stability of a feedback system called as a noise shaper. A noise shaper arithmetic unit is a unit which converts a multi-bit digital signal, inputted by oversampling, to a digital signal with lower bits than those of the multi-bit digital signal by noise shaper operation and outputs it from a quantizer. For example, a third-order noise shaper arithmetic unit is the one as is shown in Fig. 1, which comprises multipliers Y1 and Y2, delay circuits Y3, Y4 and Y5, and adders Y6 and Y7. The delay circuits Y3, Y4 and Y5, each provides a delay by one sampling period, are connected in series in this order. At the adder Y6, an output from the delay circuit Y5 and outputs from the multipliers Y1 and Y2 are added to an inputted multi-bit digital signal. At the multipliers Y1 and Y2, outputs from the delay circuits Y3 and Y4 are multiplied by coefficients 3 and -3, respectively,. The result of the addition outputted from the adder is inputted

to the quantizer 1. The output of the quantizer 1 is branched and subtracted from the input thereto at the adder Y7 to be an input to the delay circuit Y3. In the figure, an arithmetic unit is shown as the one in which a 22 bits digital signal is inputted to be converted to a 4bits digital signal with 11 levels.

As for increasing a sampling frequency, namely increasing an operating frequency of the noise shaper arithmetic unit, it requires to thereby force to increase a frequency of a system clock in audio equipment. This results in possible increase in cost of the audio equipment and its power consumption, and a possible cause of an interference noise to an analog audio system, so that the increase in frequency is limited to a certain extent.

In view of the foregoing, it is most suitable for means for providing a D/A converter with a reduced distortion factor and a heightened S/N ratio to adequately set the order of the delta sigma modulator and the sampling frequency therefor to increase the number of quantized levels. In order to adequately set the order of the delta sigma modulator and the sampling frequency therefor for increasing the number of quantized levels, a construction of a local D/A converter is necessary to be devised which carries out a D/A conversion of the output of the built-in quantizer.

The resolution of the local D/A converter in the delta sigma modulation system is a minimum of 2 levels and at most

several tens levels. Conventionally, a PWM (Pulse Width Modulation) D/A converter or DEM (Dynamic Element Matching) D/A converter have been used for three levels or above.

The advantage of the PWM converter is a possibility of high precision because a plurality of the levels are presented in a sampling period by using a clock frequency several times the sampling frequency, which clock frequency is provided by a highly precise quartz oscillator and determines the precision of conversion. However, the necessity of using the expensive high precision clock in PWM operation is the disadvantage of the PWM converter.

As for the DEM converter, a D/A converter is used with a plurality of converting elements for carrying out respective conversions at the same time. This provides the DEM converter the advantage of offering possibility of a delta sigma modulation in which the sampling frequency is set comparably high.

The DEM converter is provided with a plurality of analog elements such as resistors and capacitors, so that, when the elements are provided as those included in an IC, the precision of the DEM converter depends on relative variations among elements which occur in a semiconductor production process of the IC. In order to reduce the influence of the variations on the precision, such DEM converter is operated so that all of the elements are made to be equally used within a certain period of time according to a specified procedure. This allows

realization of a better conversion precision than the precision of the elements determined by the relative variations in a semiconductor production process.

A specific example of such a delta sigma D/A converter is shown in Fig. 2. Hereinafter the multi-level D/A converter is referred as the multi-level DAC. Here, the highest level of the multi-level DAC is taken as the levels 11 for simplicity of the explanation. In addition, twelve 1 bit local DACs are to be provided as an LDAC1 to an LDAC 12. For convenience of explanation, hereinafter the local DAC LDAC 1 to LDAC 12 are explained as being referred to simply as LDAC 1 to LDAC 12. Therefore, there is no case in which all of the LDAC 1 to LDAC 12 are turned on, that is, unit amounts are given to all of them. The D/A converter shown in Fig. 2 comprises a thermometer code converter X2 which outputs a thermometer code corresponding to the number of outputted levels from the quantizer 1 shown in Fig. 1, a barrel shifter X3 which shifts in rotation a bit arrangement of the thermometer code every sampling period, LDAC 1 to LDAC 12 which are equally weighted to each other, namely, provided with resistors with resistance values equal to each other, and an analog adder X4. The thermometer code converter 2 produces a thermometer code with the number of bits corresponding to the number of the levels outputted from the quantizer 1. Along with this, the barrel shifter X3 shifts in rotation the bit arrangement of the thermometer code to

selectively supply currents (unit amounts) to the LDAC 1 to LDAC 12. The unit amount supplied to each of the local DAC is added to others in analog to generate an analog output corresponding to the outputted levels of the quantizer 1.

However, the conventional DEM converter, which shifts the thermometer code every sampling frequency period to supply in order the unit amount equally to the N local DACs, has the following problem. Namely, the mode of rotation of the unit amount in the local DACs changes depending on the output data of the quantizer 1 converted in a form of the thermometer code to cause distortion depending on an inputted data, by which the converter is unsuitable for a DEM converter for a multi-levels over eleven levels. This is shown in Fig. 3 which presents states at every period T_s for the sampling frequency f_s about the unit amounts supplied to the LDAC 1 to LDAC 12, an integral value of errors in the local DACs, an integral value of the unit amounts in the LDAC 1 to LDAC 12, an averaged value of errors in the local DACs about the period, a cumulative average of errors in the local DACs, and an output level of the analog adder 9. As shown in Fig. 3, the thermometer code of 1 level is inputted to only one local DAC in one sampling period T_s . Therefore, as is apparent from Fig. 3, for a quantized output X lasting with level 1, it takes several cycles of T_s until all of the LDAC 1 to LDAC 12 are used. While, for a quantized output X with the higher number of levels almost all of the local DACs are used in 1 cycle of

Ts. That is, the DEM converter has the disadvantage in that averaging of variations in local DACs tends to depend on signal values. In this regard, a simulation is carried out for the case where LDAC 1 to LDAC 12 have errors shown in the right upper column in Fig. 3. The result of the simulation shows that influence of the error for a signal in lower level is liable to remain over.

While, there is a DEM converter in which, although no detailed configuration thereof is explained here, the unit amounts corresponding to a code are given to all of N local DACs in order in a sampling period Ts so that every local DAC is equally used. Such DEM converter, however, has the following problem.

For quantized levels of N and a noise shaper frequency of fs, at least a frequency of as high as ($N \cdot f_s$) is necessary for a system clock, so that an audio system must provide an expensive system clock. Figure 4 is a diagram showing a result of simulation carried out about a case where a high system clock frequency is used under the same error conditions as those in the case shown in Fig. 3. In the figure, a case is shown where a sampling period Ts is finely divided by twelve. In a period of ($T_s/12$), one level is given to one of LDAC 1 to LDAC 12 in rotation. This allows all of the local DACs to be equally used even for an output of the quantizer being in one level, so that the output of the converter is fully averaged in a sampling period Ts. In this case, however, a clock with a frequency as high

as $12f_s$ is necessary, which induces a problem in cost.

SUMMARY OF THE INVENTION

In view of the foregoing, in the present invention, a bit arrangement of the thermometer code is divided into P blocks each being taken as one block for every Q bits, the bit arrangement is shifted in unit of the block in rotation at the sampling frequency f_s , the bit arrangement is further shifted in unit of the bit in rotation at a frequency $f_s \cdot Q$ and a code output of the shifted code is produced, each of bits of which output is given to the local DAC corresponding to each of the bits. Alternatively, the bit arrangement of the code output, which arrangement is taken as being expressed in terms of a matrix having P rows and Q columns where P represents an arrangement of the blocks and Q represents an arrangement in the block, is converted to a code output expressed in terms of a matrix having Q rows and P columns by interchanging the rows and columns with each other, by which a scattering in space is provided for the local DACs supplied with unit amounts. By means of any one or combination of the two, it is allowed to keep an operating frequency lower and to reduce distortion in the output which is due to change in shifting the data in rotation in the local DACs, which change occurs depending on bit levels of the data in a form of the thermometer code. That is, the present invention solves the problems arisen in a conventional DEM converter to

allow the realization of a D/A converter in which cost rising thereof is prevented while improved converting performance thereof being provided.

Thus, the delta sigma D/A converter is constituted to comprise a set of $(P \cdot Q)$ numbers (each of P and Q is an arbitrary integer of two or more) of 1 bit local DACs (digital to analog converters) equally weighted to each other; a quantizer producing an output with a quantized levels of $(P \cdot Q - 1)$ levels at a sampling frequency f_s ; a first converter converting the output of the quantizer to a thermometer code comprising $P \cdot Q$ bits; and a second converter receiving the thermometer code, dividing a bit arrangement of the thermometer code into P blocks each being taken as one block for every Q bits, shifting the bit arrangement in unit of the block in rotation at the sampling frequency f_s , further shifting the bit arrangement in unit of the bit in rotation at a frequency $(f_s \cdot Q)$, and producing a code output of the shifted code, each of bits of the code output produced in the second converter being given to the local DAC corresponding to each of the bits.

It is preferable for the second converter to convert the bit arrangement of the code output, which arrangement is taken as being expressed in terms of a matrix having P rows and Q columns where P represents an arrangement of the blocks and Q represents an arrangement in the block, to a code output expressed in terms of a matrix having Q rows and P columns by interchanging the

rows and columns with each other, and to supply the code output, expressed in terms of a matrix having Q rows and P columns, to a set of the $(P \cdot Q)$ numbers of the local DACs, the local DACs being disposed in parallel with each other on a semiconductor substrate, and being arranged to be provided with Q blocks corresponding to the Q rows in order each provided with P local DACs corresponding to the P columns so that each receives each code output corresponding thereto.

In addition, the delta sigma D/A converter is also constituted as to comprise: a set of $(P \cdot Q)$ numbers (each of P and Q is an arbitrary integer of two or more) of 1 bit local DACs (digital to analog converters) equally weighted to each other; a quantizer producing an output with a quantized levels of $(P \cdot Q - 1)$ levels at a sampling frequency f_s ; a first converter converting the output of the quantizer to a thermometer code comprising $P \cdot Q$ bits; and a second converter receiving the thermometer code, dividing a bit arrangement of the thermometer code into P blocks each being taken as one block for every Q bits, converting the bit arrangement of the code output, which arrangement is taken as being expressed in terms of a matrix having P rows and Q columns where P represents an arrangement of the blocks and Q represents an arrangement in the block, to a code output expressed in terms of a matrix having Q rows and P columns by interchanging the rows and columns with each other, and supplying the code output, expressed in terms of a matrix

having Q rows and P columns, to a set of the $(P \cdot Q)$ numbers of the local DACs, the local DACs being disposed in parallel with each other on a semiconductor substrate, and being arranged to be provided with Q blocks corresponding to the Q rows in order each provided with P local DACs corresponding to the P columns so that each receives each code output corresponding thereto.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating an example of a configuration of a third-order noise shaper arithmetic unit as a principal part of a delta sigma D/A converter in related art;

Fig. 2 is a diagram illustrating an example of a configuration of a delta sigma D/A converter in related art;

Fig. 3 is a diagram illustrating operation of the delta sigma D/A converter shown in Fig. 2;

Fig. 4 is a diagram illustrating operation of the delta sigma D/A converter shown in Fig. 2 with a higher clock frequency;

Fig. 5 is a diagram illustrating a configuration of the first embodiment of the delta sigma D/A converter according to the present invention;

Fig. 6 is a diagram illustrating operation of the delta sigma D/A converter shown in Fig. 5;

Fig. 7 is a diagram as a continuation of Fig. 6 illustrating operation of the delta sigma D/A converter shown in Fig. 5;

Fig. 8 is a diagram illustrating a configuration of the

second embodiment of the delta sigma D/A converter according to the present invention; and

Fig. 9 is a diagram illustrating a configuration of a modification of the second embodiment of the delta sigma D/A converter according to the present invention;

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described with reference to the drawings.

The sigma delta D/A converter according to the present invention will be explained in detail about the first embodiment shown in Fig. 5.

In the figure, the same reference numerals as those shown in Figs. 1 and 2 designate the same constituents. Numerals 1 and 2 designate a quantizer and a thermometer code converter, respectively. The quantizer 1 converts a multi-bit digital signal, a 24 bit digital signal for example, inputted with a sampling frequency f_s to a 4 bit digital signal with 11 levels. The thermometer code converter 2 converts the output signal from the quantizer 1 to a 12 bit thermometer code. For example, a quantized output of one level "0001" from the quantizer 1 is converted to a thermometer code of "000000000001", and a quantized output of two levels "0010" is converted to as "000000000011". Numeral 3 designates a frequency dividing circuit, numeral 4 a three state counter, numeral 5 a barrel

shifter, and numeral 6 a data latch. The frequency dividing circuit 3 carries out frequency division of a clock signal with a frequency $4 f_s$ with a submultiple 4 to output a clock signal with a frequency f_s . The three state counter 4 carries out counting of three values according to the clock signal with the frequency f_s . The barrel shifter 5 carries out shifting in rotation depending on the count of the three state counter 4, in which the bit arrangement of the thermometer code is divided into P blocks, 3 blocks here, each of which is constituted of Q bits, 4 bits here. The blocks are shifted in rotation as $P = 1, 2, 3, 1, 2, 3$, depending on the counted value of the three state counter 4. For example, a thermometer code with an initial bit arrangement "000000000001" is outputted while being shifted in rotation depending on the counted value of the three state counter 4 as "000000010000", "000100000000", and then, "000000000001". The data latch 6 latches a code outputted from the barrel shifter 5 in response to the clock signal with the frequency f_s . Numeral 7 designates a shift register which shifts a code outputted from the data latch 6 one bit by one in each of the blocks in rotation in response to the clock signal with the frequency of $4 f_s$. Numeral 8 designates a data latch which latches the code outputted from the shift register 7 in response to the clock signal with the frequency of $4 f_s$. LDAC1 to LDAC 12 are 1 bit local DACs each of which is equally weighted to another and corresponds to each bit of the code outputted from

the data latch 8 so as to be supplied with a specified unit amount when the corresponding bit is "1". Numeral 9 designates an analog adder which is connected to the LDAC 1 to LDAC 12 for carrying out an analog addition of the unit amounts supplied to them to produce an analog output.

An operation of the embodiment will be explained with reference to Figs. 5, 6 and 7. Figure 6 and Figure 7, a continuation of Figure 6, show states in every period T_s and in every period $T_s/4$ to the sampling frequency f_s . The states are shown about the unit amounts supplied to the LDAC 1 to LDAC 12, an integral value outputted from the analog adder 9, an integral value and an averaged value of errors in the local DACs about a period, a cumulative average of errors in the local DACs, and an output level of the analog adder 9.

First, a 4bit digital signal X outputted from the quantizer 1 is converted to a thermometer code by the thermometer code converter 2. The barrel shifter 5 shifts each block P of 4 bits in the thermometer code in the order of $P = 1, 2, 3, 1, 2 \dots$ at the sampling frequency f_s . The shifting operation of the barrel shifter 5 is carried out in response to the output of the three state counter 3 operated at a frequency of f_s . The data latch 6 holds the result of the shifting at the barrel shifter 5. The shift register 7 shifts the output of the data latch 6 at a frequency of $4f_s$. The code outputted from the shift resistor 7, which are taken as $Y(P, Q)$, is supplied to each of

LDAC 1 to LDAC 12, the outputs of which are then added to be obtained as an analog output.

The LDAC 1 to LDAC 12 are equally divided into three blocks as a block of the LDAC 1 to LDAC 4 be taken as a DAC block ($P = 1$), that of the LDAC 5 to LDAC 8 be a DAC block ($P = 2$) and that of the LDAC 9 to LDAC 12 be a DAC block ($P = 3$). The shift register 7 shifts the thermometer code 2 in rotation in the LDAC 1 to LDAC 12 by 1 LDAC every period of $T_s/4$, to which the sampling period T_s is divided by submultiple 4. Along with this, the barrel shifter 5 shifts the thermometer code in rotation by one block every period of T_s to thereby shift the thermometer code in the DAC block every 1 T_s in rotation as $P = 1, 2, 3, 1, 2 \dots$. This allows, as shown in Fig. 6 and Fig. 7, the thermometer code, even when it is of level 1, to be supplied to all of the LDACs in 3 T_s periods to reduce the number of the sampling period required for averaging. Figures 6 and 7 show the result of a simulation about the case in which the LDAC 1 to LDAC 12 have errors as shown in the upper right column in Fig. 7, which case is the same as that explained with reference to Fig. 3. It can be understood from the result of the simulation that influence of error due to a lower level code is reduced more shortly compared with the case in a conventional converter as shown in Fig. 3.

As explained above, the system according to the present invention can eliminate an error due to variation in characteristic of the local DAC without setting the frequency

of the system clock extremely high to thereby allow to improve the method of providing better performance which was conflictingly carried out previously by either highly increasing the system clock frequency or highly increasing the number of levels.

The present invention is not limited to the first embodiment. A second embodiment of the present invention will be explained below with reference to Fig. 8A.

In the second embodiment, the bit arrangement of the thermometer code is taken as being divided into P blocks each including Q bits. The bit arrangement of the code is then taken as being expressed in terms of a matrix having P rows and Q columns in which the arrangement of the blocks is in rows and the arrangement of the bits in the blocks is in columns. The matrix is then transposed and thus arranged code is then outputted to a plurality of the local DACs. The transposition results in allowing the unit amounts to be supplied to spatially scattered local DACs to reduce input data dependent distortions. In Fig. 8A, an arrangement of 12 bit code, which was previously supplied directly to the local DACs through the thermometer code converter and the barrel shifter, although this is not particularly shown here, is taken as being expressed as $y(P, Q)$ with the bit arrangement divided into P blocks (here $P = 1$ to 3) in order for every Q bits (here $Q = 1$ to 4). Each of numerals 10 and 11 designate a data latch. The data latch 10 receives the code

$y(P, Q)$ and outputs the code with the bit arrangement as received. The data latch 11 divides the bit arrangement of the input into Q blocks in order for every P bits. At the input ($P = 1$) in the input block ($Q = 1$), the output ($Q = 1$) of the output block ($P = 1$) of the data latch 10 is received, at the input ($P = 2$) in the input block ($Q = 1$), the output ($Q = 1$) of the output block ($P = 2$) of the data latch 10 is received, and at the input ($P = 3$) in the input block ($Q = 1$), the output ($Q = 1$) of the output block ($P = 3$) of the data latch 10 is received. In this way, at each of the inputs, the data latch 11 receives the output of the data latch 10 with the output block number and the bit number in the block of the data latch 10 being interchanged with each other. Thus, the inputted code $y(P, Q)$ in terms of a matrix having P rows and Q columns is outputted as a code $z(Q, P)$, a transposed matrix with the rows and columns in the former being interchanged.

Each bits of the outputted code $Z(Q, P)$ from the latch 11 is outputted to the LDAC1 to LDAC12, letting the bit arrangement as it is.

As described above, in the embodiment, a scattering in space is provided for the local DACs supplied with unit amounts to allow reduction of the input data dependent distortion in the output, which is due to change in shifting the data in rotation in the local DACs, which change occurs depending on bit levels of the output data in a form of the thermometer code.

In addition, even with wiring as shown in Fig. 8B, which is provided from the data latch 10 to the LDAC 1 to LDAC 12 particularly with the data latch 11 being omitted, the same function and effect can be obtained as above.

The embodiment may be modified as shown in Fig. 9 so that the code $Y(P, Q)$, outputted from the shift register 7 in terms of a matrix, is inputted to the data latch 11 with the rows and columns being interchanged like the method of outputting from the data latch 10 to the data latch 11 in the above embodiment. This, like in the first embodiment, also provides a scattering in time for the local DACs supplied with the unit amounts to further average variations among the local DACs for improving distortion factor and S/N ratio of the DAC.

In the delta sigma D/A converter according to the present invention, a control is carried out for equalizing variation among multi-level local DACs both in time and in space without increasing a noise shaper frequency f_s more than necessary. This allows the realization of a lower distortion and a higher S/N ratio required for the performance of audio equipment.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details can be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A delta sigma D/A converter comprising:

a set of ($P \cdot Q$) numbers (each of P and Q is an arbitrary integer of two or more) of 1 bit local DACs (digital to analog converters) equally weighted to each other;

a quantizer producing an output with a quantized levels of ($P \cdot Q - 1$) levels at a sampling frequency f_s ;

a first converter converting the output of the quantizer to a thermometer code comprising $P \cdot Q$ bits; and

a second converter receiving the thermometer code, dividing a bit arrangement of the thermometer code into P blocks each being taken as one block for every Q bits, shifting the bit arrangement in unit of the block in rotation at the sampling frequency f_s , further shifting the bit arrangement in unit of the bit in rotation at a frequency ($f_s \cdot Q$), and producing a code output of the shifted code,

each of bits of the code output produced in the second converter being given to the local DAC corresponding to each of the bits.

2. A delta sigma D/A converter as claimed in claim 1 wherein the second converter converts the bit arrangement of the code output, which arrangement is taken as being expressed in terms of a matrix having P rows and Q columns where P represents an arrangement of the blocks and Q represents an arrangement in the block, to a code output expressed in terms of a matrix



having Q rows and P columns by interchanging the rows and columns with each other, and supplies the code output, expressed in terms of a matrix having Q rows and P columns, to a set of the $(P \cdot Q)$ numbers of the local DACs,

the local DACs being disposed in parallel with each other on a semiconductor substrate, and being arranged to be provided with Q blocks corresponding to the Q rows in order each provided with P local DACs corresponding to the P columns so that each receives each code output corresponding thereto.

3. A delta sigma D/A converter comprising:

a set of $(P \cdot Q)$ numbers (each of P and Q is an arbitrary integer of two or more) of 1 bit local DACs (digital to analog converters) equally weighted to each other;

a quantizer producing an output with a quantized levels of $(P \cdot Q - 1)$ levels at a sampling frequency f_s ;

a first converter converting the output of the quantizer to a thermometer code comprising $P \cdot Q$ bits; and

a second converter receiving the thermometer code, dividing a bit arrangement of the thermometer code into P blocks each being taken as one block for every Q bits, converting the bit arrangement of the code output, which arrangement is taken as being expressed in terms of a matrix having P rows and Q columns where P represents an arrangement of the blocks and Q represents an arrangement in the block, to a code output expressed in terms of a matrix having Q rows and P columns by interchanging the



rows and columns with each other, and supplying the code output, expressed in terms of a matrix having Q rows and P columns, to a set of the $(P \cdot Q)$ numbers of the local DACs,

the local DACs being disposed in parallel with each other on a semiconductor substrate, and being arranged to be provided with Q blocks corresponding to the Q rows in order each provided with P local DACs corresponding to the P columns so that each receives each code output corresponding thereto.



DELTA SIGMA D/A CONVERTER

ABSTRACT

A thermometer code outputted from a thermometer code converter 2 is divided into P blocks for every Q bits. An arrangement of the blocks is shifted in rotation by a barrel shifter 5 at a frequency f_s . Along with this, an arrangement of bits in the block is shifted in rotation by a shift register 7 at a frequency $(Q \cdot f_s)$, the frequency f_s multiplied by Q . The bits of thus obtained code is given to local DACs (LDAC 1 to LDAC 12) each specified to correspond to each of the given bits. This allows to keep an operating frequency lower and to reduce distortion in the output which is due to change in shifting the data in rotation in the local DACs, which change occurs depending on bit levels of the data in a form of the thermometer code.

This Sheet Has Been Replaced



THIS SHEET HAS BEEN
REPLACED

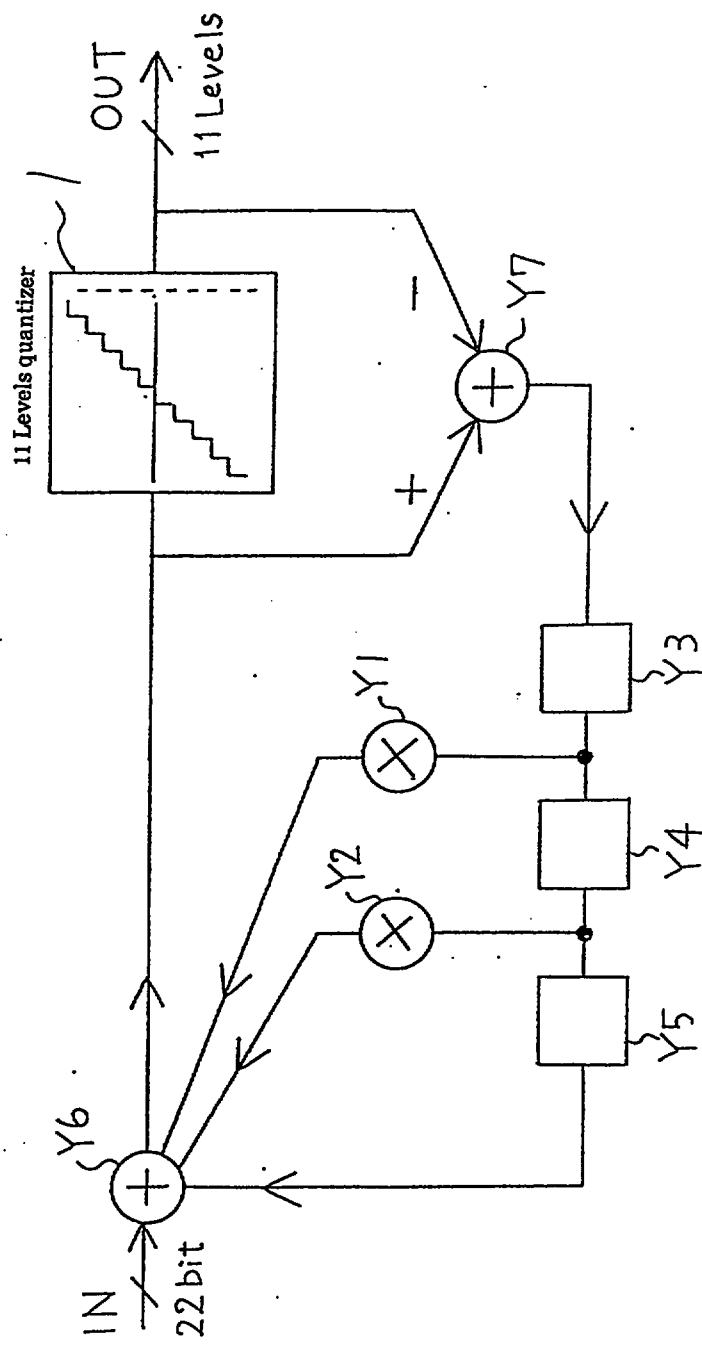


Fig.1

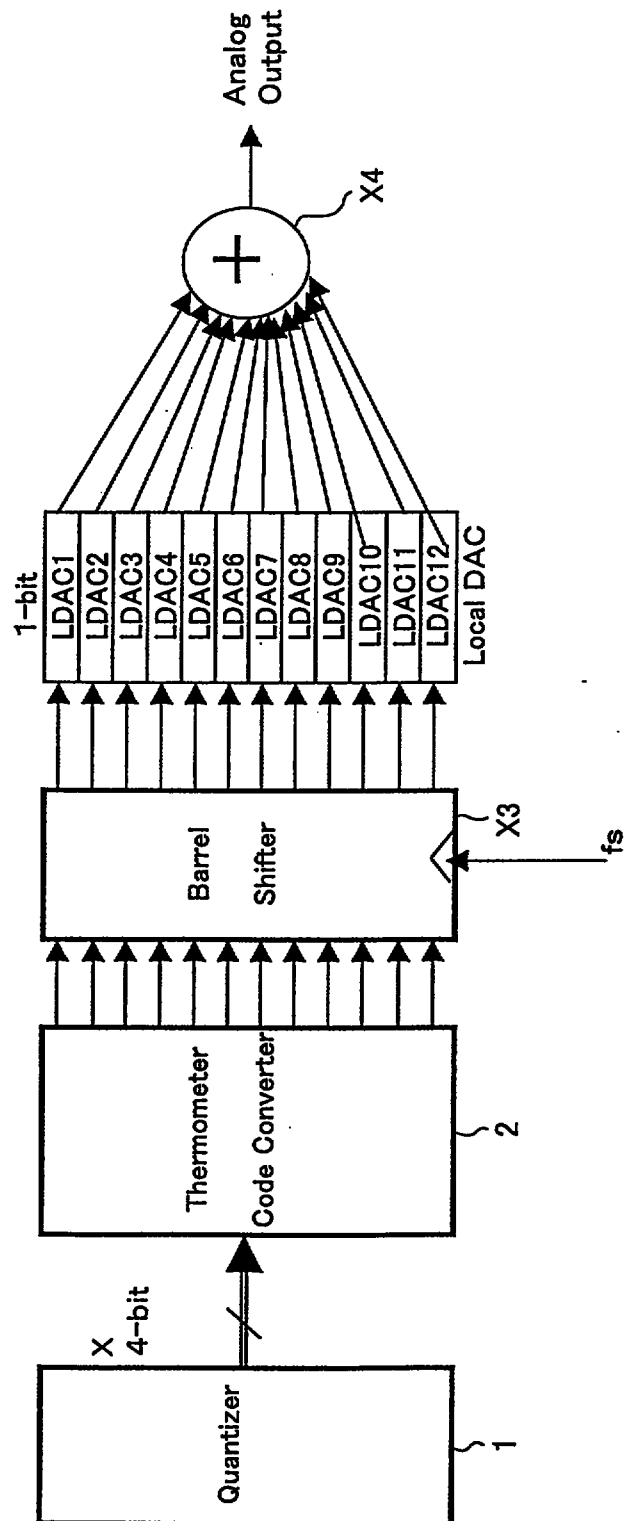


Fig.2

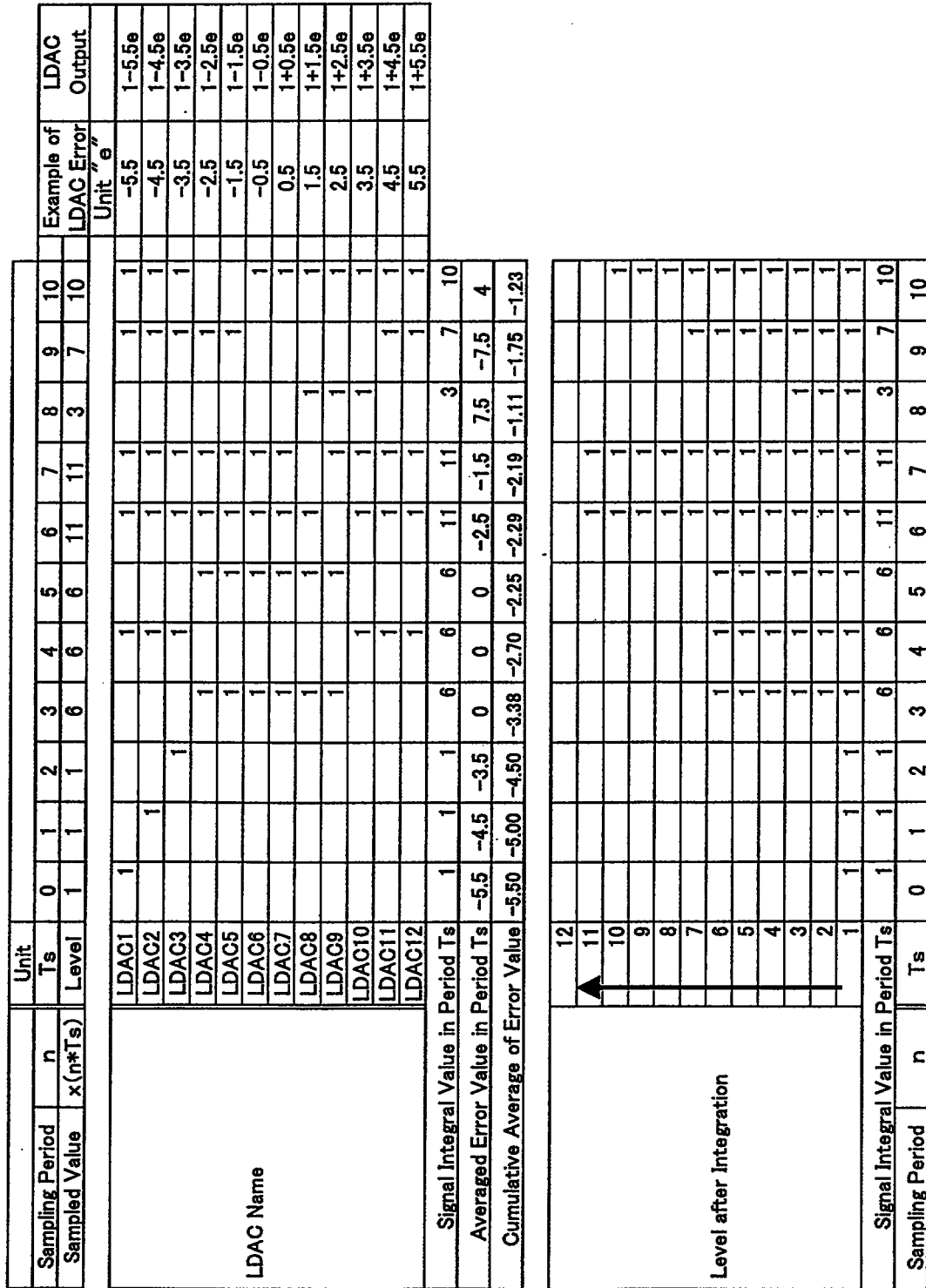


Fig.3

[illegible]

Fig. 4

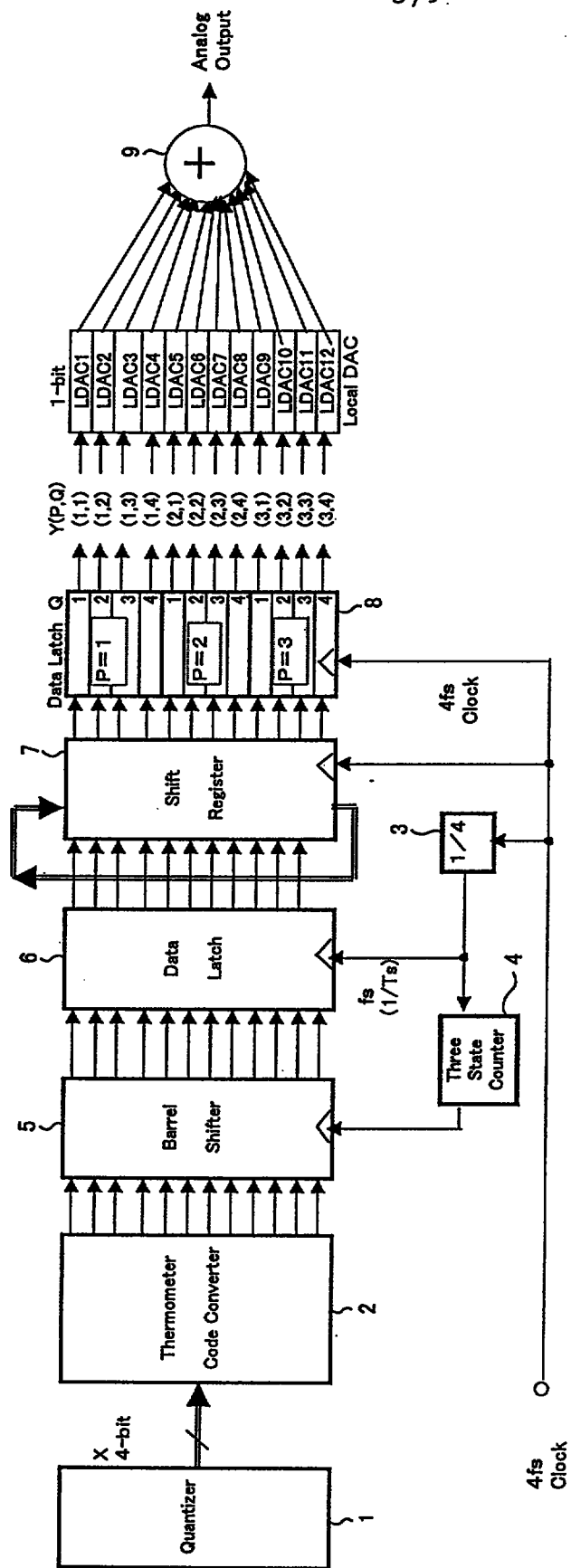


Fig.5

		Unit																
Sampling Period	n	Ts	0				1				2				3			
Clock	m	Ts/4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
Sampled Value	d(n*Ts)	Level	1				1				1				6			

Start Block		Q	1				2				3				1			
DAC Name	DAC Block P=1	1 LDAC1	1												1			
		2 LDAC2		1											1	1		
		3 LDAC3			1										1	1	1	
		4 LDAC4				1									1	1	1	1
	DAC Block P=2	1 LDAC5					1								1	1	1	1
		2 LDAC6						1							1	1	1	1
		3 LDAC7							1						1	1	1	1
		4 LDAC8								1						1	1	1
	DAC Block P=3	1 LDAC9									1							1
		2 LDAC10										1						
		3 LDAC11											1					
		4 LDAC12													1			
Signal Integral Value in Period Ts			1	1	1	1	1	1	1	1	1	1	1	1	6	6	6	6
Signal Integral Value in Period Ts/4			1				1				1				6			
Error Integral Value in Clock Period			-5.5	-4.5	-3.5	-2.5	-1.5	-0.5	0.5	1.5	2.5	3.5	4.5	5.5	-18	-12	-6	0
Averaged Error Value in Period Ts			-4				0				4				-9			
Cumulative Average of Error Value			-4.00				-2.00				0.00				-2.25			

Level after Integration	12																	
	11																	
	10																	
	9																	
	8																	
	7																	
	6														1	1	1	1
	5														1	1	1	1
	4														1	1	1	1
	3														1	1	1	1
	2														1	1	1	1
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Signal Integral Value in Clock Period			1	1	1	1	1	1	1	1	1	1	1	1	6	6	6	6
Quarter of Signal Integral Value in Periods Ts			1				1				1				6			
Time	n	Ts	0				1				2				3			

Fig.6

		Unit																		
Sampling Period	n	Ts	4				5				6				7					
Clock	m	Ts/4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4		
Sampled Value	d(n*Ts)	Level	6				6				11				11					
																		Example of LDAC Error	LDAC Output	
Start Block		Q	2				3				1				2				Unit "e"	
DAC Name	DAC Block P=1	1 LDAC1				1	1	1	1	1	1	1	1	1	1	1	1	1	-5.5	1-5.5e
		2 LDAC2					1	1	1	1	1	1	1	1	1	1	1	1	-4.5	1-4.5e
		3 LDAC3						1	1	1	1	1	1	1	1	1	1	1	-3.5	1-3.5e
		4 LDAC4							1	1	1	1	1	1	1	1	1	1	-2.5	1-2.5e
	DAC Block P=2	1 LDAC5	1						1	1	1	1	1	1	1	1	1	1	-1.5	1-1.5e
		2 LDAC6	1	1						1	1	1	1	1	1	1	1	1	-0.5	1-0.5e
		3 LDAC7	1	1	1					1	1	1	1	1	1	1	1	1	0.5	1+0.5e
		4 LDAC8	1	1	1	1				1	1	1	1	1	1	1	1	1	1.5	1+1.5e
	DAC Block P=3	1 LDAC9	1	1	1	1	1			1	1	1	1	1	1	1	1	1	2.5	1+2.5e
		2 LDAC10	1	1	1	1	1	1		1	1	1	1	1	1	1	1	1	3.5	1+3.5e
		3 LDAC11		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	4.5	1+4.5e
		4 LDAC12			1	1	1	1	1	1	1	1	1	1	1	1	1	1	5.5	1+5.5e
Signal Integral Value in Period Ts			6	6	6	6	6	6	6	6	11	11	11	11	11	11	11	11		
Signal Integral Value in Period Ts/4			6				6				11				11					
Error Integral Value in Clock Period			6	12	18	12	6	0	-6	-12	-6	5.5	4.5	3.5	2.5	1.5	0.5	-1		
Averaged Error Value in Period Ts			12				-3				2				1					
Cumulative Average of Error Value			0.60				0.00				0.29				0.38					

Level after Integration	12																			
	11										1	1	1	1	1	1	1	1	1	
	10										1	1	1	1	1	1	1	1	1	
	9										1	1	1	1	1	1	1	1	1	
	8										1	1	1	1	1	1	1	1	1	
	7										1	1	1	1	1	1	1	1	1	
	6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Signal Integral Value in Clock Period		6	6	6	6	6	6	6	6	6	11	11	11	11	11	11	11	11	11	
Quarter of Signal Integral Value in Periods Ts		6				6				11				11						
Time	n	Ts	4				5				6				7					

Fig.7

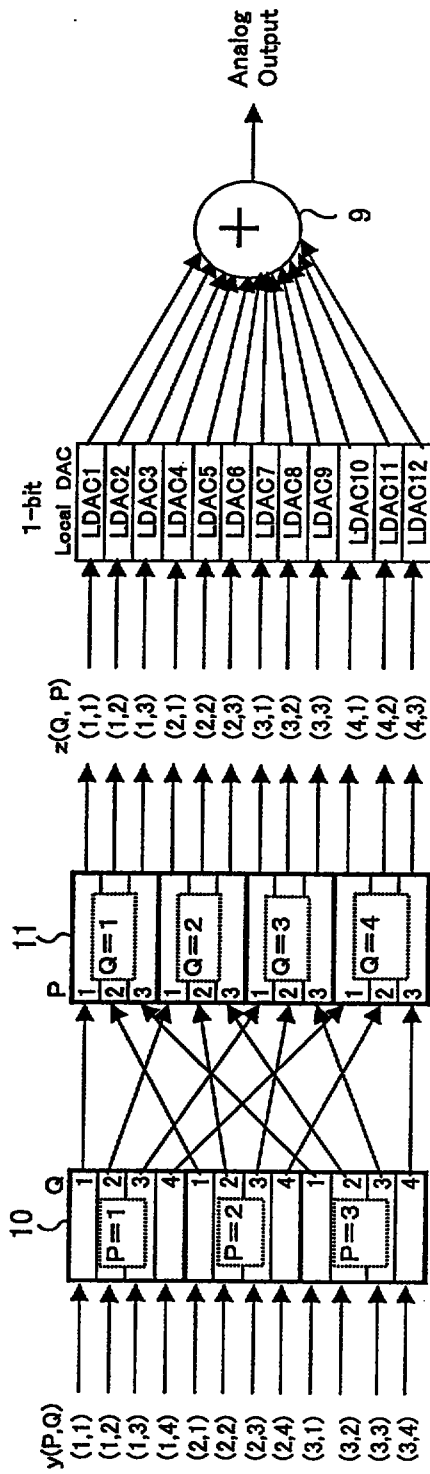


Fig. 8A

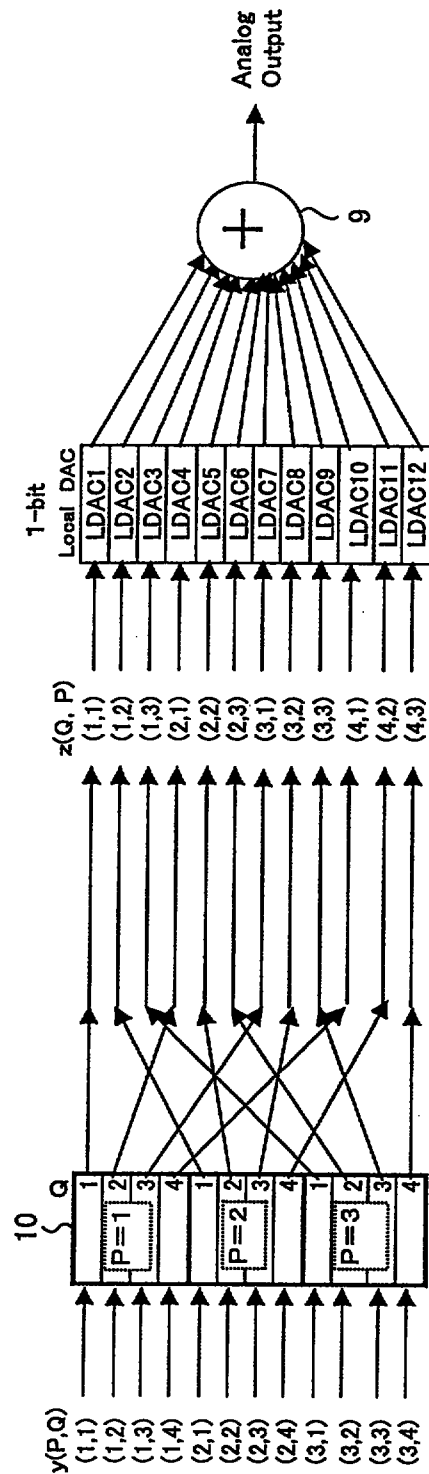
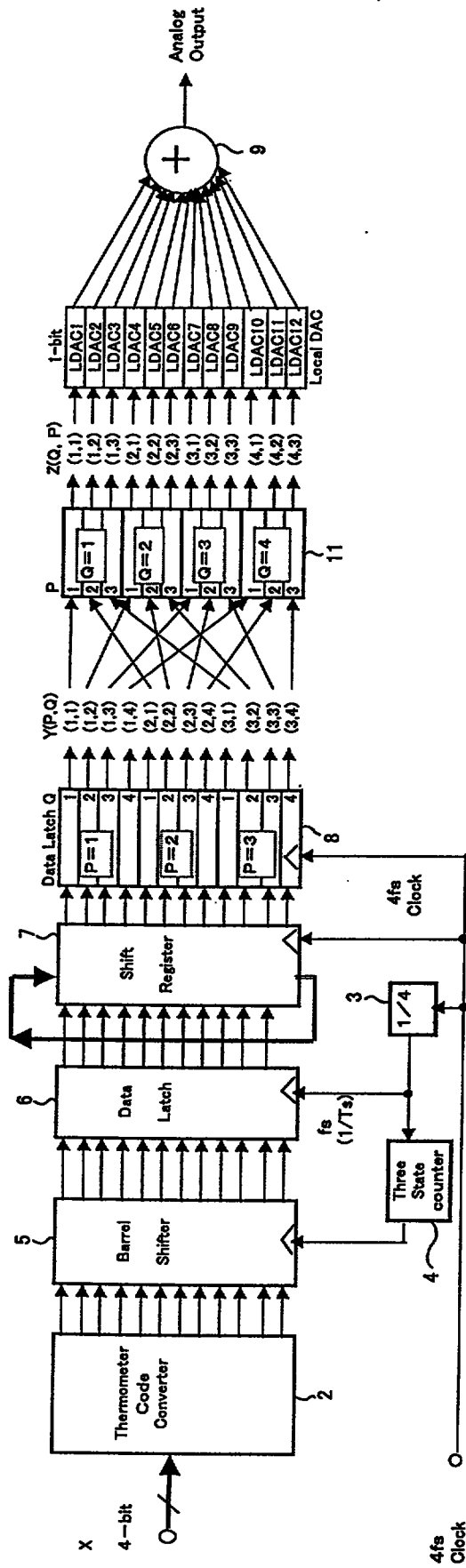


Fig. 8B



6.5

REPLACEMENT SHEET
Date : 20/10/00

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DELTA SIGMA D/A CONVERTER

ABSTRACT

A thermometer code outputted from a thermometer code converter 2 is divided into P blocks for every Q bits. An arrangement of the blocks is shifted in rotation by a barrel shifter 5 at a frequency f_s . Along with this, an arrangement of bits in the block is shifted in rotation by a shift register 7 at a frequency $(Q \cdot f_s)$, the frequency f_s multiplied by Q. The bits of thus obtained code is given to local DACs (LDAC 1 to LDAC 12) each specified to correspond to each of the given bits. This allows to keep an operating frequency lower and to reduce distortion in the output which is due to change in shifting the data in rotation in the local DACs, which change occurs depending on bit levels of the data in a form of the thermometer code.

Figure 5

REPLACEMENT SHEET
02 OCT 2000