CLAIMS

1. A substrate processing method comprising:

depositing a conformal silicon film on a three dimensional structure formed on a substrate;

exposing the silicon film to a metal halide to form a capping layer comprising metal and halogen atoms;

annealing the capping layer to diffuse halogen atoms from the capping layer and dope the three dimensional structure with the halogen atoms of the capping layer; and

removing the capping layer.

2. The method of claim 1, wherein the three dimensional structure comprises a FinFET structure.

3. The method of claim 1, wherein the three dimensional structure comprises a layered stack, the layered stack comprising a dielectric layer, a high-k layer and a nitride layer.

4. The method of claim 3, wherein the dielectric layer comprises silicon and oxygen.

5. The method of claim 3, wherein the high-k layer comprises Hf and O.

6. The method of claim 3, wherein the nitride layer comprises one or more of TiN, TiSiN, TaN, or TaSiN.

7. The method of claim 1, wherein depositing the silicon film comprises exposing the substrate to a silicon precursor, the silicon precursor comprising at least one species with a general formula of Si_xH_y, where x is an integer from 1 to 4 and y is 2x+2.

8. The method of claim 7, wherein the substrate is maintained at a temperature in a range of 400 °C to 550 °C.

9. The method of claim 1, further comprising annealing the substrate after depositing the silicon film.

10. The method of claim 9, wherein the silicon film is annealed at a temperature in a range of 500 °C to 1000 °C for a period in a range of 1 ms to 10 s.

11. The method of claim 1, wherein the metal halide comprises W.

12. The method of claim 1, wherein the metal halide comprises one or more of F or Cl.

13. The method of claim 1, wherein the metal halide consists essentially of WF_6.

14. The method of claim 1, wherein the substrate is maintained at a temperature of 100 °C to 500 °C while the substrate is exposed to the metal halide.

15. The method of claim 1, wherein the capping layer further comprises silicon.

16. The method of claim 1, wherein the substrate is maintained at a temperature of 200 °C to 1000 °C while the substrate is annealed to diffuse halogen atoms below the capping layer.

17. The method of claim 1, wherein the capping layer is removed by an etch process.

18. A substrate processing method comprising:

depositing a conformal silicon film on a FinFET structure formed on a substrate, the FinFET structure comprising a layered stack with at least an interlayer dielectric layer, a high-k layer and a nitride layer;

exposing the silicon film to WF_6 to form a capping layer comprising tungsten and fluorine atoms;

annealing the capping layer to diffuse fluorine atoms from the capping layer into the high-k layer doping the high-k layer with an atomic percent of fluorine atoms in a range of greater than 0 to less than or equal to 25; and removing the capping layer.

19. The method of claim 18, wherein removing the capping layer comprises removing the capping layer and a portion of the nitride layer and reforming the nitride layer.

20. A substrate processing method comprising:

depositing a conformal silicon film on a FinFET structure formed on a substrate by exposing the substrate to a silicon precursor, the silicon precursor comprising at least one species with a general formula of Si_xH_y, where x is an integer 1 to 4 and y is 2x+2, the FinFET structure comprising a layered stack with at least an interlayer dielectric layer comprising SiO, a high-k layer comprising HfO and a nitride layer comprising TiN;

exposing the silicon film to WF_6 to form a capping layer comprising tungsten and fluorine atoms;

annealing the capping layer at a temperature in a range of 200 °C to 1000 °C to diffuse fluorine atoms from the capping layer into the high-k layer doping the high-k layer with an atomic percentage of fluorine atoms in a range of greater than 0 to less than or equal to 25; and removing the capping layer.