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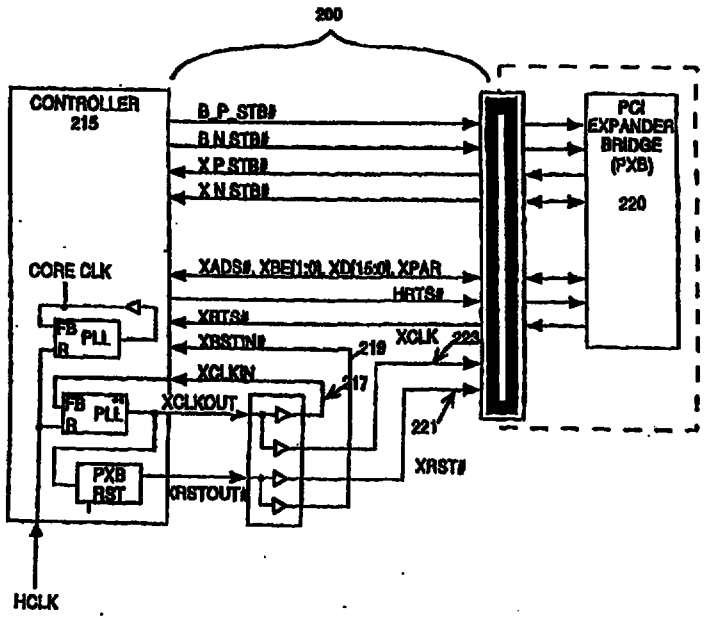
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(54) Title: FAST 16-BIT, SPLIT TRANSACTION I/O BUS



(57) Abstract

A synchronous bus system that enables the bus lengths between devices to be extended such that the timing budget is more than one clock cycle. A reset process (215 and 220) resets the transmission and reception circuitry and both circuitry function according to prespecified parameters relative to the deassertion of the reset signal such that the amount of logic required to latch and sample the data is minimized. As the timing budget is not limited to one clock cycle, devices can be spaced further apart providing more physical space for devices. Furthermore, skew sensitivity is reduced as the skew is distributed over multiple clock periods.