

THIS SHEET HAS BEEN
REPLACED

PROVISIONAL PATENT
Docket No. 5774.41 (GT2H-2)

**IMPROVED MAIN AMPLIFIER CIRCUIT AND INPUT-
OUTPUT BUS FOR DYNAMIC RANDOM ACCESS MEMORY**

Abstract of the Disclosure

A semiconductor memory is provided with a main amplifier circuit that is capable of selectively driving and precharging two I/O buses in conjunction with a write amplifier. The main amplifier circuit includes a separation and precharge section and an activation section. The activation section drives a signal for activating the first section to precharge the two I/O signals only when the two I/O buses are ~~not~~ being separated. The main amplifier circuit also includes both a main output bus and a test output bus. In so doing, the semiconductor memory can operate in a normal mode and a test mode. In the test mode, twice as many memory cells of the semiconductor memory can be accessed simultaneously, thereby reducing test time. The semiconductor memory, which can be one of many different data widths, has different sized output buses associated with each data width. Output buses with a relatively large capacitance can be produced with a large width, giving them a relatively small resistance. Conversely, output buses with a relatively small capacitance can be produced with a small width, giving them a relatively large resistance. As a result, a time constant for the output buses associated with each of the different widths is very similar.

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