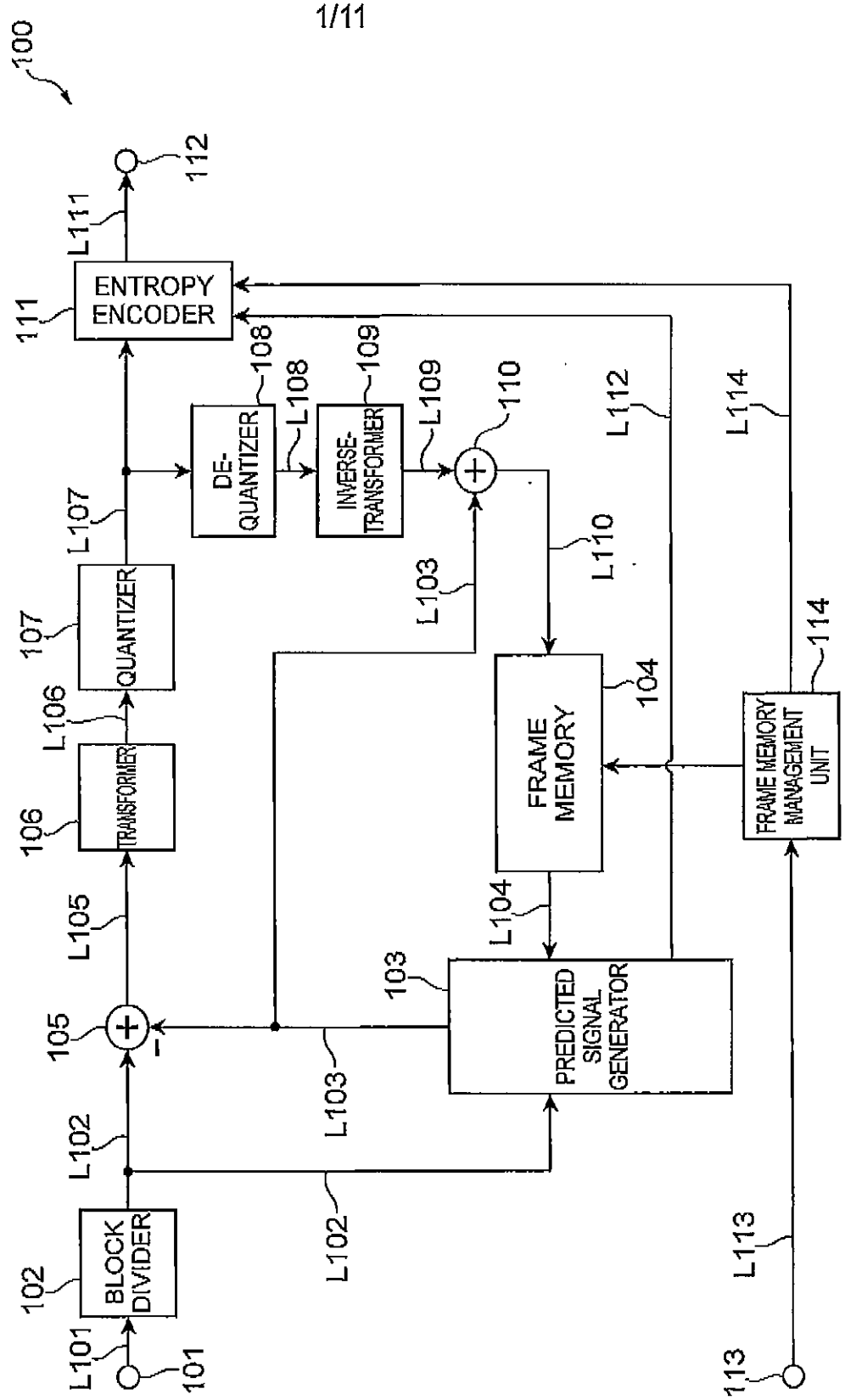
Fig.1


100
ENTROPY ENCODER
111
L111
112
DE-QUANTIZER
108
L108
INVERSE-TRANSFORMER
109
L109
110
L112
L114
QUANTIZER
107
L107
TRANSFORMER
106
L106
L103
L110
FRAME MEMORY
104
114
FRAME MEMORY MANAGEMENT UNIT
L105
105
L104
103
PREDICTED SIGNAL GENERATOR
L102
L103
L102
BLOCK DIVIDER
102
L101
101
L113
113

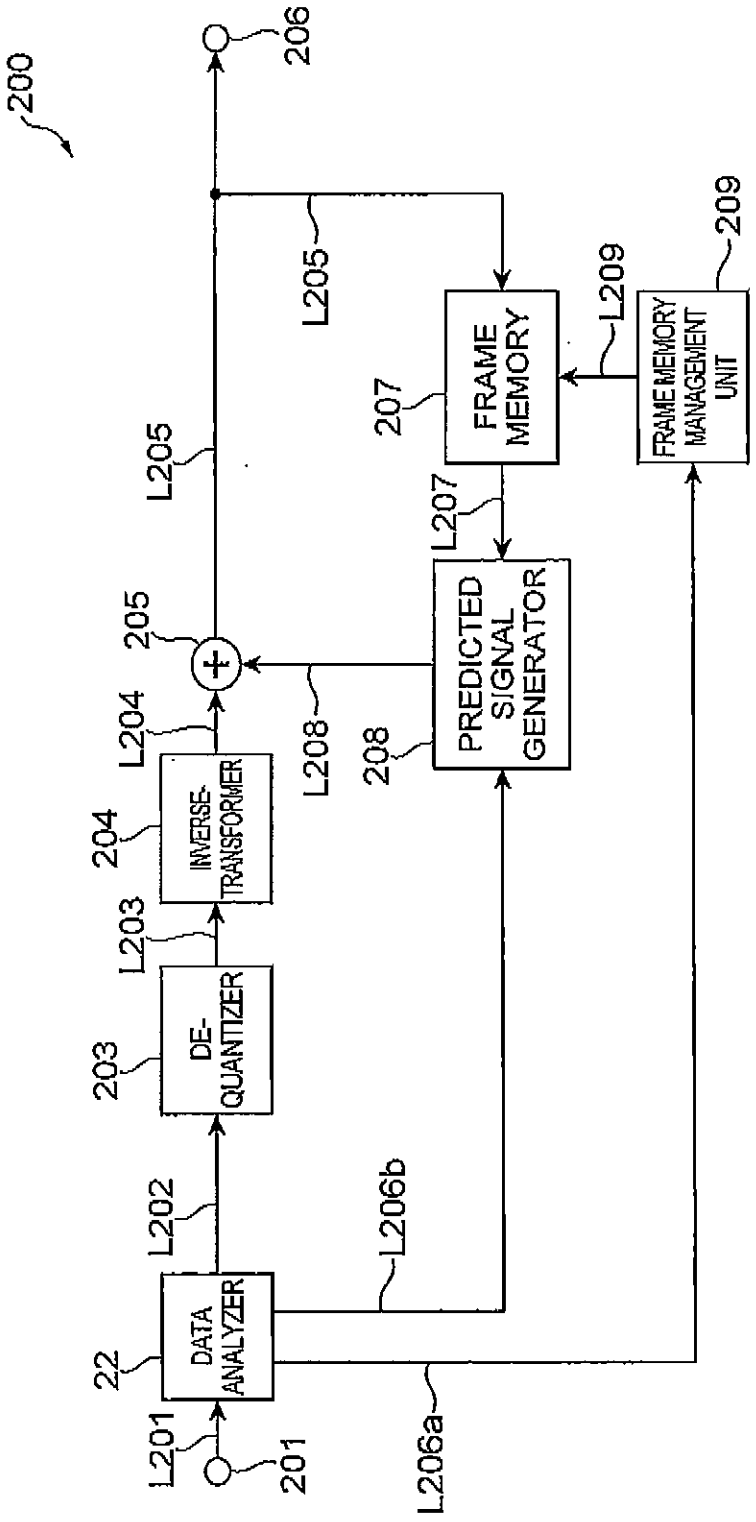

200
206
L205
209
L209
FRAME MEMORY MANAGEMENT UNIT
207
FRAME MEMORY
L205
L207
205
PREDICTED SIGNAL GENERATOR
L204
L208
208
204
INVERSE-TRANSFORMER
L203
203
DE-QUANTIZER
L202
L206b
22
DATA ANALYZER
L201
201
L206a

Fig.2

Fig.3

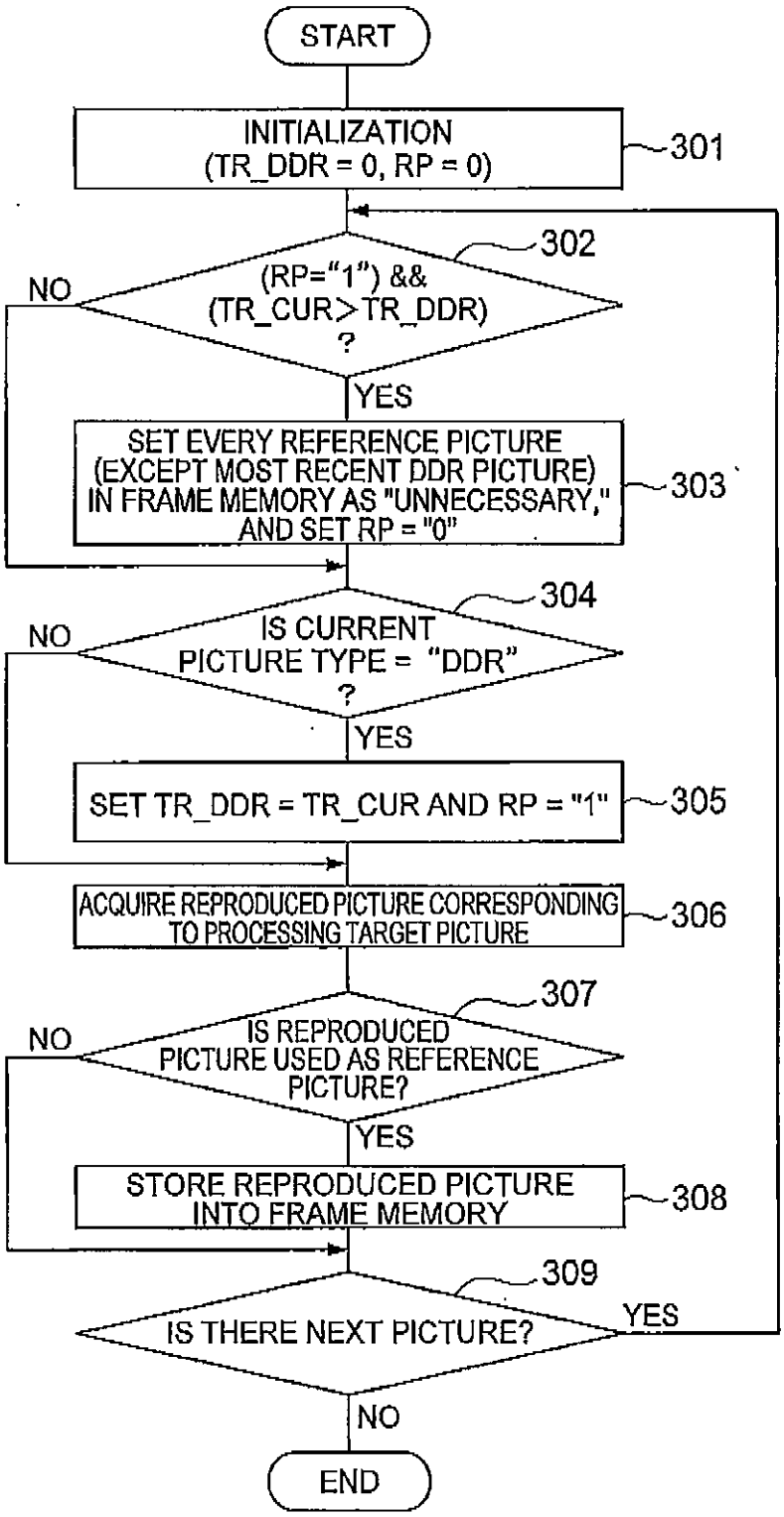

START
INITIALIZATION
(TR_DDR = 0, RP = 0)
301
302
(RP="1") &&
(TR_CUR>TR_DDR)
?
NO
YES
SET EVERY REFERENCE PICTURE
(EXCEPT MOST RECENT DDR PICTURE)
IN FRAME MEMORY AS "UNNECESSARY,"
AND SET RP = "0"
303
304
IS CURRENT
PICTURE TYPE = "DDR"
?
NO
YES
SET TR_DDR = TR_CUR AND RP = "1"
305
ACQUIRE REPRODUCED PICTURE CORRESPONDING
TO PROCESSING TARGET PICTURE
306
307
IS REPRODUCED
PICTURE USED AS REFERENCE
PICTURE?
NO
YES
STORE REPRODUCED PICTURE
INTO FRAME MEMORY
308
309
IS THERE NEXT PICTURE?
YES
NO
END

Fig.4

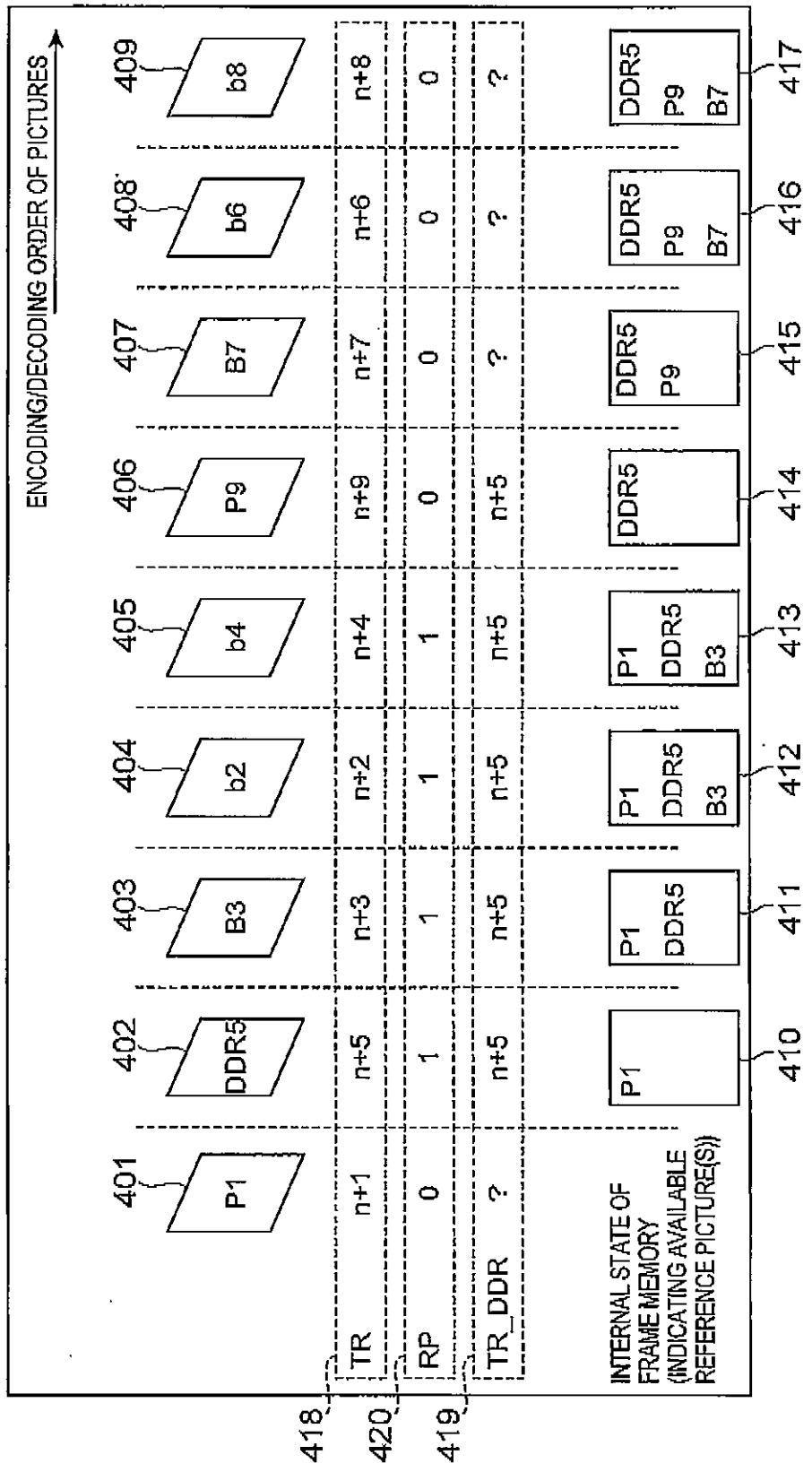

ENCODING/DECODING ORDER OF PICTURES
401
P1
402
DDR5
403
B3
404
b2
405
b4
406
P9
407
B7
408
b6
409
b8
TR
n+1
n+5
n+3
n+2
n+4
n+9
n+7
n+6
n+8
RP
0
1
1
1
1
0
0
0
0
TR_DDR
?
n+5
n+5
n+5
n+5
n+5
?
?
?
INTERNAL STATE OF FRAME MEMORY (INDICATING AVAILABLE REFERENCE PICTURE(S))
P1
P1 DDR5
P1 DDR5 B3
P1 DDR5 B3
DDR5
DDR5 P9
DDR5 P9 B7
DDR5 P9 B7
410
411
412
413
414
415
416
417
418
420
419

Fig.5

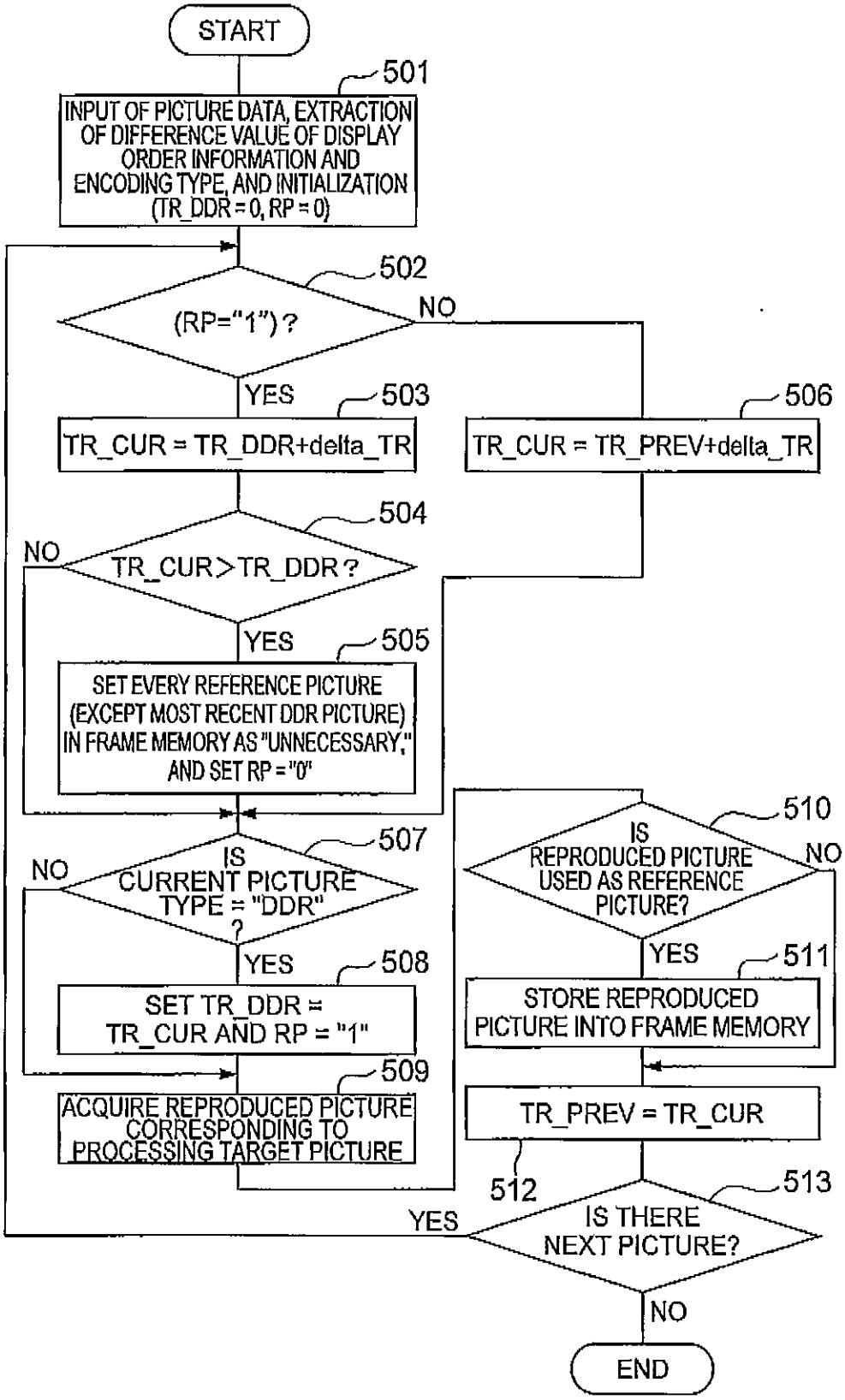

START
501
INPUT OF PICTURE DATA, EXTRACTION OF DIFFERENCE VALUE OF DISPLAY ORDER INFORMATION AND ENCODING TYPE, AND INITIALIZATION (TR_DDR = 0, RP = 0)
502
(RP="1")?
NO
YES
503
TR_CUR = TR_DDR+delta_TR
506
TR_CUR = TR_PREV+delta_TR
504
NO
TR_CUR>TR_DDR?
YES
505
SET EVERY REFERENCE PICTURE (EXCEPT MOST RECENT DDR PICTURE) IN FRAME MEMORY AS "UNNECESSARY," AND SET RP = "0"
507
NO
IS CURRENT PICTURE TYPE = "DDR" ?
YES
508
SET TR_DDR = TR_CUR AND RP = "1"
509
ACQUIRE REPRODUCED PICTURE CORRESPONDING TO PROCESSING TARGET PICTURE
510
IS REPRODUCED PICTURE USED AS REFERENCE PICTURE?
NO
YES
511
STORE REPRODUCED PICTURE INTO FRAME MEMORY
TR_PREV = TR_CUR
512
513
YES
IS THERE NEXT PICTURE?
NO
END

Fig.6

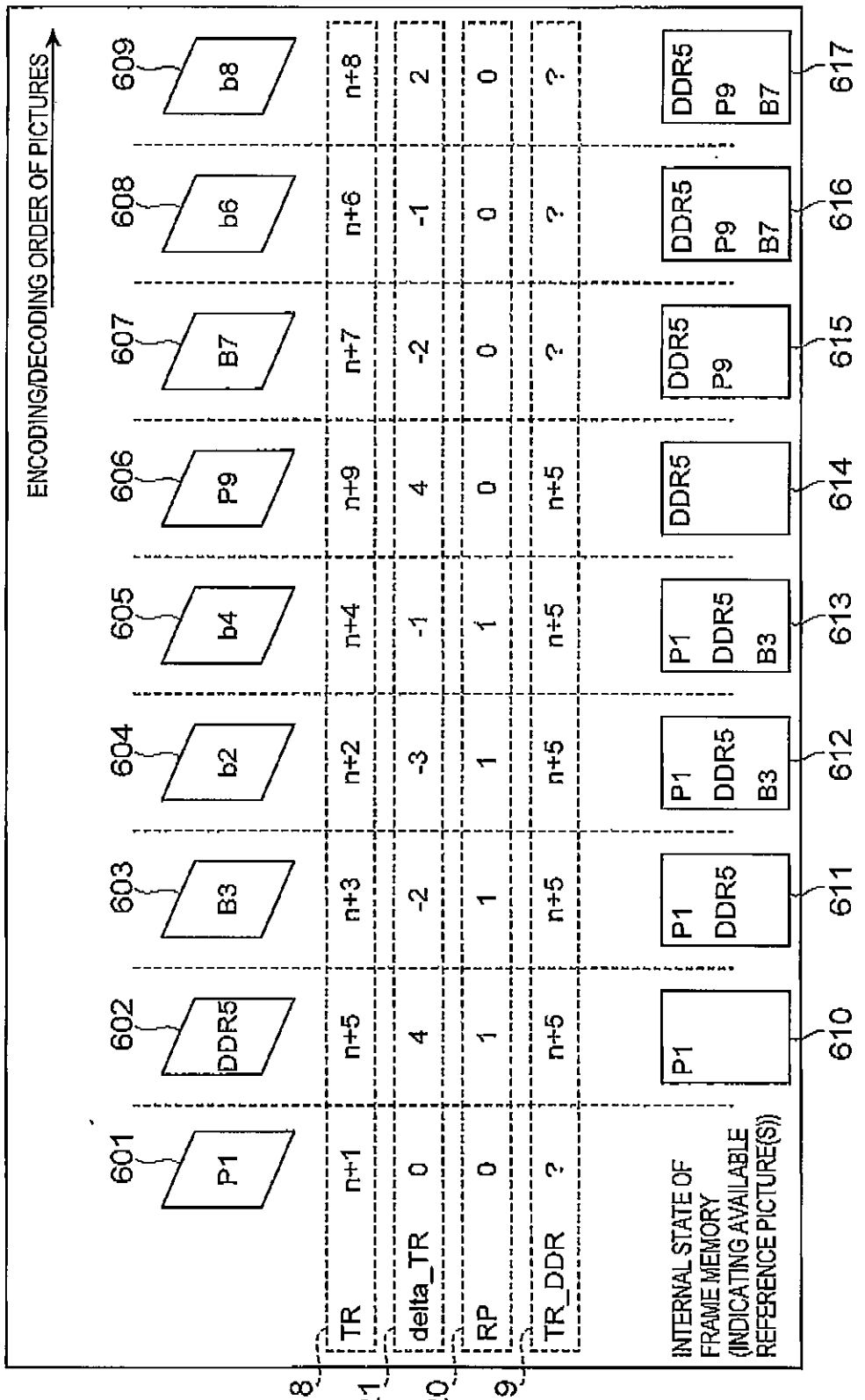

ENCODING/DECODING ORDER OF PICTURES
601
602
603
604
605
606
607
608
609
P1
DDR5
B3
b2
b4
P9
B7
b6
b8
618
TR
n+1
n+5
n+3
n+2
n+4
n+9
n+7
n+6
n+8
621
delta_TR
0
4
-2
-3
-1
4
-2
-1
2
620
RP
0
1
1
1
1
0
0
0
0
619
TR_DDR
?
n+5
n+5
n+5
n+5
n+5
?
?
?
INTERNAL STATE OF FRAME MEMORY (INDICATING AVAILABLE REFERENCE PICTURE(S))
P1
P1 DDR5
P1 DDR5 B3
P1 DDR5 B3
DDR5
DDR5 P9
DDR5 P9 B7
DDR5 P9 B7
610
611
612
613
614
615
616
617

Fig.7

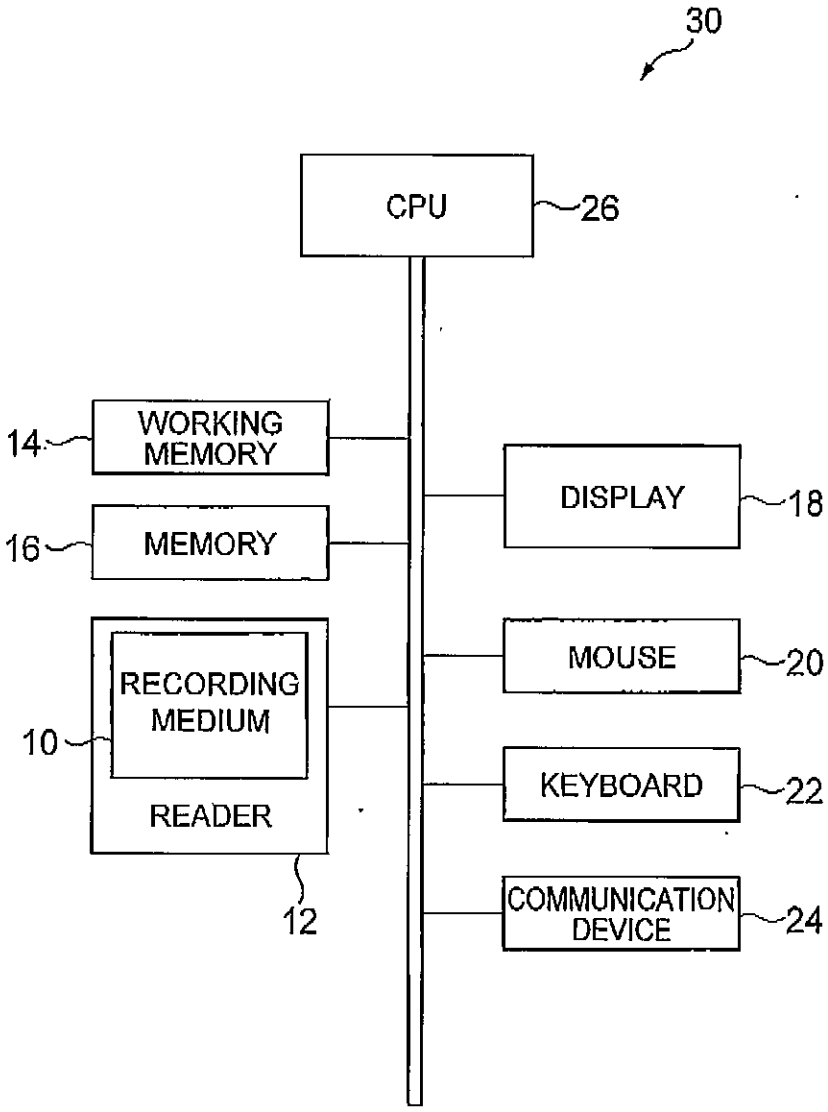

30
CPU
26
14
WORKING MEMORY
16
MEMORY
10
RECORDING MEDIUM
READER
12
DISPLAY
18
MOUSE
20
KEYBOARD
22
COMMUNICATION DEVICE
24

Fig.8

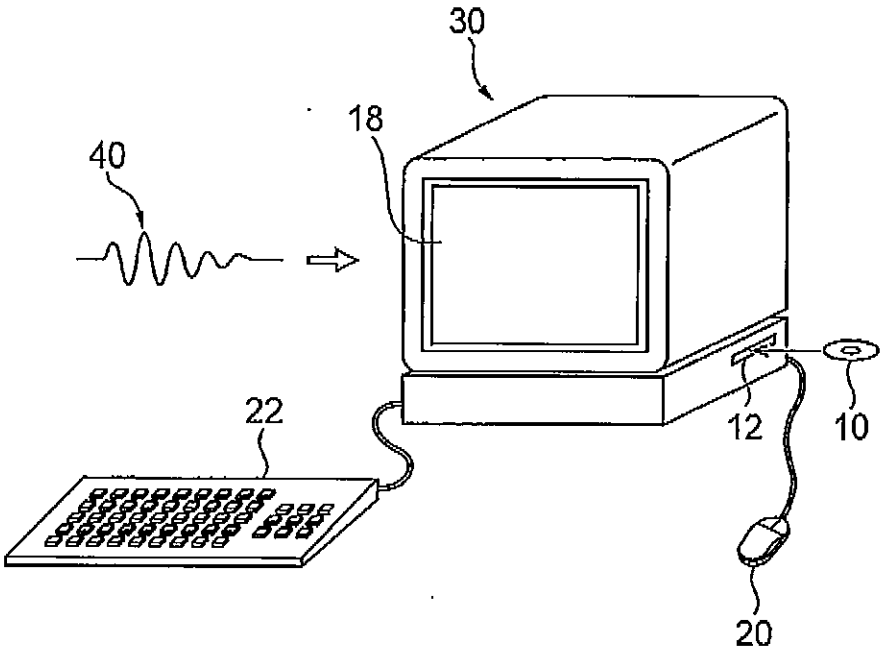


Fig.9

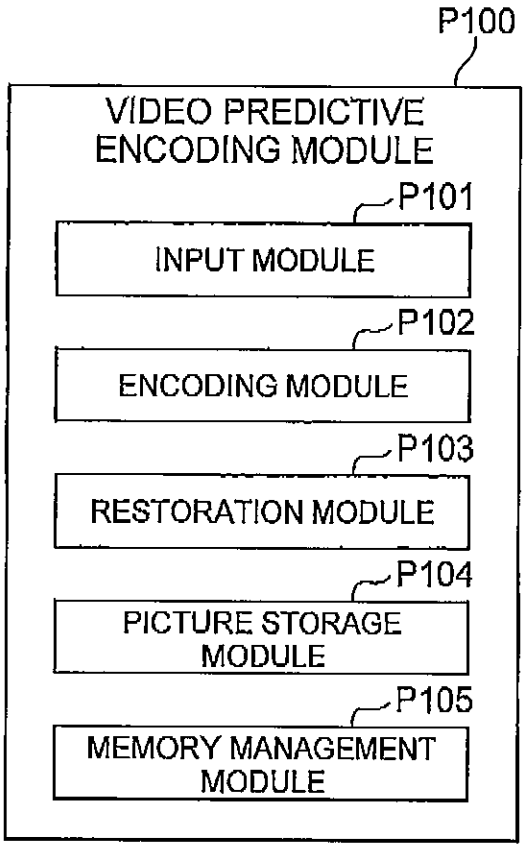

P100
VIDEO PREDICTIVE ENCODING MODULE
P101
INPUT MODULE
P102
ENCODING MODULE
P103
RESTORATION MODULE
P104
PICTURE STORAGE MODULE
P105
MEMORY MANAGEMENT MODULE

Fig.10

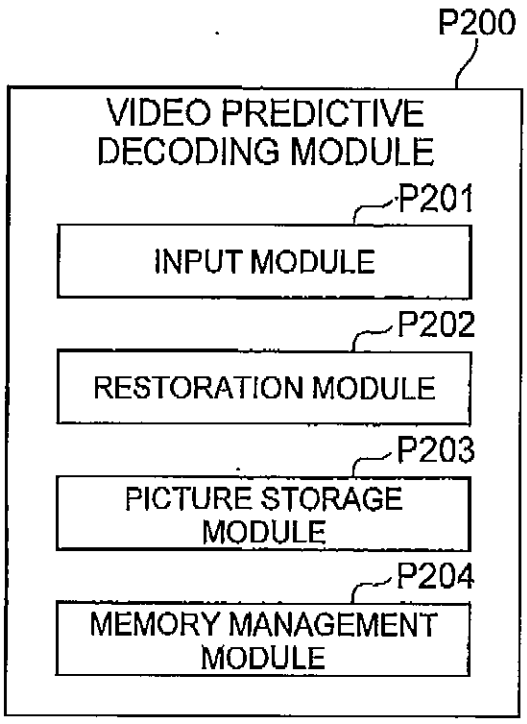
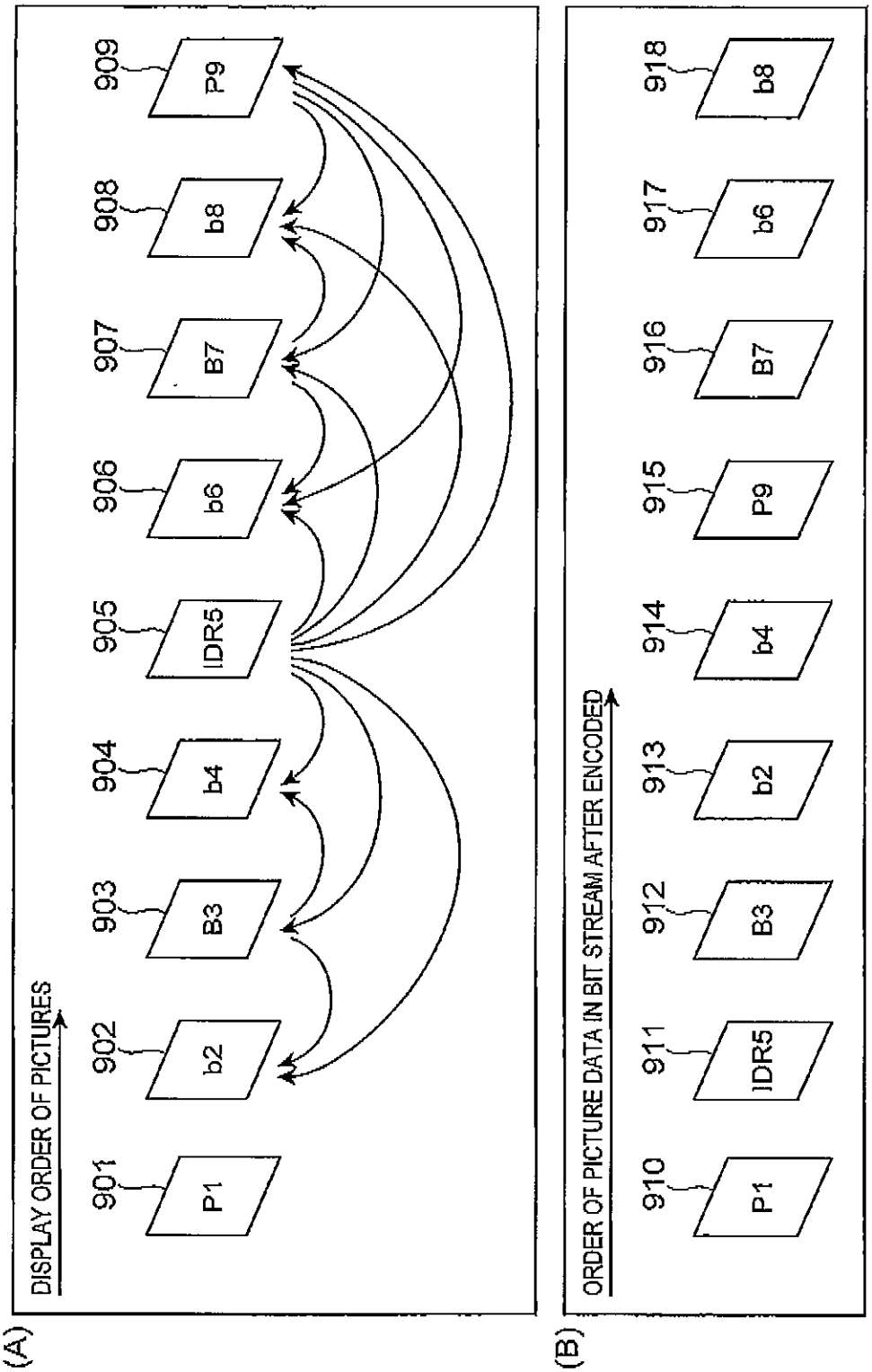

P200
VIDEO PREDICTIVE DECODING MODULE
P201
INPUT MODULE
P202
RESTORATION MODULE
P203
PICTURE STORAGE MODULE
P204
MEMORY MANAGEMENT MODULE

Fig.11


(A)
DISPLAY ORDER OF PICTURES
901
P1
902
b2
903
B3
904
b4
905
IDR5
906
b6
907
B7
908
b8
909
P9
(B)
ORDER OF PICTURE DATA IN BIT STREAM AFTER ENCODED
910
P1
911
IDR5
912
B3
913
b2
914
b4
915
P9
916
B7
917
b6
918
b8