SHALLOW TRENCH ISOLATION PROCESS AND STRUCTURE

FIELD OF THE INVENTION

The present invention is related to integrated circuit (IC) devices and to processes of making IC devices. More particularly, the present invention relates to a method of forming trench isolation structures on substrates or layers including strained layers such as strained silicon.

BACKGROUND OF THE INVENTION

Integrated circuits (ICs) include a multitude of transistors formed on a semiconductor substrate. Various methods of forming transistors are known in the art. Generally, transistors are isolated from each other by insulating or isolation structures.

One method of forming transistors on a silicon substrate involves the well-known Local Oxidation of Silicon (LOCOS) process. A conventional LOCOS process typically includes the following simplified steps. First, a silicon nitride layer is thermally grown on the silicon substrate. Generally, conventional LOCOS processes require a high quality, thermally grown silicon nitride layer to avoid delamination and other processing problems. Next, using a lithography and etch process, the nitride layer is selectively removed to produce a pattern where transistor source/drain areas are to be located. After patterning the source/drain areas, a field oxide is grown. As oxide growth is inhibited where the nitride layer still remains, the field oxide only grows on the silicon substrate exposed during the source/drain patterning step. Finally, after oxide growth is complete, the remaining portions of the nitride layer are removed, leaving only the oxidized source/drain areas on the exposed silicon substrate.

Another process for forming insulating structures and defining source and drain regions is a shallow trench isolation (STI) process. A conventional STI process typically includes the following simplified steps. First, a silicon nitride layer is thermally grown or deposited onto the silicon substrate. Next, using a lithography and etch process, the silicon nitride layer is selectively removed to produce a pattern where transistor source/drain areas are to be located. After patterning the source/drain areas, the substrate is etched to form trenches. After the trenches are formed, a liner is thermally grown on the exposed surfaces of the trench. The liner oxide is typically formed at a very high temperature in a hydrochloric (HCl) acid ambient. An insulative material such as silicon dioxide (SiO_2) is blanket deposited over the nitride layer and the liner oxide within the trench. The insulative material is polished to create a planar surface. The nitride layer is subsequently removed to leave the oxide structures within the trenches.

Shallow trench isolation (STI) structures are utilized in strained silicon (SMOS) processes. SMOS processes are utilized to increase transistor (MOSFET) performance by increasing the carrier mobility of silicon, thereby reducing resistance and power consumption and increasing drive current, frequency response, and operating speed. Strained silicon is typically formed by growing a layer of silicon on a silicon-germanium substrate or layer.

The silicon-germanium lattice associated with the silicon-germanium substrate is generally more widely spaced than a pure silicon lattice, with spacing becoming wider with a higher percentage of germanium. Because the silicon lattice aligns with the larger silicon-germanium lattice, a tensile strain is created in the silicon layer. The silicon atoms are essentially pulled apart from one another.

Relaxed or non-strained silicon has a conductive band that contains six equal valence bands. The application of tensile strain to the silicon causes four of the valence bands to increase in energy and two of the valence bands to decrease in energy. As a result of quantum effects, electrons effectively weigh 30 percent less when passing through the lower energy bands. Thus, the lower energy bands offer less resistance to electron flow. In addition, electrons meet with less vibrational energy from the nucleus of the silicon atom, which causes them to scatter at a rate of 500 to 1000 times less than in relaxed silicon. As a result, carrier mobility is dramatically increased in strained silicon compared to relaxed silicon, providing an increase in mobility of 80% or more for electrons and 20% or more for holes. The increase in mobility has been found to persist for current fields up to 1.5 megavolts/centimeter. These factors are believed to enable a device speed increase of 35% without further reduction of device size, or a 25% reduction in power consumption without a reduction in performance.

In conventional SMOS processes, a strained silicon layer is provided over a silicon-germanium layer and etched to form trenches for the STI structure. The trenches extend through the strained silicon layer and at least partially into the silicon-germanium layer. A conventional STI liner oxide process is utilized to grow a trench liner. The conventional STI liner oxide process can utilize very high temperatures and HCl ambient environments. During this process, germanium outgassing is enhanced, which can negatively impact the formation of thin films, can contaminate IC structures, layers and equipment, and can cause germanium accumulation or "pile-up" at the interface of the liner, thereby causing reliability issues for the STI structure.

In conventional SMOS processes, the STI structure can be subject to silicon overhang at the edge of the STI structure because the silicon-germanium layer is more readily etched than the strained silicon layer. Further, the strained silicon layer is more easily consumed than the silicon-germanium layer during trench liner and filling processes. In addition, conventional SMOS STI trenches can be subject to STI sidewall leakage.

Thus, there is a need for an STI structure which can be formed without damaging strained materials or layers. Further still, there is a need for a process of forming high quality oxides with good compatibility that are not susceptible to problems associated with strained materials. Further still, there is a need for an improved SMOS trench formation process that is not susceptible to silicon overhang. Yet further, there is a need for a liner formation process that is less susceptible to germanium outgassing. Further, there is a need for an STI process that is less susceptible to at least one of strained silicon consummation, STI sidewall leakage, and silicon overhang.

SUMMARY OF THE INVENTION

An exemplary embodiment relates to a method of manufacturing an integrated circuit having trench isolation regions in a substrate including a first layer. The method includes selectively etching the first layer to form apertures associated with locations of the trench isolation regions and forming strained semiconductor material above the first layer. The method also includes forming insulative material in the apertures to form the trench isolation regions.

Another exemplary embodiment relates to a method of forming shallow trench isolation structures in a compound semiconductor layer above a buried oxide (BOX) layer. The method includes providing a hard mask layer above the compound semiconductor layer, removing the hard mask layer at locations, and forming trenches in the compound semiconductor layer under the locations. The method also includes stripping the hard mask layer, forming a strained semiconductor layer above the compound semiconductor layer, and providing isolation material in the trenches to form the shallow trench isolation structures.

Still another exemplary embodiment relates to an integrated circuit. The integrated circuit includes a compound semiconductor layer, a box layer beneath the compound semiconductor layer, a strained semiconductor layer, and isolation trenches. The strained semiconductor layer is above the compound semiconductor layer. The isolation trenches are disposed in the compound semiconductor layer. The isolation trenches include insulative material and sidewalls of the isolation trenches are at least partially covered by the strained semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments will become more fully understood from the following detailed description, taken in conjunction with the accompanying drawings, wherein like reference numerals refer to like parts, and wherein:

FIGURE 1 is a schematic cross-sectional view of a portion of a semiconductor-on-insulator (SOI) substrate including an oxide layer, a hard mask layer, and a photoresist layer for use with exemplary embodiments of the shallow trench isolation (STI) processes illustrated in FIGURES 10 and 15;

FIGURE 2 is a cross-sectional view of the portion illustrated in FIGURE 1, showing a lithographic patterning step;

FIGURE 3 is a cross-sectional view of the portion illustrated in FIGURE 2, showing a selective etching step for the hard mask layer;

FIGURE 4 is a cross-sectional view of the portion illustrated in FIGURE 3, showing a selective etching step for the oxide layer;

FIGURE 5 is a cross-sectional view of the portion illustrated in FIGURE 4, showing a selective etching step for a compound semiconductor layer associated with the SOI substrate;

FIGURE 6 is a cross-sectional view of the portion illustrated in FIGURE 5, showing a removal step for the hard mask layer and the oxide layer;

FIGURE 7 is a cross-sectional view of the portion illustrated in FIGURE 6, showing a strained semiconductor formation step;

FIGURE 8 is a cross-sectional view of the portion illustrated in FIGURE 7, showing a trench fill step;

FIGURE 9 is a cross-sectional view of the portion illustrated in FIGURE 7, showing a gate formation and silicidation step;

FIGURE 10 is a general block diagram showing a shallow trench isolation process for the portion illustrated in FIGURES 1-9;

FIGURE 11 is a cross-sectional view of a portion of a semiconductor-on-insulator substrate for use with exemplary embodiments of the shallow trench insulation (STI) process illustrated in FIGURE 15, showing oxide and hard mask removal steps;

FIGURE 12 is a cross-sectional view of the portion illustrated in FIGURE 11, showing a trench fill step;

FIGURE 13 is a cross-sectional view of the portion illustrated in FIGURE 12, showing a strained silicon formation step;

FIGURE 14 is cross-sectional view of the portion illustrated in FIGURE 13, showing a gate formation and silicidation step; and

FIGURE 15 is a general block diagram showing a shallow trench isolation process for the portion illustrated in FIGURES 1-5 and 11-14.

DETAILED DESCRIPTION OF REFERRED EXEMPLARY EMBODIMENTS

FIGURES 1 through 15 illustrate methods of manufacturing an integrated circuit (IC) in accordance with an exemplary embodiment. Advantageously, process 100 (FIGURE 10) and process 200 (FIGURE 15) do not provide the strained silicon material until after the trenches are formed in an underlying layer. In this way, problems associated with silicon overhang at the STI edge, strained silicon consumption for formation of the STI structure, and STI structure sidewall leakage are reduced. The strained material can be provided according to a variety of processes after trenches are formed in the underlying layer.

The embodiments of the method (process 100) illustrated in FIGURES 1 through 9 reduce germanium outgassing and outdiffusion problems associated with silicon-germanium layers. Process 100 utilizes a strained silicon layer on sidewalls at the STI trench.

Processes 100 and 200 can be used in a shallow trench isolation (STI) process or any process requiring trench isolation and utilizing germanium or other substances prone to outgassing at high temperatures. Advantageously, a liner oxide layer can be formed at a relatively low temperature and yet still provide a high quality oxide with good compatibility. A low temperature process refers to a process performed at a temperature of less than approximately 750°C (e.g., at or below 700°C).

Referring to FIGURES 1 through 10, a cross-sectional view of a portion 12 of an integrated circuit (IC) is illustrated. Portion 12 is subjected to process 100 (FIGURE 10) to form a shallow trench isolation (STI) structure. Portion 12 includes an oxide layer 18 provided over a substrate 15. Substrate 15 includes a compound semiconductor layer 16 (e.g. silicon-germanium) provided over a buried oxide (BOX) layer 14 and a base layer 13. Substrate 15 is preferably a semiconductor-on-insulator (SOI) substrate including layer 16.

Base layer 13 is optional and portion 12 can be provided with BOX layer 14 as the bottom-most layer. Base layer 13 of substrate 15 can be the same material or a different material than layer 16. In one embodiment, base layer 13 is a semiconductor substrate such as a silicon substrate upon which layer 14 has been grown or deposited as a silicon dioxide layer. Layer 16 is grown or deposited physically above layer 14. Layer 16 is not necessarily directly deposited above layer 14. Alternatively, substrate 15 can be purchased from a wafer supplier.

Portion 12 can be any type of semiconductor device, or portion thereof, and may be made from any of a variety of semiconductor processes, such as a complementary metal oxide semiconductor (CMOS) process, bipolar process, or other semiconductor process. Portion 12 may be an entire IC or a portion of an IC and may include a multitude of electronic component portions.

Layer 16 is preferably a silicon-germanium or other semiconductor material including germanium, and can be doped with P-type dopants or N-type dopants. Layer 16 can be an epitaxial layer provided on a semiconductor or an insulative base such as layer 14. Furthermore, layer 16 is preferably a composition of silicon and germanium (Si_{1-X} Ge_X, where X is approximately 0.2 and is more generally in the range of 0.1-0.3).

Layer 14 can be grown, deposited, or formed by ion implantation above base layer 13. Layer 14 is preferably between approximately 200 and 2000 Å thick. According to alternative embodiments, layer 14 may have a thickness of between approximately 500 and 2000°, (e.g., if layer 14 is a SIMOX layer, oxygen implantation into silicon).

In one embodiment, layer 16 is grown above base layer 13 by chemical vapor deposition (CVD) using disilane (Si_2H_6) and germane (GeH_4) as source gases with a substrate temperature of 650°C, a disilane partial pressure of 30 mPa, and a germane partial pressure of 60 mPa. Growth of silicon-germanium material may be initiated using these ratios, or alternatively, the partial pressure of germanium may be gradually increased beginning from a lower pressure or zero pressure to form a gradient composition. Alternatively, a silicon layer can be doped by ion implantation with germanium or other processes can be utilized to form layer

16. Preferably, layer 16 is grown by epitaxy to a thickness of less than approximately 2 microns (and preferably between approximately .5 microns and 2 microns.

Pad oxide film or oxide layer 18 is provided above layer 16. Layer 18 is optional. Layer 18 is preferably thermally grown on layer 16 to a thickness of between approximately 100 and 300 Å. Layer 18 serves as a buffer layer and can be thermally grown in a conventional high temperature process by heating to approximately 1000°C in an oxygen-containing atmosphere.

A barrier or hard mask layer 22 is provided over oxide layer 18. Preferably, mask layer 22 is silicon nitride (Si_3N_4) provided at a thickness of between approximately 300 and 1000 Å by a deposition, CVD, or thermal growth process. A low pressure, plasma enhanced chemical vapor deposition (PECVD) process can also be utilized. A conventional thermal nitride process using a dichlorosilane (SiH_2Cl_2), ammonia (NH_3) and nitrogen (N_2) mixture at a high temperature (e.g., 600°C or above) can be used. The PECVD process for depositing nitride uses silane (SiH_4), nitrogen (N_2), and ammonia (NH_3) with a power of between approximately 550 and 650 watts at 400°C. An ammonia (NH_3) silane (SiH_4/N_2) mixture plasma, as opposed to a $N_2/NH_3/SiCl_2H_2$ associated with conventional CVD or growth process, can be used to form mask layer 22.

A photoresist layer 24 is provided (e.g., by spin-coating) above mask layer 22. Preferably, photoresist layer 24 is any commercially available i-line or deep UV photoresist such as (Shipley Corp., MA) SPR 955 (i-line) UV5 (deep UV). In FIGURES 1-2, photoresist layer 24 is selectively removed via a photolithographic process using a mask or reticle 28 to leave apertures 34 in accordance with a step 102 (FIGURE 10) of process 100.

In FIGURE 3, mask layer 22 is preferably a hard mask and is etched via a dry-etching process so that apertures 34 reach oxide layer 18 in accordance with a step 104 of process 100 (FIGURE 10). The dry-etching process is selective to silicon nitride with respect to oxide layer 18. Layer 24 can be stripped after layer 22 is etched.

In FIGURE 4, the etch process is changed to etch through silicon dioxide material and layer 18 is etched so that apertures 34 reach layer 16 in accordance with step 104 of process 100 (FIGURE 10). Layer 18 can be etched in a dry etching process. Alternatively, other etching techniques can be utilized to remove selected portions of layer 18. Photoresist layer 24 (FIGURE 1) can be removed before or after oxide layer 18 is etched. Layer 22 can also be removed after layer 18 is etched.

In FIGURE 5, the etch process is changed to etch through the compound semiconductor material of layer 16. Layer 16 can be removed in accordance with a dry-etching process so that apertures 34 reach a top of layer 14. Apertures 34 can be any width suitable for STI structures. In one embodiment, apertures 34 are preferably between approximately 150nm and 300 nm wide depending upon technology. Layer 16 is etched through apertures 34 to form trenches for shallow trench isolation structures in accordance with step 104 of process 100 (FIGURE 10). The trenches preferably have a width corresponding to apertures 34. The trenches preferably have a depth of between approximately 500 and 300Å (depending on thickness of layer 16) and width of 150-300nm. The trenches can have a trapezoidal cross-sectional shape with the narrower portion

being at the bottom. An alternative embodiment includes trenches having a more rectangular cross-sectional shape.

Although described as being etched in a dry etching process, the trenches can be formed in any process suitable for providing apertures in layer 16. In one embodiment, the apertures for the trenches are provided all the way into layer 14. Alternatively, the bottom of the trenches associated with apertures 34 may not reach layer 14, depending upon the thickness of layer 16.

In FIGURE 6, layers 18 and 22 are removed (e.g., stripped). Layers 18 and 22 can be removed using any conventional process. In FIGURE 7, strained semiconductor material 36 is provided above layer 16 in accordance with a step 106 of process 100 (FIGURE 10). Layer 36 preferably has a thickness of between 100 and 200 Å and is a tensile-strained silicon layer. Layer 36 can be formed by chemical vapor deposition CVD using silane, disilane or dichlorosilane at a temperature of 500° to 650°C or by molecular beam epitaxy (MBE).

In one preferred embodiment, sidewalls of the trenches associated with apertures 34 are covered with layer 36. Advantageously, layer 36 can prevent germanium diffusion associated with the STI trench process because it covers compound semiconductor layer 16. Layer 36 can be deposited by a number of processes including CVD and MBE and may have a variety of dimensions.

Liners (not shown) can be formed in the trenches associated with apertures 34 after layer 36 is provided. Preferably, the liners are oxide (e.g., silicon oxide or silicon dioxide) material formed in a low temperature process. In one embodiment, liners are between approximately 50 and 200 Å thick and are provided over the bottom and sidewalls of the trench.

In another embodiment, the liners can be formed in a plasma enhanced low pressure chemical vapor deposition (LPCVD) process or high density plasma oxide deposition (HDP) process similar to the CVD process discussed above. Preferably, the deposition processes do not utilize NH_3, instead utilizing silane at a temperature below 700°C.

In FIGURE 8, a layer of insulative material 42 is blanket deposited over material 36 and within the trenches associated with apertures 34 in accordance with a step 108 of process 100. Insulative material 42 is preferably silicon dioxide deposited in a CVD process. Preferably, insulative material 42 is deposited in a tetraethylorthosilicate (TEOS) process. Alternatively, a boron phosphate silicon glass (BPSG) process can be utilized. Insulative material 42 is preferably between approximately 2000 and 8000 Å thick.

Insulative material 42 is removed by polishing and/or etching until a top surface of material 36 is reached. The removal of insulative material 42 leaves insulative material within the trenches associated with apertures 34. Insulative material 42 can be removed by a number of stripping or etching processes. Preferably, insulative material 42 is removed from above material 36 by dry-etching.

After insulative material 42 is provided in the trenches associated with apertures 34, a gate structure 48 can be provided. Gate structure 48 can be a conventional MOSFET gate structure such as a metal over oxide gate structure or polysilicon over oxide gate structure.

Silicidation is utilized to form silicide layers 46 at locations of the source and drain of the transistor associated with gate structure 48. Layers 46 can be formed by a conventional germano-silicidation process using nickel.

With reference to FIGURES 1-5 and 11-15, process 200 is similar to process 100. Process 200 follows essentially the same steps associated with process 100 described with reference to FIGURES 1-5. In process 200, photoresist layer 24 is patterned above compound semiconductor layer 16 at a step 202 and the compound semiconductor layer is etched to form a trench at a step 204 (see FIGURES 1-5).

With reference to FIGURE 11, apertures 134 in layer 16 can be slightly smaller than apertures 34 discussed with reference to FIGURES 2-9. Preferably, apertures 134 are between approximately 150 and 300nm wide and have a similar depth to the depth of apertures 34 discussed above. A mask layer 118 (e.g., an oxide or nitride mask layer such as that described with respect to layers 18 and 22 described above) is provided over layer 16. The mask layer 118 has a thickness that is substantially similar to a strained material 136 (FIGURE 13) that will be provided subsequently.

As shown in FIGURE 12, in a step 207 of process 200, the trenches associated with apertures 134 are filled with insulative material 142. Insulative material 142 can be similar to insulative material 42 discussed with reference to FIGURE 8. The trenches associated with apertures 134 can be filled in a variety of processes, including the processes described above with reference to filling the trenches associated with apertures 34. The insulative material fills the trench to an upper surface of mask layer 118. According to an exemplary embodiment, the insulative material is also provided over the surface of mask layer 118 and polished or etched back to the surface of mask layer 118.

As shown in FIGURE 13, in a step 209 of process 200, the mask layer 118 is removed and a strained material 136 is grown by selective silicon epitaxy above layer 16. Because the thickness of layers 118 and 136 are substantially similar, the insulative material 142 extends to an upper surface of the strained material 136. Unlike the embodiment of process 100 discussed with reference to FIGURES 1-10, material 136 is not provided on sidewalls associated with the trench.

With reference to FIGURE 14, a gate structure 48 is provided and silicide layer 46 is provided at the locations associated with the source and drain of the transistor associated with gate structure 48. Gate structure 48 is formed in a step 212 and a silicide layer 46 is formed in a step 213.

It should be understood that while the detailed drawings, specific examples, and particular values given provide a preferred exemplary embodiment of the present invention, it is for the purpose of illustration only. The shapes and sizes of trenches are not disclosed in a limiting fashion. The method and apparatus of the invention is not limited to the precise details and conditions disclosed. Various changes may be made to

the details disclosed without departing from the scope of the invention, which is defined by the following claims.

CLAIMS:

1. A method of manufacturing an integrated circuit having trench isolation regions in a substrate (15) including a first layer (16), the method comprising:

selectively etching the first layer (16) to form apertures (34) associated with locations of the trench isolation regions;

forming strained semiconductor material (36) above the first layer (16) after selectively etching the first layer (16) to form apertures (34); and

forming insulative material (42) in the apertures (34) after forming strained semiconductor material (36) above the first layer (16) to form the trench isolation regions.

2. The method of claim 1, wherein the strained semiconductor material (36) is formed on sidewalls of the apertures (34).

3. The method of claim 1, wherein the strained semiconductor material (36) is silicon and the first layer (16) is silicon-germanium.

4. The method of claim 1, wherein the first layer is above a BOX layer (14).

5. A method of forming shallow trench isolation structures in a compound semiconductor layer (16) above a buried oxide (BOX) layer (14), the method comprising:

providing a hard mask layer (22) above the compound semiconductor layer (16);

removing the hard mask layer (22) at locations;

forming trenches (34) in the compound semiconductor layer (16) under the locations;

stripping the hard mask layer (22);

forming a strained semiconductor layer (36) above the compound semiconductor layer (16) after the step of forming trenches (34); and

providing isolation material (42) in the trenches (34) after forming the strained semiconductor layer (36) to form the shallow trench isolation structures.

6. The method of claim 5, further comprising providing a silicide layer (46) above the strained semiconductor layer (36).

7. The method of claim 5, further comprising providing a liner in the trenches (34) at low temperature below 750°C, after forming strained semiconductor layer (36).

8. An integrated circuit, comprising:

a compound semiconductor layer (16);

a buried oxide (BOX) layer (14) beneath the compound semiconductor layer (16);

a strained semiconductor layer (36) above the compound semiconductor layer (16); and

isolation trenches (34) disposed in the compound semiconductor layer (16), wherein the isolation trenches (34) include insulative material (42) and sidewalls, the sidewalls of the isolation trenches (34) are at least partially covered by the strained semiconductor layer (36).

9. The integrated circuit of claim 8, further comprising a gate structure (48) between the isolation trenches (34).

10. The integrated circuit of claim 8, wherein the strained semiconductor layer (36) comprises silicon and the compound semiconductor layer comprises silicon-germanium and the trenches (34) extend from the strained semiconductor layer (36) at a top to the buried oxide layer (14) at a bottom.