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(54) Title: MULTIPORTED BYPASS CACHE ✓

(57) Abstract

A microprocessor (80) includes a register file (84) that contains registers for storing pieces of data for use by execution units (ALU0, ALU1) that receive the pieces of data through source ports. A bypass cache (130) includes data registers (D1, D2, D3, D4) into which pieces of data from the execution units are written. Data can be written to and read from the bypass cache (130) in fewer clock cycles than it can be written to and read from the register file (84). A content addressable memory array (CAM) (128) includes address registers (A1, A2, A3, A4) into which destination addresses are written which correspond to the pieces of data in the data registers (D1, D2, D3, D4). In the case of a particular piece of data, the particular data register into which the piece of data is written and the particular address register into which the corresponding destination address is written is controlled by the position of a write pointer provided by a rotating write pointer unit (132). The CAM (128) includes comparators (160, 162, 164, 166) that compare the destination address with a source address. If there is a match, a read port is enabled which provides the piece of data in the corresponding data register to conductors leading to the source port. Multiplexers (186, 188, 190, 192, 194, 196) select between pieces of data in the register file (84) and pieces of data in the data registers (D1, D2, D3, D4) of the bypass cache (130).

