

PHASE CHANGE MEMORY HAVING GRADUAL RESET

BACKGROUND

[0001] The present invention relates generally to the electrical, electronic and computer arts, and, more particularly, to phase change memory.

[0002] Phase change memory (PCM) is a form of random-access memory (RAM) that stores data by altering a state of the matter from which the device is fabricated. At the heart of a PCM cell is a small region of a semiconductor alloy (e.g., chalcogenide) that can be changed rapidly between an ordered, crystalline phase having lower electrical resistance and a disordered, amorphous phase having much higher electrical resistance. This change in resistance between the crystalline and amorphous phases, and thus a logical state of the PCM cell, is easily discernible. Because no electrical power is required to maintain either phase of the material, phase-change memory is non-volatile.

[0003] A state (i.e., phase) of the phase change material forming the PCM cell is set (i.e., written) as a function of an amplitude and duration of an applied electrical pulse that heats the material. When heated to a temperature just above its melting point (e.g., over about 600 degrees Celsius), the semiconductor alloy's energized atoms move around into random arrangements. Turning off the applied electrical pulse gradually (e.g., over about 10 nanoseconds (ns)) provides sufficient time for the atoms to reorganize themselves back into the well-ordered crystalline phase they prefer; this is often referred to as *set* state. Alternatively, freezing the atoms into the disordered, amorphous phase requires abruptly halting the applied electrical pulse; this is often referred to as a *reset* state.

SUMMARY

[0004] The present invention, as manifested in one or more embodiments thereof, beneficially provides a phase change memory (PCM) structure, and methods for fabricating a PCM structure, which provides a gradual reset functionality. In one or more embodiments, this gradual reset functionality is achieved using a novel device geometry and applied bias signal. Specifically, aspects of the invention, as manifested in one or more embodiments, are directed to a PCM structure including phase change material sandwiched between two electrodes in a disk form factor having a gap configured to allow non-uniform heating of the phase change material. This novel PCM geometry, in conjunction with an applied bias signal having prescribed amplitude and duration characteristics, advantageously enables the PCM structure to achieve a gradual reset functionality.

[0005] In accordance with an embodiment of the invention, a PCM structure configured for performing a gradual reset operation includes first and second electrodes and a phase change material layer disposed between the first and second electrodes. The PCM structure further includes a thermal insulation layer disposed on at least sidewalls of the first and second electrodes and phase change material layer. The thermal insulation layer is

configured to provide non-uniform heating of the phase change material layer. Optionally, the thermal insulation layer may be formed as an air gap. The PCM structure may be configured having the first and second electrodes aligned in a vertical or a lateral arrangement.

[0006] In accordance with an embodiment of the invention, a method of forming a PCM structure configured for performing a gradual reset operation is provided. The method includes: forming first and second electrodes; forming a phase change material layer between the first and second electrodes; and forming a thermal insulation layer on at least sidewalls of the first and second electrodes and phase change material layer, the thermal insulation layer configured to provide non-uniform heating of the phase change material layer.

[0007] In accordance with another embodiment of the invention, a method of performing a gradual reset operation in a PCM structure is provided, the PCM structure including first and second electrodes, a phase change material layer disposed between the first and second electrodes, and a thermal insulation layer disposed on at least sidewalls of the first and second electrodes and phase change material layer. The method includes applying a first reset pulse between the first and second electrodes, the first reset pulse having an amplitude that is greater than a crystalline phase change material switching threshold voltage and less than an amorphous phase change material switching threshold voltage, for a prescribed duration to cause a temperature of the phase change material layer to rise until a temperature in a center portion of the phase change material layer exceeds a phase change material melting temperature, resulting in the center portion of the phase change material layer switching to a high-resistance amorphous state. The method further includes applying at least one subsequent reset pulse between the first and second electrodes, the subsequent reset pulse having an amplitude and duration that is the same as the first reset pulse, causing a temperature of the phase change material layer to rise until a temperature in a portion of the phase change material layer adjacent to the center portion exceeds a phase change material melting temperature, resulting in the portion of the phase change material layer adjacent to the center portion switching to a high-resistance amorphous state while the center portion of the phase change material layer remains in the high-resistance amorphous state.

[0008] As may be used herein, "facilitating" an action includes performing the action, making the action easier, helping to carry out the action, or causing the action to be performed. Thus, by way of example only and without limitation, in the context of a semiconductor fabrication methodology, steps performed by one entity might facilitate an action carried out by another entity to cause or aid the desired action(s) to be performed. For the avoidance of doubt, where an actor facilitates an action by other than performing the action, the action is nevertheless performed by some entity or combination of entities.

[0009] Techniques of the present invention can provide substantial beneficial technical effects. By way of example only and without limitation, PCM structures and/or methods of fabricating a PCM structure according to embodiments of the invention may provide one or more of the following advantages:

- gradual reset functionality;
- enables a single PCM cell to be used for both set and reset operations;
- in the context of a memory array application, achieves increased density of the overall memory array;
- increases the speed of an artificial intelligence (AI) chip in which the PCM cell is used;
- reduces power consumption of the AI chip in which the PCM cell is used.

[0010] These and other features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0011] The following drawings are presented by way of example only and without limitation, wherein like reference numerals (when used) indicate corresponding elements throughout the several views, and wherein:

[0012] FIG. 1 is a phase diagram of a germanium-antimony-tellurium (Ge-Sb-Te) ternary alloy system, with some known phase change alloys indicated;

[0013] FIG. 2 is a graph depicting exemplary temperature profiles that can be used to switch the state of the phase change material in a standard PCM cell;

[0014] FIGS. 3A and 3B are cross-sectional and top views, respectively, depicting an exemplary vertical PCM cell, according to an embodiment of the present invention;

[0015] FIG. 3C is a cross-sectional view depicting at least a portion of an exemplary vertical PCM cell having an air gap as a thermal insulation layer, according to another embodiment of the present invention;

[0016] FIGS. 4A and 4B are cross-sectional and top views, respectively, depicting an exemplary lateral PCM cell, according to an embodiment of the present invention;

[0017] FIG. 4C is a cross-sectional view depicting at least a portion of an exemplary lateral PCM cell having an air gap as a thermal insulation layer, according to another embodiment of the present invention;

[0018] FIG. 5 graphically depicts an exemplary reset signal that can be applied to the PCM cells shown in FIGS. 3A-3C and 4A-4C for performing a gradual reset operation, according to an embodiment of the present invention;

[0019] FIGS. 6A - 6C conceptually depict an exemplary amorphizing of phase change material in the exemplary vertical PCM cell of FIG. 3A resulting from an applied first reset pulse during a gradual reset operation, according to an embodiment of the present invention;

[0020] FIGS. 7A - 7C conceptually depict an exemplary amorphizing of phase change material in the exemplary vertical PCM cell of FIG. 6C resulting from an applied second reset pulse during a gradual reset operation, according to an embodiment of the present invention; and

[0021] FIG. 8 graphically depicts a plot of PCM cell conductance as a function of the number of applied reset pulses, according to an embodiment of the present invention.

[0022] It is to be appreciated that elements in the figures are illustrated for simplicity and clarity. Common but well-understood elements that may be useful or necessary in a commercially feasible embodiment may not be shown in order to facilitate a less hindered view of the illustrated embodiments.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0023] Principles of the present invention, as manifested in one or more embodiments thereof, will be described herein in the context of an illustrative phase change memory (PCM) structure, and methods for fabricating such PCM structures, having a gradual reset functionality. This gradual reset functionality, in one or more embodiments, is achieved using a novel device geometry and applied bias signal profile. It is to be appreciated, however, that the invention is not limited to the specific structures and/or methods illustratively shown and described herein. Rather, it will become apparent to those skilled in the art given the teachings herein that numerous modifications can be made to the embodiments shown that are within the scope of the claimed invention. That is, no limitations with respect to the embodiments shown and described herein are intended or should be inferred.

[0024] As previously stated, phase change materials exist in an ordered, crystalline phase (or multiple crystalline phases) having lower electrical resistance and a disordered, amorphous phase having higher electrical resistance. These phase change materials can be rapidly and repeatedly switched between their crystalline and amorphous phases, typically induced by heating through applied electrical and/or optical pulses.

[0025] Many suitable phase change materials comprise a class of compounds called chalcogenides. Chalcogenides generally exhibit strong optical and electrical contrast, fast crystallization and high crystallization temperatures (e.g., several hundred degrees Celsius). One such chalcogenide commonly used as a phase change material is the compound germanium-antimony-tellurium ($\text{Ge}_x\text{Sb}_y\text{Te}_z$ or GST). FIG. 1 is a phase diagram 100 of a Ge-Sb-Te ternary alloy system, with some known phase change alloys indicated. With reference to FIG. 1, alloys along a pseudo-binary line 102 between Sb_2Te_3 and GeTe with compositions $(\text{GeTe})_m(\text{Sb}_2\text{Te}_3)_n$, including the alloy $\text{Ge}_2\text{Sb}_2\text{Te}_5$, are used in modern PCM devices. For faster switching applications, PCM devices using undoped and slightly Ge-doped Sb phase change materials with a composition of $\text{Ge}_{15}\text{Sb}_{85}$ have also been fabricated. Another set of phase change materials along a pseudo-binary line 104 between GeTe and Sb has also been studied for use in PCM devices. Starting with the alloy $\text{Ge}_2\text{Sb}_1\text{Te}_2$ on line 104, increasing the percentage of Ge in the alloy (as represented by the arrow along line 106) leads to phase change materials having higher thermal stability of the amorphous phase, which are well-suited for high-temperature PCM applications.

[0026] As previously explained, the state of the phase change material forming the PCM cell is traditionally set (i.e., written) as a function of the amplitude and duration of an applied electrical pulse that heats the material. With

reference to FIG. 2, a graph is shown depicting exemplary temperature profiles used to switch the state of the phase change material in a standard PCM cell. Specifically, at a certain threshold voltage of the PCM cell, a resistance of the cell drops suddenly and a large current flow through the cell which heats the phase change material above its crystallization temperature, T_C , for a sufficiently long time to crystallize. Gradually turning off the applied current pulse provides sufficient time for the atoms in the phase change material to reorganize themselves back into their well-ordered crystalline phase. This *set* operation is represented by temperature profile 202. In the crystalline state, the resistance of the PCM cell is low. A larger amplitude, shorter duration current pulse applied to the PCM cell heats the phase change material above its melting temperature, T_M . By abruptly removing the current pulse, the phase change material is melt-quenched and returns to its amorphous, high resistance state. This *reset* operation is represented by temperature profile 204. Thus, traditional PCM cells can have a gradual set but an abrupt reset.

[0027] Aspects of the present invention, as manifested in one or more embodiments thereof, advantageously provide a PCM structure that, in addition to having a gradual set characteristic, provides a gradual reset functionality. This gradual reset functionality is achieved, in one or more embodiments, using a novel device geometry and applied bias signal profile.

[0028] Although the overall fabrication method and the structures formed thereby as described herein are entirely novel, certain individual processing steps required to implement the method may incorporate conventional semiconductor fabrication techniques and conventional semiconductor fabrication tooling. These techniques and tooling will already be familiar to one having ordinary skill in the relevant arts given the teachings herein. Moreover, many of the processing steps and tooling used to fabricate semiconductor devices are also described in a number of readily available publications, including, for example: P.H. Holloway et al., *Handbook of Compound Semiconductors: Growth, Processing, Characterization, and Devices*, Cambridge University Press, 2008; and R.K. Willardson et al., *Processing and Properties of Compound Semiconductors*, Academic Press, 2001, which are both hereby incorporated herein by reference in their entireties for all purposes. It is emphasized that while some individual processing steps are set forth herein, those steps are merely illustrative, and one skilled in the art may be familiar with several equally suitable alternatives that would also fall within the scope of the invention.

[0029] It is to be appreciated that the various layers and/or regions shown in the accompanying figures may not be drawn to scale. Furthermore, one or more semiconductor layers of a type commonly used in such integrated circuit devices may not be explicitly shown in a given figure to facilitate a clearer description. This does not imply that the semiconductor layer(s) not explicitly shown are omitted in the actual integrated circuit device.

[0030] By way of example only and without limitation, FIGS. 3A and 3B are cross-sectional and top views, respectively, depicting an exemplary vertical PCM cell 300, according to an embodiment of the invention. In this illustrative embodiment, the PCM cell 300 is configured having a flat, circular (i.e., discoid or disk-shaped) form

factor. More particularly, the PCM cell 300 includes a first electrode 302, which may be a bottom electrode, and a second electrode 304, which may be a top electrode. The PCM cell 300 further includes a phase change (PC) material layer 306 sandwiched between the top and bottom electrodes. That is, the PC material layer 306 is disposed on an upper surface of the bottom electrode 302, which essentially serves as a substrate to the PC material layer, and the top electrode 304 is disposed on an upper surface of the PC material layer 306. The first and second electrodes 302, 304 and PC material layer 306 can be formed, in one or more embodiments, using a standard deposition process, as will be known by those skilled in the art.

[0031] In one or more embodiments, when a bias signal (e.g., bias voltage) is applied between the top and bottom electrodes 304, 302, a current will flow through the PC material layer 306, from the electrode having a higher voltage potential to the electrode having a lower voltage potential, relative to one another. This current flowing through the PC material layer 306 will cause local heating to occur in a portion of the PC material layer. When the temperature of the phase change material reaches a prescribed threshold level, a change of state of the phase change material will, as previously explained. Since the electrodes 302, 304 are arranged in a vertical relationship relative to one another, the induced current will flow vertically through the PC material layer. Thus, the PCM cell 300 may be referred to herein as a vertical PCM device.

[0032] Beneficially, the bottom and top electrodes 302, 304 and the PC material layer 306, in this illustrative embodiment, are concentrically surrounded by a thermal insulation layer 308. The thermal insulation layer 308 functions to thermally isolate the PCM cell 300 from adjacent structures, for example, other PCM cells in a memory device. By preventing heat from escaping to surrounding structures, the thermal insulation layer 308 advantageously allows non-uniform heating of the phase change material. The thermal insulation layer 308 can also help reduce the amount of heat, and therefore applied bias signal, required to switch the crystalline state of the PCM cell 300.

[0033] As shown in FIG. 3A, a width, W , of the exemplary PCM cell 300 is preferably much greater than a height, H , of the PCM cell. In one or more embodiments, the PCM cell 300 is configured having a height in a range from about 5 nanometers (nm) to about 50 nm, and having a width in a range from about 100 nm to about 1 micron (μm), so that a ratio of width-to-height of the PCM cell 300 is about 20:1. With reference to FIG. 3B, a thickness, D , of the thermal insulation layer 308, in one or more embodiments, is in a range from about 10 nm to about 300 nm. Although it is generally desirable to minimize the thickness of the thermal insulation layer 308 to increase integration density, it is to be appreciated that embodiments of the invention are not limited to any specific dimensions of the PCM cell 300.

[0034] The material used to form the bottom and top electrodes 302, 304, in one or more embodiments, comprises a material having increased thermal resistance, such as, but not limited to, silicon, germanium, carbon, tungsten, Manganin (an alloy containing copper, manganese and nickel), etc., although embodiments of the invention are not limited to any specific material(s) for forming the bottom and top electrodes. Moreover, the bottom

and top electrodes 302, 304 need not be formed of the same material. In one or more embodiments, a thermal conductance of the first and second electrodes 302, 304 is preferably less than about 100 watts per meter-kelvin (W/m·K). The thermal insulation layer 308 preferably comprises a material having sufficient thermal insulation properties, such as materials having a thermal conductivity that is less than about 0.1 W/m·K. Suitable materials for forming the thermal insulation layer 308 include, but are not limited to, porous oxides (e.g., silicon dioxide) or air.

[0035] Alternatively, FIG. 3C is a cross-sectional view depicting at least a portion of an illustrative vertical PCM cell 350 having an air gap as a thermal insulation layer, according to another embodiment of the invention. With reference to FIG. 3C, in the illustrative PCM structure 350, the thermal insulation layer is formed as an air gap, since the properties of air are suitable for use as a thermal insulator. In one or more embodiments, when forming the thermal insulation layer as an air gap, a dielectric cap layer 352 is formed over the upper surface of the PCM cell and sidewalls of the thermal insulation layer (308 in FIG. 3A); in this embodiment, the thermal insulation layer merely serves as a dummy layer. A selective etch is then performed to remove the dummy layer, leaving an air gap 354 acting as a thermal insulation layer. The resulting PCM structure 350 is shown in FIG. 3C after removal of the dummy layer (308 in FIG. 3A).

[0036] By way of example only and without limitation, FIGS. 4A and 4B are cross-sectional and top views, respectively, depicting an exemplary lateral PCM structure or cell 400, according to another embodiment of the invention. In this illustrative embodiment, the PCM cell 400 is configured having a flat, rectangular form factor. More particularly, the PCM cell 400 includes a first electrode 402 and a second electrode 404 disposed on an upper surface of a dielectric substrate 406. Unlike the first and second electrodes 302, 304 in the illustrative PCM cell 300 shown in FIGS. 3A and 3B, the first and second electrodes 402, 404 are laterally separated and are substantially in a same plane relative to one another.

[0037] The PCM cell 400 further includes a PC material layer 408 disposed on a portion of the substrate 406 between the first and second electrodes 402, 404 and disposed on at least a portion of an upper surface of first and second electrodes. The first and second electrodes 402, 404 and PC material layer 408 can be formed, in one or more embodiments, using a standard deposition process, as will be known by those skilled in the art.

[0038] In one or more embodiments, a portion of an upper surface of the PC material layer 408 includes a trench or channel 410 formed therein, so that the upper surface of the PC material layer has a stepped, rather than a planar, profile. A thermal insulation layer 412 is then formed on the PCM cell 400, including on the upper surface of the PC material layer 408, on sidewalls of the first and second electrodes 402, 404 and PCM layer, and on a portion of the substrate 406. In this manner, the thermal insulation layer 412 essentially encapsulates the PC material layer 408, in one or more embodiments. The PCM cell 400, or at least a portion thereof, may be formed during back-end-of-line (BEOL) processing.

[0039] As shown in FIG. 4B, a width, W , of the exemplary PCM cell 400 is preferably much greater than a length, L , of the PCM cell. In one or more embodiments, the PCM cell 400 is configured having a length in a range from about 5 nm to about 50 nm, and having a width in a range from about 100 nm to about 1 μm , so that a ratio of width-to-length of the PCM cell 400 is about 20:1. With reference to FIG. 4A, a thickness, D , of the combined thermal insulation layer 412 and substrate 406, in one or more embodiments, is in a range from about 30 nm to about 300 nm and is not a critical dimension. A cross-sectional thickness of the PC material layer 408, in one or more embodiments, is in a range from about 20 nm to about 200 nm; a thickness of the PC material layer 408 may be selected based at least in part on resistance and/or power switching requirements of the PCM cell 400. It is to be appreciated, however, that embodiments of the invention are generally not limited to any specific dimensions of the PCM cell 400.

[0040] Consistent with the PCM cell 300 shown in FIGS. 3A and 3B, the material used to form the first and second electrodes 402, 404, in one or more embodiments, comprises a material having high thermal resistance, such as, but not limited to, silicon, germanium, carbon, tungsten, Manganin (an alloy containing copper, manganese and nickel), etc., although embodiments of the invention are not limited to any specific material(s) for forming the bottom and top electrodes. In one or more embodiments, a thermal conductance of the first and second electrodes 402, 404 is preferably less than about 100 W/m $\cdot$ K. Moreover, the first and second electrodes 402, 404 need not be formed of the same material. Each of the substrate 406 and thermal insulation layer 412 preferably comprises a material having sufficient thermal insulation properties. In one or more embodiments, each of the substrate 406 and thermal insulation layer 412 comprises a material having a thermal conductivity of less than about 0.1 W/m $\cdot$ K, such as, for example, porous oxides (e.g., silicon dioxide). In one or more embodiments, the substrate 406 and thermal insulation layer 412 are formed of the same material, although in other embodiments the substrate and thermal insulation layer are formed of different materials.

[0041] Alternatively, in a manner consistent with the illustrative vertical PCM cell 350 shown in FIG. 3C, the thermal insulation layer 412 may be formed as an air gap, since the properties of air are favorable for use as a thermal insulator. With reference to FIG. 4C, an illustrative lateral PCM cell 450 is depicted that utilizes an air gap for the thermal insulation layer, in accordance with another embodiment of the invention. In this embodiment, the thermal insulation layer (412 in FIG. 4A) merely serves as a dummy layer. A dielectric cap layer 452 is formed over the upper surface and sidewalls of the thermal insulation layer (412 in FIG. 4A) so as to encapsulate the thermal insulation layer. Then, a selective undercut etch is performed to remove the thermal insulation layer, leaving an air gap 454 which serves as the thermal insulation layer. The resulting PCM structure 450 is shown in FIG. 4C after removal of the dummy layer (412 in FIG. 4A).

[0042] In one or more embodiments, with reference to FIG. 4A, when a bias signal (e.g., bias voltage) is applied between the first and second electrodes 402, 404, a current will flow through the PC material layer 408, from the electrode having a higher voltage potential to the electrode having a lower voltage potential, relative to one another.

This current flowing through the PC material layer 408 will cause local heating to occur in a portion of the PC material layer. When the temperature of the phase change material reaches a prescribed threshold level (melting temperature T_M), a change of state of the phase change material will occur, as previously explained. Since the electrodes 402, 404 are arranged in the same plane (i.e., side-by-side) relative to one another, the induced current will flow laterally (i.e., horizontally) through the PC material layer 408. Thus, the PCM cell 400 may be referred to herein as a lateral PCM device.

[0043] FIG. 5 graphically depicts an exemplary reset signal 500 that can be applied to the PCM cells 300 and 400 shown in FIGS. 3A-3B and 4A-4B, respectively, for performing a gradual reset operation, according to an embodiment of the invention. As apparent from FIG. 5, the reset signal 500, in this illustration, comprises a series of pulses, with each pulse having an amplitude that is less than a threshold switching voltage of the amorphous phase change material, $V_{th(a)}$, so that no significant current passes through the phase change material that has already been amorphized. Recall that the amorphous phase of the phase change material has a much higher electrical resistance compared to the resistance of the crystalline phase of the phase change material, and thus the current will tend to favor a path of least resistance through the crystalline phase change material. Preferably, each pulse has a duration (i.e., pulse width), t_{PCM} , that is configured such that it is sufficiently long enough to raise a temperature in the crystalline phase change material to melt the material. That is, the applied reset signal 500, in one or more embodiments, is configured having a voltage amplitude that is greater than the crystalline phase change material switching threshold voltage, $V_{th(c)}$, but is less than the amorphous phase change material switching threshold voltage $V_{th(a)}$.

[0044] By way of example only, in one or more embodiments, an amplitude of each of the pulses in the reset signal 500 is about 1.5 volts (V) to about 3.5 V, and a pulse width or duration of each pulse is about 10 ns to about 50 ns. It is to be appreciated, however, that embodiments of the invention are not limited to any specific pulse amplitude or duration.

[0045] During a gradual reset operation in a PCM cell according to one or more embodiments of the invention, only a center portion of the phase change material is amorphized by a first reset pulse. A second reset pulse is configured so that a temperature of the phase change material will not exceed the amorphized region switching threshold voltage so that the current in this center amorphized region will be low. Consequently, the center region of the PC material layer will not be appreciably heated and will thus remain in its amorphous state. Instead, most of the reset current will flow around the center amorphized region and will heat up a region of the phase change material immediately adjacent to and surrounding the center amorphized region; and so on for subsequent reset pulses. In this manner, the phase change material surrounding the center region will be amorphized, layer by layer, with each successive reset pulse.

[0046] More particularly, FIGS. 6A - 6C conceptually depict an exemplary amorphizing of phase change material in a PCM cell (e.g., 300 or 400 in FIGS. 3A or 4A, respectively) resulting from an applied first reset pulse during a gradual reset operation, according to an embodiment of the invention. With reference to FIG. 6A, the exemplary vertical PCM cell 300 of FIG. 3 is shown in its crystalline phase. When a first reset pulse having an amplitude, V , that is greater than the crystalline phase change material switching threshold voltage but less than the amorphous phase change material switching threshold voltage $V_{th(a)}$ (i.e., $V_{th(c)} < V < V_{th(a)}$) is applied between the top electrode 304 and bottom electrode 302, a current (represented by the arrows in FIG. 6A) will flow throughout the PC material layer 306 in a substantially uniform manner. FIG. 6B depicts an exemplary temperature profile 620 of the phase change material as a function of distance in the PC material layer 306. As apparent from FIG. 6B, the current flowing through the PC material layer 306 will cause a temperature of the phase change material to rise until the temperature in a center portion of the phase change material exceeds a phase change material melting temperature, T_M . This results in a center portion 630 of the PC material layer 306 switching to its high-resistance amorphous state, as shown in FIG. 6C. A width of this amorphous portion of the PC material layer 306 is labelled $W1$ in FIGS. 6B and 6C.

[0047] Similarly, FIGS. 7A - 7C conceptually depict an exemplary amorphizing of phase change material in the PCM cell (e.g., 300 or 400 in FIGS. 3A or 4A, respectively) resulting from an applied second reset pulse during a gradual reset operation, according to an embodiment of the invention. With reference to FIG. 7A, the exemplary vertical PCM cell of FIG. 6C is shown with the PC material layer 306 including an amorphized center portion 630 of width $W1$ after the first reset pulse was applied. When a second reset pulse having the same characteristics as the first reset pulse, at least in terms of amplitude V ($V_{th(c)} < V < V_{th(a)}$) and duration, is applied between the top electrode 304 and bottom electrode 302, a current (represented by the arrows shown in FIG. 7A) will flow primarily through the low-resistance crystalline portion of the PC material layer 306, and substantially no current will flow through the high-resistance amorphous portion 630. FIG. 7B depicts an exemplary temperature profile 720 of the phase change material as a function of distance in the PC material layer 306. As apparent from FIG. 7B, the current flowing through the PC material layer 306 will cause a temperature of the phase change material to rise until the temperature of the phase change material (portions 722 and 724 of the temperature profile 720) adjacent to the center amorphized portion 630 exceeds the phase change material melting temperature T_M . Additionally, the temperature of the center amorphized portion 630 will remain below the critical melting temperature, and thus the center amorphized portion will not return to its crystalline state. This results in portions (722 and 724) of the phase change material adjacent to the center portion 630 becoming amorphized such that a width of the amorphized portion 630 in the PC material layer 306 will increase to $W2$ ($W2 > W1$), as shown in FIG. 7C. This process can be repeated until essentially all of the phase change material comprised in the PC material layer 306 has been amorphized.

[0048] FIG. 8 graphically depicts a plot 800 of PCM cell conductance as a function of the number of applied reset pulses, according to an embodiment of the present invention. As apparent from FIG. 8, the electrical conductance, in units of Siemens (S), of the PCM cell according to one or more embodiments of the invention decreases substantially linearly with the number of successive reset pulses, thereby providing a gradual reset operation in the PCM cell. Each successive reset pulse will have a corresponding distinguishable resistance value that can be measured (e.g., by a sense amplifier or the like). In this manner, a PCM cell according to embodiments of the invention functions as an analog memory device.

[0049] At least a portion of the structures and fabrication methods of the present invention may be implemented in an integrated circuit. In forming integrated circuits, identical die are typically fabricated in a repeated pattern on a surface of a semiconductor wafer. Each die includes a device described herein, and may include other structures and/or circuits. The individual die are cut or diced from the wafer, then packaged as an integrated circuit. One skilled in the art would know how to dice wafers and package die to produce integrated circuits. Any of the exemplary structures illustrated in the accompanying figures, or portions thereof, may be part of an integrated circuit. Integrated circuits so manufactured are considered part of this invention.

[0050] Those skilled in the art will appreciate that the exemplary structures discussed above can be distributed in raw form (i.e., a single wafer having multiple unpackaged chips), as bare dies, in packaged form, or incorporated as parts of intermediate products or end products that benefit from having PCM devices therein formed in accordance with one or more embodiments of the invention.

[0051] An integrated circuit in accordance with aspects of the present disclosure can be employed in essentially any application and/or electronic system involving PCM, such as, but not limited to, a memory array, neural network, etc. Suitable systems for implementing embodiments of the invention may include, but are not limited to, computing systems. Systems incorporating such integrated circuits are considered part of this invention. Given the teachings of the present disclosure provided herein, one of ordinary skill in the art will be able to contemplate other implementations and applications of embodiments of the invention.

[0052] The illustrations of embodiments of the invention described herein are intended to provide a general understanding of the various embodiments, and they are not intended to serve as a complete description of all the elements and features of apparatus and systems that might make use of the structures and semiconductor fabrication methodologies described herein. Many other embodiments will become apparent to those skilled in the art given the teachings herein; other embodiments are utilized and derived therefrom, such that structural and logical substitutions and changes can be made without departing from the scope of this disclosure. The drawings are also merely representational and are not drawn to scale. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

[0053] Embodiments of the invention are referred to herein, individually and/or collectively, by the term "embodiment" merely for convenience and without intending to limit the scope of this application to any single embodiment or inventive concept if more than one is, in fact, shown. Thus, although specific embodiments have been illustrated and described herein, it should be understood that an arrangement achieving the same purpose can be substituted for the specific embodiment(s) shown; that is, this disclosure is intended to cover any and all adaptations or variations of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will become apparent to those of skill in the art given the teachings herein.

[0054] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, steps, operations, elements, components, and/or groups thereof. Terms such as "above," "below," "upper," "lower," "top" and "bottom" which may be used throughout the present disclosure are intended to indicate the positioning of elements or structures relative to each other rather than absolute orientation.

[0055] The corresponding structures, materials, acts, and equivalents of all means or step-plus-function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the various embodiments has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the forms disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiments were chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the various embodiments with various modifications as are suited to the particular use contemplated.

[0056] The following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as separately claimed subject matter. Given the teachings of embodiments of the invention provided herein, one of ordinary skill in the art will be able to contemplate other implementations and applications of the techniques of embodiments of the invention. Although illustrative embodiments of the invention have been described herein with reference to the accompanying drawings, it is to be understood that embodiments of the invention are not limited to those precise embodiments, and that various other changes and modifications are made therein by one skilled in the art without departing from the scope of the appended claims.