# FULLY DEPLETED SILICON-ON-INSULATOR CMOS LOGIC

## TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to silicon-on-insulator devices and in particular the present invention relates to fully depleted silicon-on-insulator logic.

## BACKGROUND OF THE INVENTION

The increased speed and capability of computers and other electronic devices requires better performance from the integrated circuits that make up a device. One way to make the integrated circuits faster is to reduce the size of the transistors that make up the device. However, as transistors are made smaller and faster, delays through the connections between the transistors becomes greater in relation to the speed of the transistor.

An alternative technique to speed up integrated circuits is to use alternative semiconductors. For example, silicon-on-insulator (SOI) technology provides a 25 – 35% performance increase over equivalent CMOS technologies. SOI refers to placing a thin layer of silicon on top of an insulator such as silicon oxide or glass. The transistors would then be built on this thin layer of SOI. The SOI layer reduces the capacitance of the transistors so that they operate faster.

Figure 1 illustrates a typical SOI semiconductor. The transistor is formed in the silicon layer 101 that is over the insulator 102. The insulator is formed on top of the substrate 103. Within the silicon layer 101, the drain/source regions 105 and 106 are formed. The gate 107 is formed above the partially depleted channel 109. A floating body 110 is within the depleted region 112 and results from the partial depletion.

SOI technology, however, imposes significant technical challenges. The silicon film used for SOI transistors must be perfect crystalline silicon. The insulator layer, however, is not crystalline. It is very difficult to make perfect crystalline silicon-on-oxide or silicon with other insulators since the insulator layer's crystalline properties are so different from the pure silicon. If perfect crystalline silicon is not obtained, defects will find their way onto the SOI film. This degrades the transistor performance.

Additionally, if the p-type body is contacted by implanted regions there will be a very high resistance of the body region, particularly if the transistor is wide. Impact

ionization can cause a large current through this resistance and forward bias the body, thus resulting in transients.

One alternative to this floating body effect is the fully depleted silicon-on-sapphire (SOS) semiconductor. This type of semiconductor does not have a partially depleted silicon layer or floating body. However, they can still experience a problem where the drain current does not stay constant as the drain voltage increases when the transistor is in the saturation region of operation. Instead, the current "kinks" up to a higher value. Clearly, the collection of carriers either on a floating body or near the source is undesirable.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a way to control adverse floating body effects in partially depleted CMOS devices using SOI technology.

## SUMMARY

The above-mentioned problems with adverse floating body effects and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

The present invention encompasses a method for generating a fully depleted body structure in a silicon-on-insulator device. The method provides an extractor contact coupled to the body structure. An extractor voltage is provided such that the extractor contact is reverse biased and minority carriers in the body structure are removed.

Further embodiments of the invention include methods and apparatus of varying scope.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a cross sectional view of a typical silicon-on-insulator transistor.

Figure 2 shows a top view of one embodiment of a silicon-on-insulator transistor of the present invention.

Figure 3 shows a cross sectional view of a fully depleted silicon-on-insulator inverter using one embodiment of the reverse biased extractor contact method of the present invention.

Figure 4 shows a cross sectional view of an NROM flash memory cell using one embodiment of the method of the present invention to fully deplete silicon-on-insulator transistors.

Figure 5 shows a top view of the NROM flash memory cell of Figure 4.

Figure 6 shows a cross sectional view of a typical prior art partially depleted NROM flash memory cell.

Figure 7 shows a cross sectional view of a fully depleted NROM flash memory cell using one embodiment of the extractor contact reverse bias method of the present invention.

Figure 8 shows a cross sectional view of a fully depleted vertical NROM flash memory cell using one embodiment of the extractor contact reverse bias method of the present invention.

Figure 9 shows an electronic system in accordance with a fully depleted silicon-on-insulator transistor of the present invention.

## DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

Figure 2 illustrates a top view of one embodiment of a silicon-on-insulator (SOI) NMOS transistor of the present invention. The present invention uses reverse biasing of the body contacts, also known as extractors, to provide a fully depleted transistor. The extractors

remove minority carriers from the body region of a partially depleted MOS device. This eliminates the effect where the drain current does not stay constant as the drain voltage increases when a device is operating in the saturation mode.

The SOI transistor illustrated in Figure 2 is comprised of two drain/source regions 201 and 202. In one embodiment, these regions are n+ wells formed in the silicon layer. The width of these regions 201 and 202 is indicated as W. In one embodiment, the width is one micron or less. Alternate embodiments use other widths. In another embodiment, transistors wider than one micron can be realized through parallel transistors.

A p+ region extractor contact 205 is formed in the silicon layer substantially adjacent the two drain/source regions 201 and 202. In an alternate embodiment, such as a PMOS device, the extractor contact 205 would be implemented on an n+ silicon region. A gate 207 is formed above and between the drain/source regions 201 and 202.

Figure 3 illustrates a cross sectional view of one embodiment of an SOI inverter using the reverse biased extractors of the present invention. The inverter is comprised of two transistors, an NMOS device 320 and a PMOS device 321. Each transistor 320 and 321 has an associated extractor contact 310 and 311. Each extractor 310 and 311 is coupled to the body structure 301 and 302 of each transistor. The NMOS body structure 301 is comprised of a p-type silicon while the PMOS body structure 302 is comprised of an n-type silicon.

Each transistor 320 and 321 has an associated control gate 307 and 308 respectively. The control gate 307 is located above the drain/source regions (not shown). The insulator 305 and substrate 306 are also illustrated.

The extractors 310 and 311 are reverse biased with respect to the substrate potential. To reverse bias the extractor 302 of the PMOS transistor 321, a voltage that is greater than the drain voltage, $V_{DD}$, is applied. The NMOS transistor's extractor 301 is reverse biased by applying a voltage that is less than ground potential.

In one embodiment, the additional voltages needed to bias the extractor nodes above $V_{DD}$ and below ground can be generated by charge pump circuits that are well known in the art. These pumps are not illustrated.

The extractor reverse biasing of the present invention changes the partially depleted SOI structure to fully depleted without a floating body region. Charge that is generated by

floating body or near the source. Removal of any excess charge generated by leakage currents or impact ionization will be by diffusion current and not be drift along a highly resistive p-type body region.

Flash memories based on electron trapping are well known and commonly used electronic components. Smaller cell sizes have always been one of the more important issues for low bit cost and high density flash memory. Conventional planar NOR flash memory cells require a large number of contacts. NAND flash memories are a series of devices with contacts at the end of a long series of bits. This results in a very high bit density.

Nitride read only memory (NROM) flash memory devices employ charge trapping in a silicon nitride layer. NROM devices can be implemented with the CMOS process.

SOI has recently been employed for NROM flash cells. Figure 4 illustrates a cross sectional view of an NROM flash memory cell using one embodiment of the method of the present invention to fully deplete silicon-on-insulator transistors. The NROM flash memory cell of Figure 4 is a NOR array cell with virtual ground bit lines.

The NROM flash memory cell is comprised of the SOI layer 410 on the insulator 411. The bit lines 401 and 402 are n-type regions in this embodiment. When the extractor contacts (shown in Figure 5) are reverse biased, the body region 403 between the bit lines is fully depleted. The oxide-nitride-oxide (ONO) region 405 is between the control gate 406 and the silicon layer 410.

Figure 5 illustrates a top view of the NROM flash memory cell of Figure 4. This view shows the bit lines 401 and 402 and the control gate 406. The extractor contacts 501 and 502 are p-type regions over the depleted body 403.

One problem with typical partially depleted NROM flash memory cells is that the floating body causes a problem during an erase operation. When a negative erase potential is applied to the control gate in an NROM device, the partially depleted body terminates many of the electric field lines as illustrated in the cross sectional view of Figure 6. In this case, the body potential floats negative causing the electric field 601 that is attempting to erase the charge 603, stored in the ONO composite gate insulator 605, to become smaller and the erase speed slower.

The extractor reverse biasing method of the present invention can be applied to an NROM flash memory cell to increase erase speed. Additionally, the erase speed will not drift and change with time due to floating body effects as occurs in partially depleted devices.

Figure 7 illustrates a cross sectional view of an NROM flash memory cell that uses one embodiment of the method of the present invention for fully depleting silicon-on-insulator transistors. The charge 703 stored in the ONO layer 705 is erased by the electric field 701 without a drift in the erase speed. The fully depleted body 710 does not have a negative effect on the electric field 701 as in a partially depleted device.

While the embodiments of Figures 4 – 7 illustrate NROM flash memory cells, alternate embodiments may use conventional flash memory cells on SOI. If there is a floating body, the negative control gate potential couples through the floating gate to the floating body. The floating body then changes to a negative potential. This decreases the electric field used for negative control gate to source erase, thus slowing the erase operation. The fully depleted SOI transistor bodies of the present invention eliminate this effect.

Figure 8 illustrates a vertical NROM 301 that can use the reverse biased extractors of the present invention to produce a fully depleted body structure. As shown in Figure 8, the vertical NROM 801 includes a vertical metal oxide semiconductor field effect transistor (MOSFET) 801 extending outwardly from a substrate 800. The MOSFET 801 has a first source/drain region 802 that, in this n-channel embodiment, includes a heavily doped (n+) n-type region layered with an n-type doped region. The MOSFET 801 includes a similarly structured second source/drain region 806.

A channel region 805 is located in the vertical pillar between the first and the second source/drain regions, 802 and 806 respectively. As shown in the embodiment of Figure 8, a gate 809 is separated from the channel region 805 by a gate insulator 807 as is located alongside of the vertical pillar opposing the channel region 805.

In the embodiment shown in Figure 8, the gate insulator 807 includes a gate insulator formed of an oxide-nitride-oxide (ONO) composition 807. In alternative embodiments, discussed below, the gate insulator 807 includes a gate insulator selected from the group of silicon dioxide ($SiO_2$) formed by wet oxidation, silicon oxynitride (SON), silicon rich oxide (SRO), and silicon rich aluminum oxide ($Al_2O_3$). In one embodiment, the gate insulator 807 has a thickness of approximately 10 nanometers (nm).

In other embodiments, the gate insulator 807 includes a gate insulator 807 selected from the group of silicon rich aluminum oxide insulators, silicon rich oxides with inclusions of nanoparticles of silicon, silicon oxide insulators with inclusions of nanoparticles of silicon carbide, and silicon oxycarbide insulators. In still other embodiments, the gate insulator 807 includes a composite layer selected from the group of an oxide-aluminum oxide ($Al_2O_3$)-oxide composite layer, an oxide-silicon oxycarbide-oxide composite layer, and an oxide-nitride-aluminum oxide composite layer.

The aluminum oxide top layer has a higher dielectric constant so that this layer can be thicker in order to preclude tunneling to and from the control gate to the nitride storage layer. Alternate embodiments use other high dielectric constant insulators as the top layer.

In still other embodiments, the gate insulator 807 includes a gate insulator 807 that includes a composite layer, or a non-stoichiometric single layer of two or more materials selected from the group of silicon (Si), titanium (Ti), and tantalum (Ta).

Figure 9 illustrates a functional block diagram of a memory device 900 coupled to a processor 910 and incorporating one embodiment of an SOI memory cell of the present invention. The processor 910 may be a microprocessor, a processor, or some other type of controlling circuitry. The memory device 900 and the processor 910 form part of an electronic system 920.

The memory device includes an array of SOI-structured memory cells 930 as described in the various embodiments above. In one embodiment, the memory cells are non-volatile floating-gate memory cells and the memory array 930 is arranged in banks of rows and columns.

An address buffer circuit 940 is provided to latch address signals provided on address input connections A0-Ax 942. Address signals are received and decoded by a row decoder 944 and a column decoder 946 to access the memory array 930. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 930. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

The memory device 900 reads data in the memory array 930 by sensing voltage or current changes in the memory array columns using sense/latch circuitry 950. The sense/latch

circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 930. Data input and output buffer circuitry 960 is included for bi-directional data communication over a plurality of data connections 962 with the controller 910. Write circuitry 955 is provided to write data to the memory array.

Control circuitry 970 decodes signals provided on control connections 972 from the processor 910. These signals are used to control the operations on the memory array 930, including data read, data write, and erase operations. The control circuitry 970 may be a state machine, a sequencer, or some other type of controller.

The flash memory device illustrated in Figure 9 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art.

## CONCLUSION

In summary, floating body effects in partially depleted CMOS devices using SOI technology are undesirable in many logic and memory applications. In static CMOS logic and SRAM memories, the floating bodies cause threshold voltages and switching speeds to be variable and complex functions of the switching history of a particular logic gate. In dynamic logic DRAM memories, the floating bodies cause excess charge leakage and short retention times that can result in data loss. Conventional flash memories and NROM memories experience reduced erase fields and slower erase times due to floating bodies. The use of reverse biased extractors of the present invention, resulting in fully depleted body structures, substantially reduces or eliminates these undesirable effects.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention.

## CLAIMS

1. A transistor having a silicon-on-insulator structure on a substrate, the transistor comprising:

a drain region comprising a first doped material and formed in the silicon-on-insulator;

a source region comprising the first doped material and formed in the silicon-on-insulator;

a control gate formed above and substantially between the drain and source regions; and

an extractor contact, in the silicon-on-insulator, comprising a second doped material and coupled to a depletion region substantially between the drain and source regions, the depletion region being fully depleted in response to a reverse bias of the extractor contact.

2. The transistor of claim 1 wherein the first doped material is comprised of n-type silicon and the second doped material is comprised of p-type silicon.

3. The transistor of claim 1 wherein the first doped material is comprised of p-type silicon and the second doped material is comprised of n-type silicon.

4. The transistor of claim 1 wherein the extractor contact is coupled to a p-type silicon on the insulator or an n-type silicon on the insulator.

5. A vertical multiple bit memory cell having a silicon-on-insulator structure on a substrate, the memory cell comprising:

a vertical metal oxide semiconductor field effect transistor (MOSFET) extending horizontally outward from a substrate, the MOSFET having a drain region, a source region, a channel region between the source and drain regions, and a gate separated from the channel region by a high dielectric constant gate insulator that can store a first charge in a first storage region and a second charge in a second storage region;

a first transmission line coupled to the drain region;

a second transmission line coupled to the source region; and

an extractor contact coupled to the channel region in the silicon-on-insulator such that a reverse bias voltage on the extractor contact fully depletes the channel region.

6. The cell of claim 5 wherein the reverse bias voltage is greater than a drain voltage applied to the drain region for cell operation.

7. The cell of claim 5 wherein the reverse bias voltage is less than a voltage applied to substrate for cell operation.

8. The cell of claim 7 wherein the substrate voltage is ground potential.

9. The cell of claim 5 wherein a positive voltage is applied to the gate in order to erase a charge stored in the cell.

10. The cell of claim 5 wherein the extractor contact is comprised of p-type silicon.

11. The cell of claim 5 wherein the high dielectric constant gate insulator comprises an oxide-nitride-oxide layer.

12. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes a memory array having a plurality of memory cells with a silicon-on-insulator structure, each memory cell comprising:

a drain region comprising a first doped material and formed in the silicon-on-insulator;

a source region comprising the first doped material and formed in the silicon-on-insulator;

a control gate formed above and substantially between the drain and source regions; and

an extractor contact comprising a second doped material and coupled to a depletion region in the silicon-on-insulator substantially between the drain and source regions, the depletion region being fully depleted in response to a reverse bias of the extractor contact.

13. The electronic system of claim 12 wherein the memory cell is a vertical memory cell.

14. The electronic system of claim 12 and further including an oxide-nitride-oxide layer between the control gate and the silicon-on-insulator.

15. The electronic system of claim 12 wherein the memory device is a flash memory device.

16. The electronic system of claim 15 wherein the flash memory device is a NAND flash memory device.

17. A silicon-on-insulator inverter comprising:

a PMOS transistor formed in an n+ well in an insulator structure on a substrate, the transistor comprising:

a drain region comprising a first p+ doped region in the n+ well;

a source region comprising a second p+ doped region in the n+ well;

an control gate formed above and substantially between the drain and source regions; and

an extractor contact coupled to a depletion region in the n+ well substantially between the drain and source regions, the depletion region being fully depleted in response to a reverse bias of the extractor contact; and

an NMOS transistor coupled to the PMOS transistor and formed in a p+ well in the insulator structure on the substrate, the transistor comprising:

a drain region comprising a first n+ doped region in the p+ well, the drain region coupled to the NMOS source region;

a source region comprising a second n+ doped region in the p+ well;

a control gate formed above and substantially between the drain and source regions, the PMOS control gate coupled to the NMOS control gate; and

an extractor contact coupled to a depletion region in the p+ well substantially between the drain and source regions, the depletion region being fully depleted in response to a reverse bias of the extractor contact.

18. The inverter of claim 17 wherein a bias voltage of $V_{DD}$ is coupled to the PMOS drain region and the PMOS extractor contact is biased at a voltage greater than $V_{DD}$ and the NMOS extractor contact is biased at a voltage less than ground potential.

19. The inverter of claim 17 wherein the NMOS source region is coupled to ground potential.

20. The inverter of claim 17 wherein the reverse bias on the PMOS extractor contact is a voltage greater than $V_{DD}$ and the reverse bias on the NMOS extractor contact is a voltage less than ground potential.