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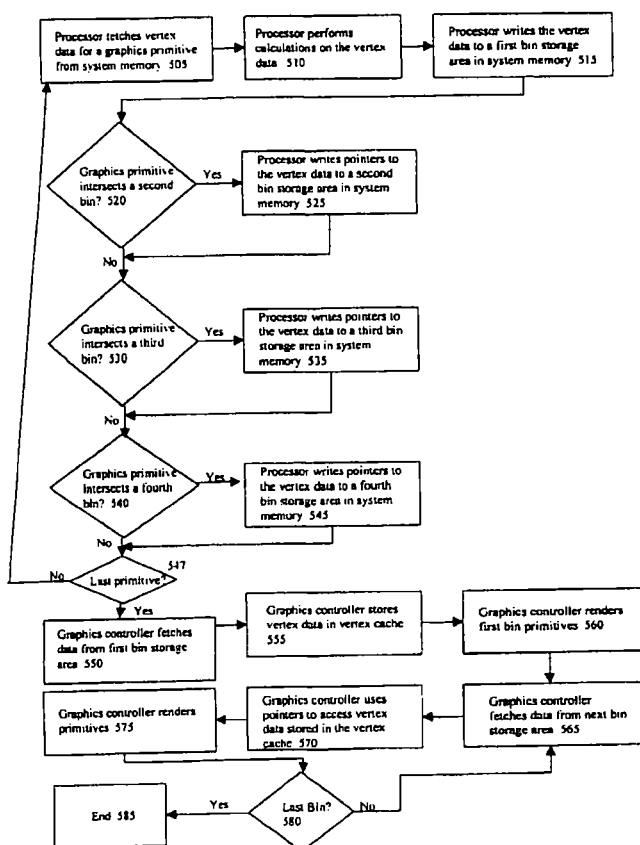
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(54) Title: TILED GRAPHICS ARCHITECTURE



(57) Abstract: A method and apparatus for reducing memory bandwidth utilization in a tiled graphics architecture is disclosed. In one embodiment, a microprocessor reads vertex data for a graphics primitive from graphics memory. The processor determines with which bins the graphics primitive intersects. Assuming that the processor determines that the graphics primitive intersects a first and a second bin, the processor writes the vertex data for the graphics primitive to a first bin storage area in graphics memory. The processor then writes a pointer to a second bin storage area. The pointer indicates the location in memory of the actual vertex data.



WO 01/75804 A1

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