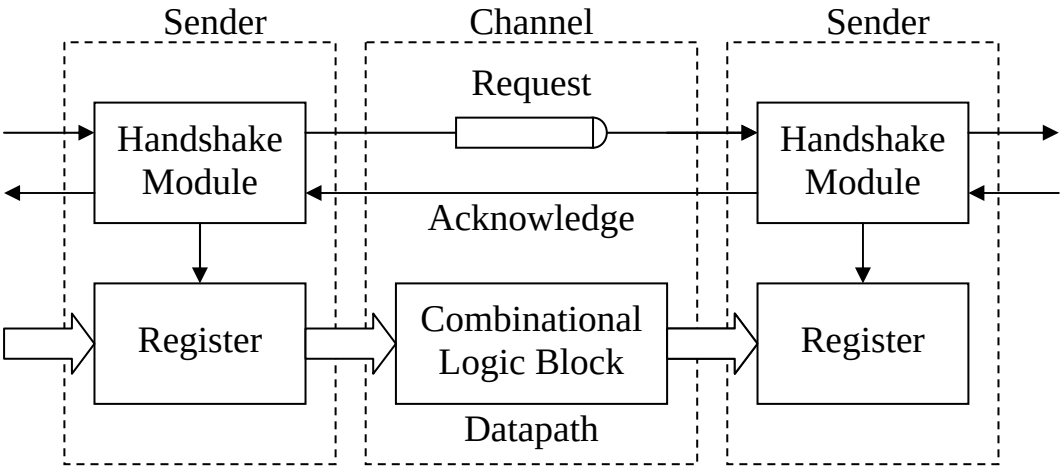

FIG. 1 (Prior-art)

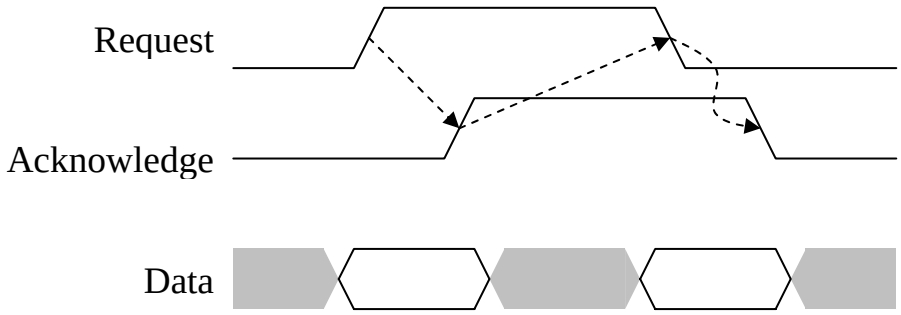

FIG. 2 (Prior-art)

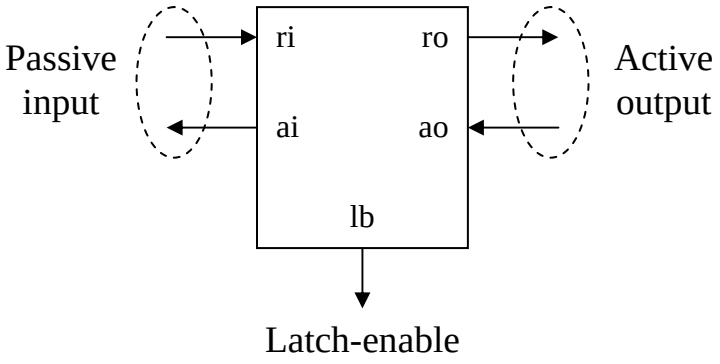
Passive
input
ri
ro
Active
output
ai
ao
lb
Latch-enable

FIG. 3

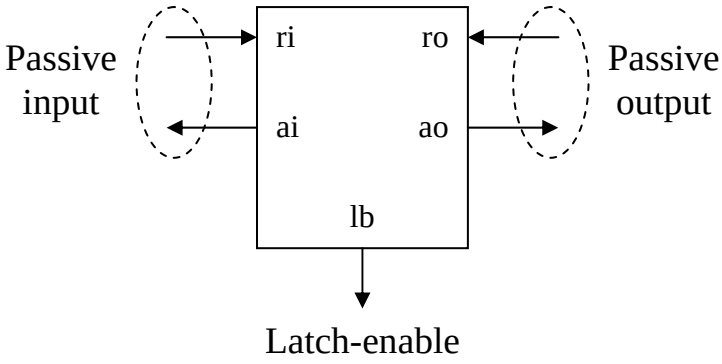
Passive
input
ri
ro
Passive
output
ai
ao
lb
Latch-enable

FIG. 4

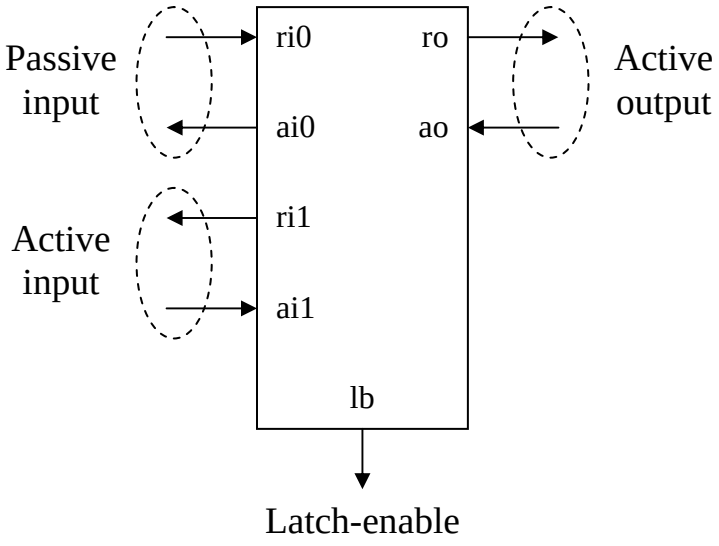
Passive
input
ri0
ro
Active
output
ai0
ao
Active
input
ri1
ai1
lb
Latch-enable

FIG. 5

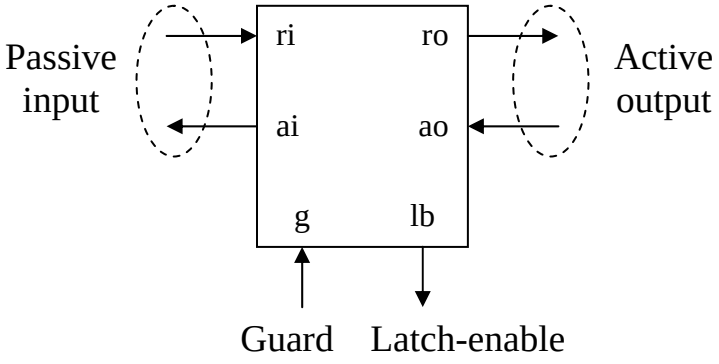
Passive
input
ri
ro
Active
output
ai
ao
g
lb
Guard
Latch-enable

FIG. 6

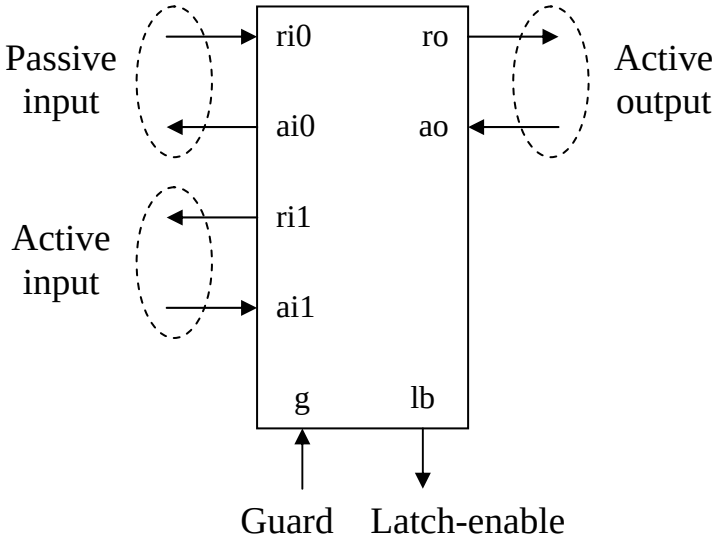
Passive input
Active input
ri0
ro
ai0
ao
ri1
ai1
g
lb
Active output
Guard
Latch-enable

FIG. 7

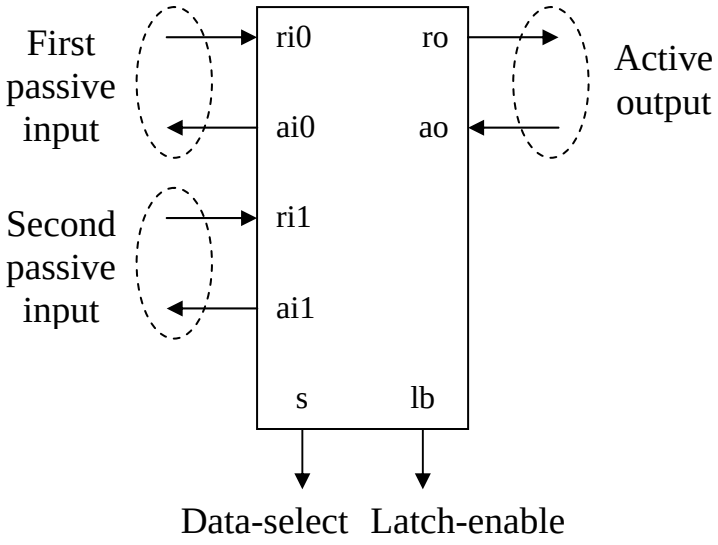
First passive input
Second passive input
ri0
ro
ai0
ao
ri1
ai1
s
lb
Active output
Data-select
Latch-enable

FIG. 8

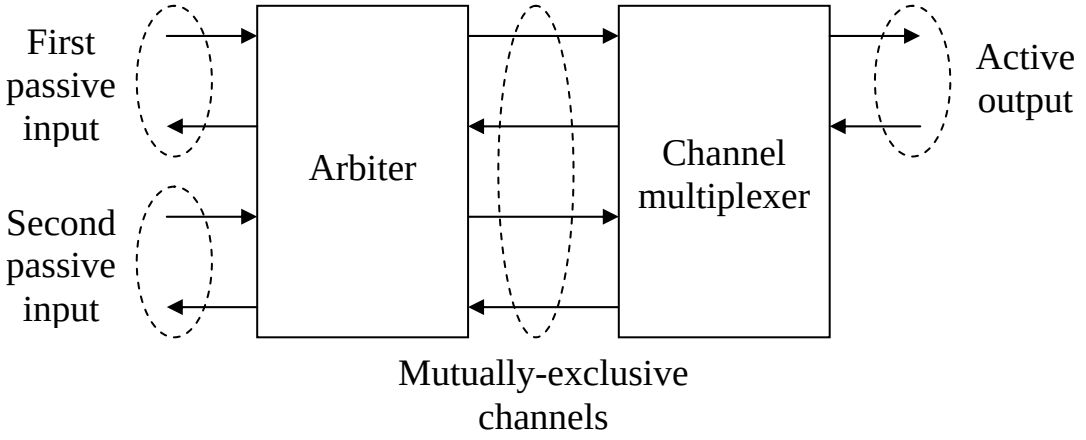
First
passive
input
Second
passive
input
Arbiter
Channel
multiplexer
Active
output
Mutually-exclusive
channels

FIG. 9

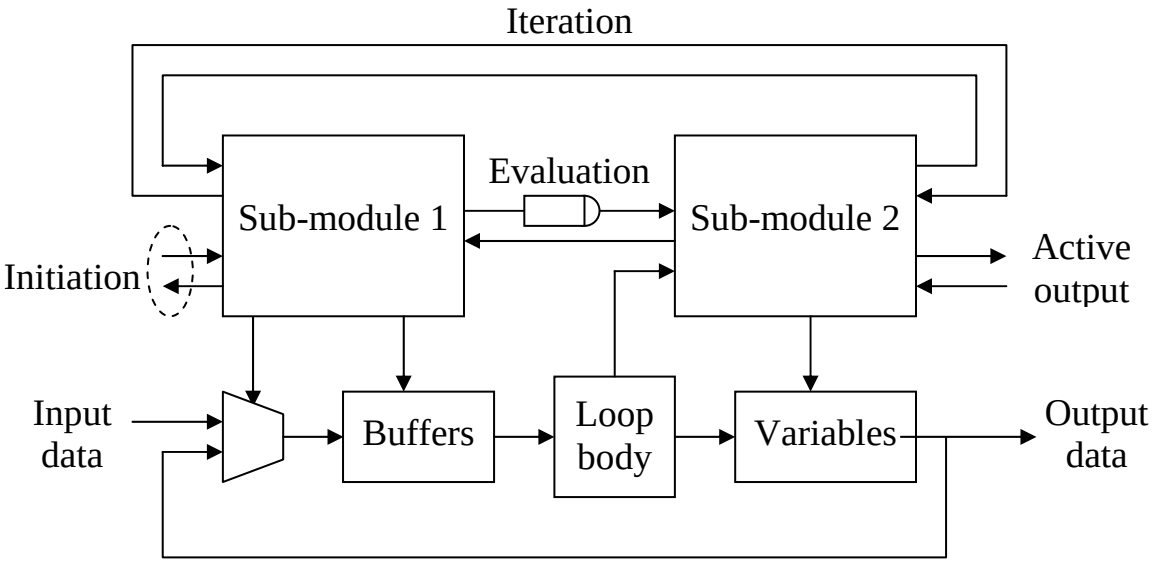
Iteration
Sub-module 1
Evaluation
Sub-module 2
Initiation
Active
output
Input
data
Buffers
Loop
body
Variables
Output
data

FIG. 10

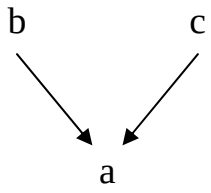

FIG. 11

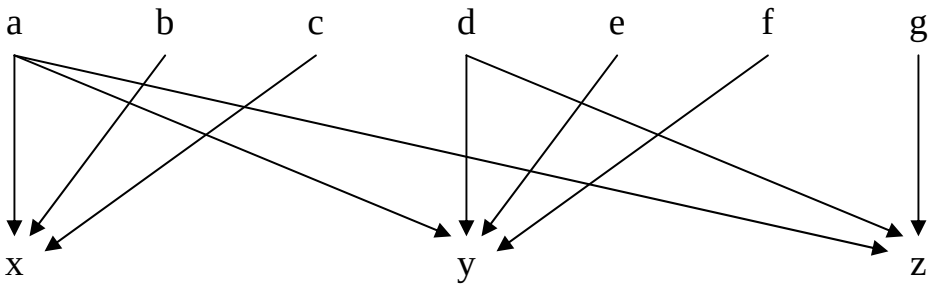

FIG. 12

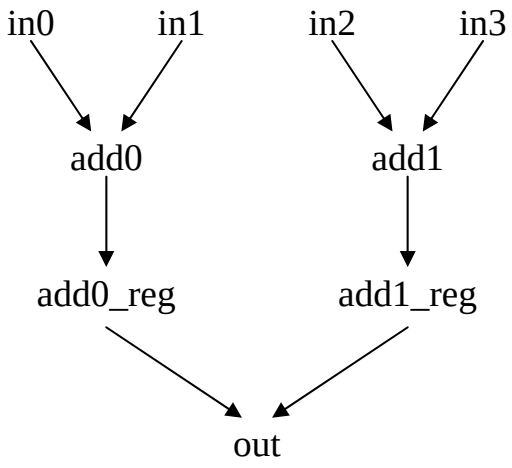
in0
in1
in2
in3
add0
add1
add0_reg
add1_reg
out

FIG. 13

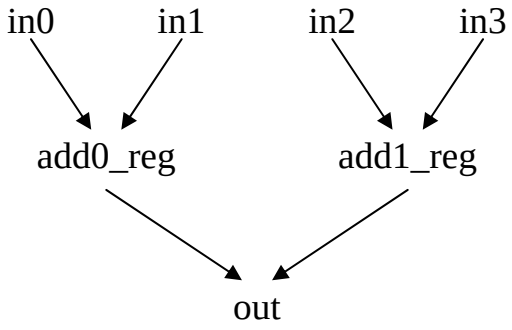
in0
in1
in2
in3
add0_reg
add1_reg
out

FIG. 14