predetermined sequence. The limitation of this method is linked to the difficulty of stopping the process at the right moment, i.e. to completely remove the required material without damaging the metal pad and to avoid the resputtering of its conductive material (usually, copper), *i.e.* ejection of conductive material towards the walls of the via, which can later induce short-circuits at the active device's junctions due to the diffusion of unwanted copper ions into the silicon bulk.

As a consequence, in spite of the aforementioned drawbacks, dry etching is still privileged over other known techniques since it is a simple and common way to rapidly obtain a straight via in an integrated circuit.

An insulating film is then coated on the via walls by conventional techniques such as deposition. These methods however also coat the conductive pad and the existing insulating layer(s), so that an additional step to remove the insulating film at least from the conductive pad becomes necessary, in order to enable connection with the components.

There is therefore a need for a method that overcomes the aforementioned drawbacks.

SUMMARY OF THE INVENTION

Embodiments~~An objective~~ of the invention ~~is to~~ provide a method for precisely forming a good through electrical connection in a layered semiconductor structure that avoids resputtering and guarantees the exposition of the device structure in a few steps.

~~To this end, the invention proposes a method for forming a vertical electrical connection in a layered semiconductor structure, comprising the following steps:~~

~~providing a layered semiconductor structure, said layered semiconductor structure comprising:~~

~~a support substrate including a first surface and a second surface (24);~~

~~- an insulating layer overlying the first surface of the support substrate, and~~

~~- at least one device structure formed in the insulating layer; and~~

~~- drilling a via from the second surface of the support substrate (20) up to the device structure, in order to expose the device structure;~~

~~characterized in that drilling of the insulating layer is at least partially performed by wet etching.~~

According to a first aspect, there is provided a method for forming a vertical electrical connection in a layered semiconductor structure, comprising the following steps:

- providing a layered semiconductor structure, said layered semiconductor structure comprising:
  - a support substrate including a first surface and a second surface,
  - an insulating layer overlying the first surface of the support substrate, and
  - at least one device structure formed in the insulating layer; and
- drilling a via from the second surface of the support substrate up to the device structure, in order to expose the device structure, drilling of the insulating layer being at least partially performed by wet etching;

the method being characterized in that it further comprises a step of wet coating of the via with an insulating film by bringing a surface of said via into contact with a liquid solution, in order to obtain a uniform insulating film, wherein the wet coating of the via is selective and only coats the via in the vicinity of the support substrate.

Some preferred but non limiting ~~aspects~~embodiments of the invention are the following:

* wet etching is performed during a predetermined time, said predetermined time depending on the material of the insulating layer, the etchant and the thickness of the insulating layer to be drilled;

* wet etching is performed with a solution containing fluorhydric acid, and optionally glycerol;

* the etchant comprises between 0.5% and 50% in volume of fluorhydric acid, preferably 1.35%;

* the etchant further comprises between 0.5 and 50% in volume of glycerol, preferably 1.35%;

* the method further comprises a pre-wetting step prior to the wet etching step (320), wherein the layered semiconductor structure is plunged in water;

* a rinsing step following the wet etching step, wherein the layered semiconductor structure is rinsed with water;

* the method further comprises a vacuum step following the wet etching step, wherein the layered semiconductor structure is submitted to a controlled vacuum;

* the layered semiconductor structure is plunged in water during the vacuum step;

* the method further comprises a removal step before the wet etching step, wherein the support substrate is thinned;

* the method further comprises a pre-drilling step before the wet etching step, wherein a pre-via is formed from the second surface up to at least the insulating layer; and

* the pre-via is formed by dry etching, wet etching or reactive ion etching.

Disclosed herein is~~In accordance with a second aspect, the invention proposes~~ a method for fabricating a vertical connection in a layered semiconductor structure, comprising the following steps:

- forming the vertical connection in the layered semiconductor structure in accordance with the above-mentioned method, and
- wet coating the vertical connection with an insulating film by bringing a surface of said vertical connection into contact with a liquid solution.

Preferred but non limiting ~~aspects~~embodiments of the method of the invention are the following:

* the wet coating solution comprises:
- a protic solvent;
- at least one diazonium salt;
- at least one monomer that is chain-polymerizable and soluble in said protic solvent;
- at least one acid in a sufficient quantity to stabilize said diazonium salt by adjusting the pH of said solution to a value less than 7, preferably less than 2.5; and

the surface of said vertical connection is polarizes according to a potentio- or galvano-pulsed mode for a duration sufficient to form a film having a thickness of at least 60 nanometres, and preferably between 80 and 500 nanometers;

* the method further comprises the preparation of a copper diffusion barrier by:

- at least one solvent;

- copper ions in a concentration of between approximately 14 and 120mM;

- ethylenediamine;

- the molar ratio of ethylenediamine to copper being between 1.80 and 2.03;

- the pH of said composition being between 6.6 and 7.5;

b) polarizing said free surface of the second layer for a sufficient duration to form said copper seed layer;

* the method further comprises a step of metallization of the vertical electrical connection by electrodepositing copper with a composition comprising:

- copper ions, said copper ions having a concentration of 45 to 1500 mM, preferably 45 to 500 mM, and more preferably 100 to 300 mM;

- a complexing agent for copper, comprising at least one component of the group comprising the aliphatic polyamines having 2 to 4 amino groups, said complexing agent for copper having a concentration of 45 to 3000 mM, preferably 45 to 1500 mM, and more preferably 300 to 900 mM;

The complexing agent for copper can be, for example, ethylenediamine, diethylenediamine, triethylenediamine or dipropylenetriamine, preferably ethylenediamine.

- the molar ratio between copper and said complexing agent for copper being of 0.1 to 5, preferably 0.1 to 1, and more preferably 0.2 to 0.4;

- thiodiglycolic acid, said thiodiglycolic acid having a concentration of 1 to 500 mg/L; and

- optionnaly, a buffering system, in particular ammonium sulphate, in a concentration of 0.1 to 3 M.

~~In accordance with a third aspect, the invention proposes a layered semiconductor structure comprising:~~

~~—a support substrate including an first surface and a second surface,~~

~~- an insulating layer overlying the first surface of the support substrate,~~

~~- at least one device structure formed in the insulating layer; and~~

~~- at least one vertical connection, extending from the second surface of the support substrate up to the device structure,~~

~~characterized in that the vertical connection comprises an undercut in the vicinity of the first surface of the support substrate obtainable in accordance with the aforementioned method.~~

According to a second aspect, there is provided a layered semiconductor structure comprising:

- a support substrate including an first surface and a second surface,
- an insulating layer overlying the first surface of the support substrate,
- at least one device structure formed in the insulating layer ;
- at least one vertical connection, extending from the second surface of the support substrate up to the device structure,

wherein the vertical connection comprises an undercut (U) in the insulating layer in the vicinity of the first surface of the support substrate, and

- at least an insulating film applied on the walls of the vertical connection only in the vicinity of the support substrate, wherein said insulating layer has a uniform thickness.

Preferred but non-limiting ~~aspects~~embodiments of the invention are the following:

* the method further comprises at least an insulating film applied on the walls of the vertical connection in the vicinity of the support substrate (30), wherein said insulating layer has a uniform thickness and is obtained in particular by the aforementioned method;

* the method further comprises a copper diffusion barrier over the insulating layer and the walls of the vertical connection, wherein said copper diffusion barrier has a uniform thickness and is obtained in particular by the aforementioned method;

* the method further comprises a copper seed layer (80) over the copper diffusion barrier (70), wherein said copper seed layer (80) has a uniform thickness and is obtained in particular by the aforementioned method;

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figures 1 to 6 represent a sectional view of an example of semiconductor structure during the different steps of a method in accordance with the invention;

Figure 3A is a close-up of one of the undercuts of Figure 3; and

CLAIMS

1. A method for forming a vertical electrical connection (50) in a layered semiconductor structure (1), comprising the following steps:

- providing (100) a layered semiconductor structure (1), said layered semiconductor structure (1) comprising:
- a support substrate (20) including a first surface (22) and a second surface (24),
- an insulating layer (30) overlying the first surface (22) of the support substrate (20), and
- at least one device structure (40) formed in the insulating layer (30); and
- drilling (300) a via (50) from the second surface of the support substrate (20) up to the device structure (40), in order to expose the device structure (40);

characterized in that drilling (300) of the insulating layer is at least partially performed by wet etching (320).

2. The method of claim 1, wherein wet etching (320) is performed during a predetermined time, said predetermined time depending on the material of the insulating layer (30), the etchant and the thickness of the insulating layer (30) to be drilled.

3. The method of claim 1 or 2, wherein wet etching (320) is performed with a solution containing fluorhydric acid, and optionally glycerol.

4. The method of claim 3, wherein the etchant comprises between 0.5% and 50% in volume of Fluorhydric acid, preferably 1.35%.

5. The method of claim 3 or 4, wherein the etchant further comprises between 0.5 and 50% in volume of glycerol, preferably 1.35%.

6. The method of anyone of claims 1 to 5 further comprising a pre-wetting step (322) prior to the wet etching step (320), wherein the layered semiconductor structure (1) is plunged in water.

7. The method of anyone of claims 1 to 6 further comprising a rinsing step (324) following the wet etching step (320), wherein the layered semiconductor structure (1) is rinsed with water.

8. The method of anyone of claims 1 to 7 further comprising a vacuum step (326, 328) following the wet etching step (320), wherein the layered semiconductor structure (1) is submitted (328) to a controlled vacuum.

9. The method of claim 8, wherein the layered semiconductor structure (1) is plunged (326) in water during the vacuum step (326, 328).

10. The method of anyone of claims 1 to 9 further comprising a removal step (310) before the wet etching step (320), wherein the support substrate (20) is thinned.

11. The method of anyone of claims 1 to 10 further comprising a pre-drilling step (310) before the wet etching step (320), wherein a pre-via (52) is formed from the second surface (24) up to at least the insulating layer (30).

12. The method of claim 11, wherein the pre-via (52) is formed by dry etching, wet etching or reactive ion etching.

13. A method for fabricating a vertical connection (50) in a layered semiconductor structure (1), comprising the following steps:

- forming the vertical connection (50) in the layered semiconductor structure in accordance with anyone of claims 1 to 12, and
- wet coating (400) the vertical connection (50) with an insulating film (60) by bringing a surface of said vertical connection (50) into contact with a liquid solution.

14. The method of claim 13, wherein the solution comprises:
- a protic solvent;
- at least one diazonium salt;
- at least one monomer that is chain-polymerizable and soluble in said protic solvent;
- at least one acid in a sufficient quantity to stabilize said diazonium salt by adjusting the pH of said solution to a value less than 7, preferably less than 2.5; and

wherein the surface of said vertical connection (50) is polarizes according to a potentio- or galvano-pulsed mode for a duration sufficient to form a film having a thickness of at least 60 nanometres, and preferably between 80 and 500 nanometers.

15. The method of claims 13 or 14, further comprising the preparation (500) of a copper diffusion barrier (70) by:

a) forming by a wet process, at the surface of the insulating film (60), an organic film containing particles, especially nanoparticles, of metals or metal alloys, in particular of nickel or cobalt;

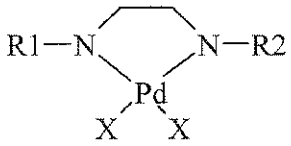
b) bringing the film thus formed into contact with a liquid solution containing at least one metal salt, preferably of the same nature as the metal incorporated into the organic film, a stabilizing agent, and at least one reducing agent under conditions enabling the formation of a metal film having a thickness of at least 100 nm.

16. The method of claims 13 or 14, further comprising the preparation (500) of a copper diffusion barrier (70) by:

1) activating the surface of the insulating layer with a solution comprising:

i) an activator constituted of one or several palladium complexes chosen in the group consisting of:

- palladium complexes having the formula (I):

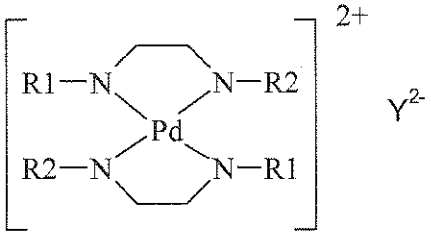


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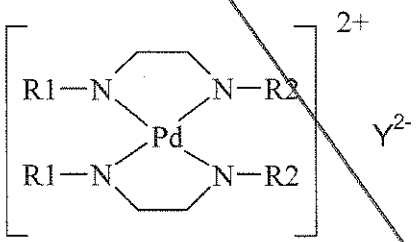
wherein :

- R1 and R2 are identical and represent H ; $CH_2CH_2NH_2$; CH_2CH_2OH ; or
- R1 represents H and R2 represents $CH_2CH_2NH_2$; or
- R2 represents CH2CH2NHCH2CH2NH2 and R1 represents $CH_2CH_2NH_2$; or
- R2 represents $CH_2CH_2NHCH_2CH_2NHCH_2CH_2NH_2$ and R1 represents H;
- X represents a ligand chosen in the group consisting of Cl^- ; Br^- ; I^- ; H_2O, NO_3^- ; $CH_3SO_3^-$; $CF_3SO_3^-$; CH_3-Ph-SO_3^- ; CH_3COO^-;

- palladium complexes having the formula (IIa) or (IIb):



(IIa)



(IIb)

wherein :

- R1 and R2 are defined as above-mentioned, and
- Y represents a counter-ion comprising two negative charges constituted:

▪ either of two mono-anions preferably chosen in the group consisting of Cl^- ; PF_6^- ; BF_4^- ; NO_3^- ; $CH_3SO_3^-$; $CF_3SO_3^-$; $CH_3C_6H_4SO_3^-$; CH_3COO^- ; or

▪ of a di-anion, preferably SO_4^{2-} ;

ii) an bi-functional organic binder constituted of one or several organosilanes having the general formula:

$$\{NH_2\text{-}(L)\}_{3-n}\text{-}Si(OR)_n \qquad (V)$$

wherein:

- L is a spacer selected from the group consisting of CH_2; CH_2CH_2; $CH_2CH_2CH_2$- and $CH_2CH_2NHCH_2CH_2$;
- R is a group selected from the group consisting of CH_3, CH_3CH_2, $CH_3CH_2CH_2$, $(CH_3)_2CH$; and
- n is an integer equal to 1, 2 or 3.

iii) a solvent system constituted of one or several solvents suitable for solubilising said activator and said binder;

2. electrolessly depositing a metallic layer on the activated surface.

17. The method of claim 15 or 16, further comprising the preparation (600) of a copper seed layer (70) by:

a) bringing the free surface of the copper diffusion barrier layer into contact with a liquid solution comprising:

- at least one solvent;
- copper ions in a concentration of between approximately 14 and 120mM;
- ethylenediamine;
- the molar ratio of ethylenediamine to copper being between 1.80 and 2.03;

- the pH of said composition being between 6.6 and 7.5;

b) polarizing said free surface of the second layer for a sufficient duration to form said copper seed layer.

18. The method of claim 16 or 17, further comprising a step of metallization of the vertical electrical connection by electrodepositing copper with a composition comprising:

- copper ions, said copper ions having a concentration of 45 to 1500 mM, preferably 45 to 500 mM, and more preferably 100 to 300 mM;
- a complexing agent for copper, comprising at least one component of the group comprising the aliphatic polyamines having 2 to 4 amino groups, said complexing agent for copper having a concentration of 45 to 3000 mM, preferably 45 to 1500 mM, and more preferably 300 to 900 mM;
- the molar ratio between copper and said complexing agent for copper being of 0.1 to 5, preferably 0.1 to 1, and more preferably 0.2 to 0.4;
- thiodiglycolic acid, said thiodiglycolic acid having a concentration of 1 to 500 mg/L; and
- optionally, a buffering system, in particular ammonium sulphate, in a concentration of 0.1 to 3 M.

19. A layered semiconductor structure (1) comprising:

- a support substrate (20) including an first surface (22) and a second surface (24),
- an insulating layer (30) overlying the first surface (22) of the support substrate (20),
- at least one device structure (40) formed in the insulating layer (30); and
- at least one vertical connection (50), extending from the second surface (24) of the support substrate (30) up to the device structure (40),

characterized in that the vertical connection (50) comprises an undercut (U) in the vicinity of the first surface (22) of the support substrate (30) obtainable in accordance with anyone of claims 1 to 12.

20. The layered semiconductor structure (1) of claim 19, further comprising at least an insulating film (60) applied on the walls of the vertical connection in the vicinity of the support substrate (30), wherein said insulating layer (60) has a uniform thickness and is obtained in particular by the method of claim 13 or 14.

21. The layered semiconductor structure (1) of claim 20, further comprising a copper diffusion barrier (70) over the insulating layer (60) and the walls of the vertical connection (50), wherein said copper diffusion barrier (70) has a uniform thickness and is obtained in particular by the method of claim 15 or 16.

22. The layered semiconductor structure (1) of claim 20, further comprising a copper seed layer (80) over the copper diffusion barrier (70), wherein said copper seed layer (80) has a uniform thickness and is obtained in particular by the method of claim 17.

CLAIMS

1. A method for forming a vertical electrical connection in a layered semiconductor structure, comprising the following steps:

- providing a layered semiconductor structure, said layered semiconductor structure comprising:
  - a support substrate including a first surface and a second surface,
  - an insulating layer overlying the first surface of the support substrate, and
  - at least one device structure formed in the insulating layer; and
- drilling a via from the second surface of the support substrate up to the device structure, in order to expose the device structure, drilling of the insulating layer being at least partially performed by wet etching;

the method being characterized in that it further comprises a step of wet coating of the via with an insulating film by bringing a surface of said via into contact with a liquid solution, in order to obtain a uniform insulating film, wherein the wet coating of the via is selective and only coats the via in the vicinity of the support substrate.

2. The method of claim 1, wherein wet etching is performed during a predetermined time, said predetermined time depending on the material of the insulating layer, the etchant and the thickness of the insulating layer to be drilled.

3. The method of claim 1 or 2, wherein wet etching is performed with a solution containing fluorhydric acid, and optionally glycerol.

4. The method of claim 3, wherein the etchant comprises between 0.5% and 50% in volume of Fluorhydric acid, preferably 1.35%.

5. The method of claim 3 or 4, wherein the etchant further comprises between 0.5 and 50% in volume of glycerol, preferably 1.35%.

6. The method of anyone of claims 1 to 5 further comprising a pre-wetting step prior to the wet etching step, wherein the layered semiconductor structure is plunged in water.

7. The method of anyone of claims 1 to 6 further comprising a rinsing step following the wet etching step, wherein the layered semiconductor structure is rinsed with water.

8. The method of anyone of claims 1 to 7 further comprising a vacuum step following the wet etching step, wherein the layered semiconductor structure is submitted to a controlled vacuum.

9. The method of claim 8, wherein the layered semiconductor structure is plunged in water during the vacuum step.

10. The method of anyone of claims 1 to 9 further comprising a removal step before the wet etching step, wherein the support substrate is thinned.

11. The method of anyone of claims 1 to 10 further comprising a pre-drilling step before the wet etching step, wherein a pre-via is formed from the second surface up to at least the insulating layer.

12. The method of claim 11, wherein the pre-via is formed by dry etching, wet etching or reactive ion etching.

13. The method of claim 1, wherein the solution comprises:

a protic solvent;

at least one diazonium salt;

at least one monomer that is chain-polymerizable and soluble in said protic solvent;

at least one acid in a sufficient quantity to stabilize said diazonium salt by adjusting the pH of said solution to a value less than 7, preferably less than 2.5; and

wherein the surface of said vertical connection is polarizes according to a potentio- or galvano-pulsed mode for a duration sufficient to form a film having a thickness of at least 60 nanometres, and preferably between 80 and 500 nanometers.

14. The method of claims 1 or 13, further comprising the preparation of a copper diffusion barrier by:

a) forming by a wet process, at the surface of the insulating film, an organic film containing particles, especially nanoparticles, of metals or metal alloys, in particular of nickel or cobalt;

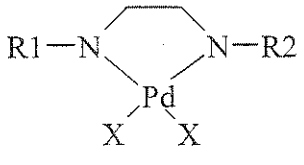
b) bringing the film thus formed into contact with a liquid solution containing at least one metal salt, preferably of the same nature as the metal incorporated into the organic film, a stabilizing agent, and at least one reducing agent under conditions enabling the formation of a metal film having a thickness of at least 100 nm.

15. The method of claims 1 or 13, further comprising the preparation (500) of a copper diffusion barrier by:

1. activating the surface of the insulating layer with a solution comprising:

i) an activator constituted of one or several palladium complexes chosen in the group consisting of:

- palladium complexes having the formula (I):

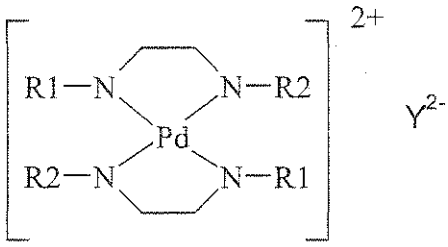


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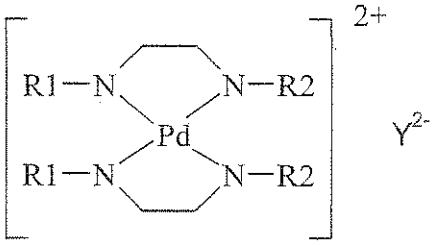
wherein :

- R1 and R2 are identical and represent H ; $CH_2CH_2NH_2$; CH_2CH_2OH ; or
- R1 represents H and R2 represents $CH_2CH_2NH_2$; or
- R2 represents CH2CH2NHCH2CH2NH2 and R1 represents $CH_2CH_2NH_2$; or
- R2 represents $CH_2CH_2NHCH_2CH_2NHCH_2CH_2NH_2$ and R1 represents H;
- X represents a ligand chosen in the group consisting of Cl^- ; Br^- ; I^- ; H_2O, NO_3^- ; $CH_3SO_3^-$; $CF_3SO_3^-$; CH_3-Ph-SO_3^- ; CH_3COO^-;

▪ palladium complexes having the formula (IIa) or (IIb):



(IIa)



(IIb)

wherein :

- R1 and R2 are defined as above-mentioned, and
- Y represents a counter-ion comprising two negative charges constituted:

▪ either of two mono-anions preferably chosen in the group consisting of Cl^- ; PF_6^- ; BF_4^- ; NO_3^- ; $CH_3SO_3^-$; $CF_3SO_3^-$; $CH_3C_6H_4SO_3^-$; CH_3COO^- ; or

▪ of a di-anion, preferably SO_4^{2-} ;

ii) an bi-functional organic binder constituted of one or several organosilanes having the general formula:

$$\{NH_2\text{-}(L)\}_{3-n}\text{-}Si(OR)_n \qquad (V)$$

wherein:

- L is a spacer selected from the group consisting of CH_2; CH_2CH_2; $CH_2CH_2CH_2$- and $CH_2CH_2NHCH_2CH_2$;
- R is a group selected from the group consisting of CH_3, CH_3CH_2, $CH_3CH_2CH_2$, $(CH_3)_2CH$; and

- n is an integer equal to 1, 2 or 3.

iii) a solvent system constituted of one or several solvents suitable for solubilising said activator and said binder;

2. electrolessly depositing a metallic layer on the activated surface.

16. The method of claim 14 or 15, further comprising the preparation of a copper seed layer by:

a) bringing the free surface of the copper diffusion barrier layer into contact with a liquid solution comprising:

- at least one solvent;

- copper ions in a concentration of between approximately 14 and 120mM;

- ethylenediamine;

- the molar ratio of ethylenediamine to copper being between 1.80 and 2.03;

- the pH of said composition being between 6.6 and 7.5;

b) polarizing said free surface of the second layer for a sufficient duration to form said copper seed layer.

17. The method of claim 15 or 16, further comprising a step of metallization of the vertical electrical connection by electrodepositing copper with a composition comprising:

- copper ions, said copper ions having a concentration of 45 to 1500 mM, preferably 45 to 500 mM, and more preferably 100 to 300 mM;

- a complexing agent for copper, comprising at least one component of the group comprising the aliphatic polyamines having 2 to 4 amino groups, said complexing agent for copper having a concentration of 45 to 3000 mM, preferably 45 to 1500 mM, and more preferably 300 to 900 mM;

- the molar ratio between copper and said complexing agent for copper being of 0.1 to 5, preferably 0.1 to 1, and more preferably 0.2 to 0.4;

- thiodiglycolic acid, said thiodiglycolic acid having a concentration of 1 to 500 mg/L; and

- optionally, a buffering system, in particular ammonium sulphate, in a concentration of 0.1 to 3 M.

18. A layered semiconductor structure comprising:

- a support substrate including an first surface and a second surface,
- an insulating layer overlying the first surface of the support substrate,
- at least one device structure formed in the insulating layer ;
- at least one vertical connection, extending from the second surface of the support substrate up to the device structure,

wherein the vertical connection comprises an undercut (U) in the insulating layer in the vicinity of the first surface of the support substrate, and

- at least an insulating film applied on the walls of the vertical connection only in the vicinity of the support substrate, wherein said insulating layer has a uniform thickness.

19. The layered semiconductor structure of claim 18, further comprising a copper diffusion barrier over the insulating layer and the walls of the vertical connection, wherein said copper diffusion barrier has a uniform thickness.

20. The layered semiconductor structure of claim 19, further comprising a copper seed layer over the copper diffusion barrier, wherein said copper seed layer has a uniform thickness.