

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor device, comprising:
 - a horizontal semiconductor layer including a plurality of well regions having a first conductivity and a separation impurity region having a second conductivity, the separation impurity region being between and in contact with the plurality of well regions; and
 - a plurality of cell array structures provided on the plurality of well regions of the horizontal semiconductor layer, respectively,
 - wherein the plurality of well regions are arranged along first and second directions that are perpendicular to each other and parallel to a top surface of the horizontal semiconductor layer,
 - wherein the separation impurity region surrounds each of the plurality of well regions, and
 - wherein each of the cell array structures comprises:
 - a stack structure including a plurality of stacked electrodes stacked in a vertical direction on the top surface of the horizontal semiconductor layer; and
 - a plurality of vertical structures penetrating the stack structure and connected to a corresponding one of the well regions.
2. The three-dimensional semiconductor device of claim 1, wherein the horizontal semiconductor layer includes at least two PN junctions formed by the separation impurity region and two well regions that are adjacent to each other and have the separation impurity region therebetween.

3. The three-dimensional semiconductor device of claim 1, wherein the horizontal semiconductor layer includes at least two PN junctions formed by the separation impurity region and portions of the well regions in contact with the separation impurity region.

4. The three-dimensional semiconductor device of claim 1, wherein the separation impurity region comprises a pair of impurity regions having the second conductivity, and

wherein the pair of impurity regions are spaced apart from each other and disposed between well regions adjacent to each other.

5. The three-dimensional semiconductor device of claim 4, further comprising:

a dummy impurity region between the pair of impurity regions and having the first conductivity,

wherein the horizontal semiconductor layer includes a plurality of PN junctions formed by the dummy impurity region and the pair of impurity regions.

6. The three-dimensional semiconductor device of claim 5, wherein an impurity concentration of the first conductivity is less in the dummy impurity region than an impurity concentration of the first conductivity in the well regions.

7. The three-dimensional semiconductor device of claim 1, wherein the separation impurity region is disposed between cell array structures adjacent to each other.

8. The three-dimensional semiconductor device of claim 1, wherein each of the cell array structures comprises a plurality of NAND cell strings that extend in the vertical direction to the top surface of the horizontal semiconductor layer.

9. The three-dimensional semiconductor device of claim 1, wherein the horizontal semiconductor layer is a single layer extending in the first and second directions.

10. The three-dimensional semiconductor device of claim 1,
wherein the plurality of well regions are arranged along first and second directions that are perpendicular to each other and parallel to the top surface of the horizontal semiconductor layer, and

wherein the separation impurity region extends in the second direction between well regions adjacent to each other in the first direction, and extends in the first direction between well regions adjacent to each other in the second direction.

11. The three-dimensional semiconductor device of claim 1,
wherein the plurality of well regions are arranged along first and second directions that are perpendicular to each other and parallel to the top surface of the horizontal semiconductor layer, and

wherein the separation impurity region has a width in the first direction less than that of one of the plurality of well regions.

12. The three-dimensional semiconductor device of claim 1,

wherein the separation impurity region comprises first and second separation impurity regions that are provided between well regions adjacent to each other in a first direction and are spaced apart from each other in a second direction perpendicular to the first direction, and

wherein the horizontal semiconductor layer comprises an opening between the first and second separation impurity regions.

13. The three-dimensional semiconductor device of claim 1, further comprising:

a peripheral logic structure including a semiconductor substrate, peripheral logic circuits on the semiconductor substrate, and a lower buried insulation layer covering the peripheral logic circuits,

wherein the horizontal semiconductor layer is disposed on a top surface of the lower buried insulation layer.

14. The three-dimensional semiconductor device of claim 13, further comprising:

an upper buried insulation layer on the horizontal semiconductor layer and covering the stack structure,

wherein the horizontal semiconductor layer comprises an opening between well regions adjacent to each other in one direction and exposing the lower buried insulation layer, the opening of the horizontal semiconductor layer being filled with the upper buried insulation layer.

15. A three-dimensional semiconductor device, comprising:

a peripheral logic structure including a peripheral logic circuit integrated on a semiconductor substrate;

a horizontal semiconductor layer on the peripheral logic structure and including a plurality of well regions and a separation impurity region between adjacent well regions, the plurality of well regions being doped with first conductivity impurities and the separation impurity region being doped with second conductivity impurities; and

a plurality of cell array structures on corresponding well regions of the horizontal semiconductor layer, each of the cell array structures including a plurality of three-dimensionally arranged memory cells;

wherein the plurality of well regions are arranged along first and second directions that are perpendicular to each other and parallel to a top surface of the horizontal semiconductor layer,

wherein the separation impurity region surrounds each of the plurality of well regions.

16. The three-dimensional semiconductor device of claim 15, wherein the plurality of well regions and the separation impurity region overlap the peripheral logic circuit, when viewed in a plan view.

17. The three-dimensional semiconductor device of claim 15, wherein the horizontal semiconductor layer is a single layer extending in the first and second directions.

18. The three-dimensional semiconductor device of claim 15,

wherein the well regions are arranged along the first and second directions,
and

wherein the separation impurity region is provided between well regions adjacent to each other in the first direction and between well regions adjacent to each other in the second direction.

19. The three-dimensional semiconductor device of claim 15,
wherein the well regions are arranged along the first and second directions,
and

wherein the separation impurity region has a width in the first direction less than a width of each of the well regions.

20. The three-dimensional semiconductor device of claim 15,
wherein the well regions are spaced apart from each other in the first direction,

wherein the separation impurity region comprises first and second impurity regions spaced apart from each other in the first direction, and

wherein the three-dimensional semiconductor device further comprises a dummy impurity region between the first and second impurity regions and doped with the first conductivity impurities.