CLAIMS

What is claimed is:

1. A method of operating a memory array, comprising:

writing a first logic state to a ferroelectric memory cell;

determining that the ferroelectric memory cell has stored the first logic state for a first time period;

writing a second logic state to the ferroelectric memory cell based at least in part on the determining that the ferroelectric memory cell has stored the first logic state for the first time period, wherein the second logic state is different from the first logic state; and

storing an indicator in a latch, wherein a value of the indicator indicates whether an intended logic state of the ferroelectric memory cell is the first logic state or the second logic state.

2. The method of claim 1, further comprising:

sensing the second logic state of the ferroelectric memory cell with a sense component that is in electronic communication with the ferroelectric memory cell; and

determining that the freintended logic state of the ferroelectric memory cell is the first logic state based at least in part on sensing the second logic state and the value of the indicator.

3. The method of claim 1, further comprising:

identifying a codeword from a read operation of the memory array, wherein [[a]] the value of the codeword is based at least in part on the value of the indicator; and

determining that the intended logic state of the ferroelectric memory cell is the first logic state based at least in part on the codeword.

4. The method of claim 1, further comprising:

receiving the first logic state for storage in the ferroelectric memory cell; and

writing the second logic state to the ferroelectric memory cell based at least in part on the value of the indicator.

5. The method of claim 1, further comprising:

updating the value of the indicator based at least in part on writing the second logic state to the ferroelectric memory cell, wherein the updated value of the indicator indicates that the intended logic state of the ferroelectric memory cell is the first logic state.

6. The method of claim 5, further comprising:

determining that the ferroelectric memory cell has stored the second logic state for a second time period; and

writing back the first logic state to the ferroelectric memory cell based at least in part on determining that the ferroelectric memory cell has stored the second logic state for the second time period.

7. The method of claim 6, further comprising:

updating the value of the indicator based at least in part on writing the first logic state to the ferroelectric memory cell, wherein the updated value of the indicator indicates that the intended logic state of the ferroelectric memory cell is the first logic state.

8. The method of claim 6, wherein the first time period comprises a first interval of a cycle and the second time period comprises a second interval of the cycle, wherein a period of the cycle includes a time between writing the first logic state and writing back the first logic state.

9. The method of claim 1, wherein the latch comprises one latch of a plurality of latches, and wherein the intended logic state of the ferroelectric memory cell is based at least in part on the value being stored by a majority of the plurality of latches.

10. The method of claim 1, further comprising:

identifying that the ferroelectric memory cell has stored the first logic state for the first time period without being accessed, wherein writing the second logic state is based at least in part on the identifying.

11. The method of claim 1, further comprising:

identifying a subsection of the memory array that includes the ferroelectric memory cell; and

writing different logic states to each ferroelectric memory cell of the subsection based at least in part on determining that one or more ferroelectric memory cells of the subsection has stored the first logic state for the first time period.

12. The method of claim 1, wherein determining the first time period has elapsed comprises at least one of:

determining that a number of errors has exceeded a threshold number;

determining that the memory array has operated in a low power mode;

determining that the memory array has operated in a powered down mode; or

determining that a command from a user has been received.

13. The method of claim 1, further comprising:

activating a subsection of the memory array that includes the ferroelectric memory cell, wherein writing the ferroelectric memory cell comprises writing different logic states to each ferroelectric memory cell of the subsection based at least in part on activating the subsection.

14. The method of claim 1, wherein the second logic state is opposite the first logic state.

15. The method of claim 1, wherein the first time period is based at least in part on at least one of a temperature of the ferroelectric memory cell, an age of the ferroelectric memory

cell, an average delay between access operations of the ferroelectric memory cell, or a sensing window resulting from reading the ferroelectric memory cell, or any combination thereof.

16. An electronic memory apparatus, comprising:

a ferroelectric memory cell writable with a first logic state and writable with a second logic state based at least in part on the first logic state being written for a first time period; and

a latch coupled to the ferroelectric memory cell, wherein the latch comprises a non-volatile memory cell to store an indication of whether the first logic state or the second logic state represents an intended logic state of the ferroelectric memory cell.

17. The electronic memory apparatus of claim 16, further comprising:

a sense amplifier in electronic communication with the latch and the ferroelectric memory cell.

18. The electronic memory apparatus of claim 16, further comprising:

an error correction code (ECC) component in electronic communication with the latch and an output of a sense amplifier.

19. The electronic memory apparatus of claim 16, wherein the latch comprises a second ferroelectric memory cell.

20. An electronic memory apparatus, comprising:

a ferroelectric memory cell; and

a controller in electronic communication with the ferroelectric memory cell, wherein the controller is operable to:

determine that the ferroelectric memory cell has stored a first logic state for a first time period;

write a second logic state to the ferroelectric memory cell based at least in part on the determining that the ferroelectric memory cell has stored the first logic state for the first time period, wherein the second logic state is different from the first logic state; and

update a value of an indicator based at least in part on writing the second logic state to the ferroelectric memory cell, wherein the updated value of the indicator indicates that an intended logic state of the ferroelectric memory cell is the first logic state.

21. An electronic memory apparatus, comprising:

a latch that comprises a non-volatile memory cell;

a ferroelectric memory cell; and

a controller in electronic communication with the ferroelectric memory cell, wherein the controller is operable to:

determine that the ferroelectric memory cell has stored a first logic state for a first time period;

write a second logic state to the ferroelectric memory cell based at least in part on the determining that the ferroelectric memory cell has stored the first logic state for the first time period, wherein the second logic state is different from the first logic state; and

store an indicator in the latch, wherein a value of the indicator indicates whether an intended logic state of the ferroelectric memory cell is the first logic state or the second logic state.

22. The electronic memory apparatus of claim 20, wherein the controller is operable to:

measure a temperature of a memory array that includes the ferroelectric memory cell, wherein the first time period is based at least in part on the temperature; or

measure a number of access operations performed on the ferroelectric memory cell, wherein the first time period is based at least in part on the number of access operations of the ferroelectric memory cell; and

modify a value of the first time period based at least in part on a measured temperature or the number of access operations, or both.

23. The electronic memory apparatus of claim 22, wherein the controller is operable to:

initiate a timer after the first logic state is written, wherein a value of the timer indicates whether the ferroelectric memory cell has stored the first logic state for the first time period.

24. An electronic memory apparatus, comprising:

means for determining that a ferroelectric memory cell has stored a first logic state for a first time period;

means for writing a second logic state to the ferroelectric memory cell based at least in part on the determining that the ferroelectric memory cell has stored the first logic state for the first time period, wherein the second logic state is different from the first logic state; and

means for updating a value of an indicator based at least in part on writing the second logic state to the ferroelectric memory cell, wherein the updated value of the indicator indicates that an intended logic state of the ferroelectric memory cell is the first logic state.

25. The electronic memory apparatus of claim 24, further comprising:

means for storing the indicator in a latch that comprises a non-volatile memory cell, wherein the value of the indicator indicates whether the intended logic state of the ferroelectric memory cell is the first logic state or the second logic state.

26. The electronic memory apparatus of claim 24, further comprising:

means for measuring a temperature of a memory array that includes the ferroelectric memory cell, wherein the first time period is based at least in part on the temperature; or

means for measuring a number of access operations performed on the ferroelectric memory cell, wherein the first time period is based at least in part on the number of access operations of the ferroelectric memory cell; and

means for modifying a value of the first time period based at least in part on a measured temperature or the number of access operations, or both.

27. The electronic memory apparatus of claim 26, further comprising:

means for initiating a timer after the first logic state is written, wherein a value of the timer indicates whether the ferroelectric memory cell has stored the first logic state for the first time period.