WHAT IS CLAIMED IS:

1. An application processor comprising:

a central processing unit;

a root complex that communicates with an external device under control of the central processing unit, generates a state change interrupt when an operation state changes, and store information indicating success or fail of the changed operation state into a state register; and

an interrupt aggregation and debug unit that performs debugging on a component associated with the state change interrupt by checking the information stored in the state register in response to receiving the state change interrupt to determine whether a recovery is needed.

2. The application processor of claim 1, wherein the root complex generates the state change interrupt in response to change of a power saving state of the root complex.

3. The application processor of claim 2, wherein the change of the power saving state includes a change according to active state power management (ASPM).

4. The application processor of claim 1 or claim 2, wherein the root complex generates the state change interrupt in response to activating or deactivating a phase locked loop.

5. The application processor of any one of claims 1 to 4, further comprising:

a bus connected with the central processing unit that communicates with the central processing unit depending on a first communication scheme; and

a bridge connected with the bus that changes the first communication scheme to a second communication scheme, wherein:

the root complex includes:

a first interface that communicates with the bus depending on the first communication scheme; and

a second interface that communicates with the bridge depending on the second communication scheme.

6. The application processor of claim 5, wherein the interrupt aggregation and debug unit performs the debugging by checking the state register of the root complex through the bus and the first interface.

7. The application processor of claim 5 or claim 6, wherein the interrupt aggregation and debug unit performs the debugging by checking the state register of an external device, which is connected with the root complex, through the bus and the root complex.

8. The application processor of any one of claims 5 to 7, wherein the interrupt aggregation and debug unit performs the debugging by checking the state register associated with the second interface through the bus, the bridge, and the second interface.

9. The application processor of any one of claims 1 to 8, wherein the interrupt aggregation and debug unit performs the recovery from a malfunction of the root complex depending on the information.

10. The application processor of claim 9, wherein the interrupt aggregation and debug unit performs the recovery from the malfunction by initializing a value of a register in the root complex depending on the information.

11. The application processor of claim 9 or claim 10, wherein the interrupt aggregation and debug unit performs the recovery from the malfunction by initializing a value of a register in an external device, which is connected to the root complex, through the root complex depending on the information.

12. The application processor of any one of claims 1 to 11, wherein:

the root complex includes a phase locked loop, and

the information includes whether a lock of the phase locked loop is achieved.

13. The application processor of claim 12, wherein the interrupt aggregation and debug unit performs recovering for initialization of the phase locked loop when the lock of the phase locked loop fails.

14. The application processor of any one of claims 1 to 13, wherein the interrupt aggregation and debug unit clears the state change interrupt without sending the state change interrupt to the central processing unit.

15. The application processor of any one of claims 1 to 14, wherein the interrupt aggregation and debug unit:

increases an interrupt count when an interrupt designated for aggregation is received from the root complex; and

sends an interrupt to the central processing unit when the interrupt count reaches a threshold value.

16. An automotive electronic processor comprising:

a central processing unit;

a root complex that communicates with an external device under control of the central processing unit and to generate an interrupt when an operation state changes and store information indicating success or fail of the changed operation state into a register; and

an interrupt aggregation and debug unit that performs debugging on a component associated with the interrupt by checking the information stored in the register in response to receiving the interrupt to determine whether a recovery is needed, wherein the external device includes a brake controller, a steering controller, a power train controller, a lamp controller, an image controller, an engine controller, a battery controller, a wiper controller, a safety controller, or a display controller.

17. The automotive electronic processor of claim 16, wherein the interrupt aggregation and debug unit performs recovering of a malfunction depending on the information.

18. A computing device comprising:

an application processor and a device that communicate with each other, wherein:

the application processor includes:

a central processing unit;

a root complex that communicates with the device, generates an interrupt when an operation state of the device and the root complex changes, and store information indicating success or fail of the changed operation state into a register;

a bus that connects the central processing unit and the root complex; and

an interrupt aggregation and debug unit that communicates with the root complex through the bus,

the device includes an end point interface that communicates with the root complex, and

the interrupt aggregation and debug unit performs debugging of the end point interface by checking the information stored in the register in response to receiving the interrupt to determine whether a recovery is needed.

19. The computing device of claim 18, wherein the interrupt aggregation and debug unit:

increases an interrupt count in response to a data interrupt occurring while the root complex is communicating with the end point interface, and

sends an interrupt to the central processing unit when the interrupt count reaches a threshold value.

20. The computing device of claim 18 or claim 19, wherein the device includes at least one of a Wi-Fi modem, a solid-state drive, and a neuromorphic device.