

ABSTRACT OF THE DISCLOSURE

A memory device includes an output pin, a mode register, a signal generator configured to generate a detection clock output signal including one of a random data pattern and a hold data pattern in response to first and second control signals from the mode register, and output the detection clock output signal through the output pin. The random data pattern includes pseudo-random data generated by the memory device. The hold data pattern is a fixed pattern pre-stored in the memory device. The detection clock output signal is used for a clock and data recovery operation.

FIG. 1