

METHOD AND APPARATUS FOR PROVIDING REAL-TIME OPERATION IN A PERSONAL COMPUTER SYSTEM

FIELD OF THE INVENTION

The present invention relates to computer systems; more particularly, the present invention relates to executing real-time applications at a computer system.

BACKGROUND

5 Currently, personal computers are used for various applications in order to simplify tasks to be performed by a user. Nevertheless, conventional personal computers are unable to perform real-time applications. A real-time application is one in which the correctness of computations performed by a computer not only depends upon logical correctness of the computation, but also upon the time at
10 which the result is produced. If the timing constraints are not met, the system fails. For example, in a patriot missile application, a patriot must locate an incoming missile on a radar detection system and fire a defense missile before the incoming missile can destroy its target.

 It is difficult to execute real-time operations on conventional computer
15 systems operating with general-purpose operating systems such as Windows 98® or Windows NT® because general-purpose operating system kernels do not have the capability to respond to events within a given time restriction. In addition, the hardware platforms of typical computer systems do not generate events within the resolution of time required for execution.

20 In an operating system like Windows 98® there are no rules as to how application drivers are to treat events. For example, in some instances drivers may shut off a received event for up to five seconds before the event is processed. It is apparent that such a delay would be unacceptable for a real-time operation.

Therefore, it would be desirable to provide real-time function to a personal computer system.

BRIEF DESCRIPTION OF THE DRAWINGS

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The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention. The drawings, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

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Figure 1 is a block diagram of one embodiment of a computer system; and

Figure 2 is a block diagram of one embodiment of a non-symmetric processor.

DETAILED DESCRIPTION

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A method and apparatus for providing real-time operation in a personal computer system is described. In the following detailed description of the present invention numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

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Figure 1 is a block diagram of one embodiment of a computer system 100.

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Computer system 100 includes a central processing unit (processor) 105 coupled to processor bus 110. In one embodiment, processor 105 is an Intel architecture

processor in the Pentium® family of processors including the Pentium® II family and mobile Pentium® and Pentium® II processors available from Intel Corporation of Santa Clara, California. Alternatively, other processors may be used. Processor 105 may include a first level (L1) cache memory (not shown in
5 Figure 1).

In one embodiment, processor 105 is also coupled to cache memory 107, which is a second level (L2) cache memory, via dedicated cache bus 102. The L1 and L2 cache memories can also be integrated into a single device. Cache memory 107 is optional and is not required for computer system 100. In addition,
10 computer system 100 includes a non-symmetric processor (NSP) 109 coupled to cache memory 107 and processor bus 110. According to one embodiment, NSP is integrated with processor 105 and is implemented to execute real-time protocols at computer system 100.

Chip set 120 is also coupled to processor bus 110. In one embodiment, chip
15 set 120 is the 440BX chip set available from Intel Corporation; however, other chip sets can also be used. Chip set 120 may include a memory controller for controlling a main memory 113. Further, chipset 220 may also include an Accelerated Graphics Port (AGP) Specification Revision 2.0 interface 320 developed by Intel Corporation of Santa Clara, California. AGP interface 320 is
20 coupled to a video device 125 and handles video data requests to access main memory 113.

Main memory 113 is coupled to processor bus 110 through chip set 120. Main memory 113 and cache memory 107 store sequences of instructions that are

executed by processor 105 and NSP109. The sequences of instructions executed by processor 105 and NSP109 may be retrieved from main memory 113, cache memory 107, or any other storage device. Additional devices may also be coupled to processor bus 110, such as multiple main memory devices. Video device 125 is
5 also coupled to chip set 120. In one embodiment, video device includes a video monitor such as a cathode ray tube (CRT) or liquid crystal display (LCD) and necessary support circuitry.

Processor bus 110 is coupled to system bus 130 by chip set 120. In one embodiment, system bus 130 is a Peripheral Component Interconnect (PCI) bus
10 adhering to a Specification Revision 2.1 bus developed by the PCI Special Interest Group of Portland, Oregon; however, other bus standards may also be used. Multiple devices, such as audio device 127, may be coupled to system bus 130. According to one embodiment, a radio transceiver 129 is coupled to system bus 130. Radio transceiver 129 may be used to implement a communication interface
15 between computer system 100 and a remote device (not shown).

Bus bridge 140 couples system bus 130 to secondary bus 150. In one embodiment, secondary bus 150 is an Industry Standard Architecture (ISA) Specification Revision 1.0a bus developed by International Business Machines of Armonk, New York. However, other bus standards may also be used, for
20 example Extended Industry Standard Architecture (EISA) Specification Revision 3.12 developed by Compaq Computer, et al. Multiple devices, such as hard disk 153 and disk drive 154 may be coupled to secondary bus 150. Other devices, such as cursor control devices (not shown in Figure 1), may be coupled to secondary

bus 150.

Figure 2 is a block diagram of one embodiment of NSP 109. NSP 109 includes an event timer 220, an event mechanism 230, a digital signal processor 240 and a radio correlator 250. Event timer 220 is used as a mechanism to generate timer interrupts at event mechanism 240. According to one embodiment, timer 220 transmits a signal to event mechanism 230 at predetermined intervals. The signal indicates that event mechanism 230 is to generate a timer interrupt. According to one embodiment, timer interrupts are generated every 5 milliseconds. However, one of ordinary skill in the art will appreciate that other time intervals may be used to generate interrupts.

DSP 240 is coupled to event mechanism 230. According to one embodiment, NSP 109 implements a real-time operating system that executes real-time applications. Real-time applications are applications that have time constraints on aspects of their behavior. If the constraints are not met, the application either fails or needs to adapt gracefully to the operating conditions.

DSP 240 is integrated on the same semiconductor die as processor 105 and shares the memory resources of processor 105. Processor 105 operates with a general purpose operating system that executes non-real time application. According to one embodiment, processor 105 operates using the Windows 98® operating system developed by Microsoft Corporation of Redmond, Washington. However, one of ordinary skill in the art will appreciate that computer system 100 may be implemented using other general-purpose operating systems.

According to a further embodiment, the general-purpose operating system

regards DSP 240 as an input/output (I/O) subsystem. For example, the general-purpose operating system of processor 105 communicates with the real-time operating system as if the real-time operating system were a driver interface attempting to access the resources of processor 105. As a result, the general

5 purpose operating system provides non-pageable memory for execution of the real-time operating system by NSP 109.

Further, the general-purpose operating system is implemented such that no application driver operated by computer system 100 may disable interrupts longer than the predetermined time interval calculates at timer 220.

10 Consequently, the interrupt latency of computer system 100 is guaranteed, allowing computer system 100 to consistently respond to events and information in real-time.

Radio correlator 250 receives real-time data from a source external to computer system 100. Radio correlator 250 converts the received data from a

15 serial format to a parallel format. According to one embodiment, radio correlator is a wireless Bluetooth radio that may communicate with external devices via a Bluetooth interface developed by the Bluetooth Special Interest Group. However, in other embodiments, radio correlator 250 may be used to implement other communication devices (e.g., a baseband processor).

20 Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that any particular embodiment shown and described by way of illustration is in no way intended to

be considered limiting. Therefore, references to details of various embodiments are not intended to limit the scope of the claims which in themselves recite only those features regarded as the invention.

CLAIMS

What is claimed is:

1. A computer system comprising:
a central processing unit (CPU); and
a non-symmetric processor (NSP) coupled to the CPU, wherein the NSP is
integrated on the same semiconductor die as the CPU.
- 5 2. The computer system of claim 1 further comprising a cache memory
coupled to the CPU and the NSP, wherein both the CPU and the NSP share the
cache memory.
3. The computer system of claim 1 further comprising:
A processor bus coupled to the NSP and the CPU;
10 A chipset coupled to the processor bus; and
a main memory coupled to the chipset, wherein the CPU and the NSP
share the main memory.
4. The computer system of claim 1 wherein the CPU implements a general
purpose operating system and the NSP implements a real-time operating system.
- 15 5. The computer system of claim 4 wherein general purpose operating system
communicates with the real-time operating system as an input/output subsystem.

6. The computer system of claim 1 wherein the NSP comprises:
a digital signal processor (DSP);
an event mechanism coupled to the DSP; and
an event timer coupled to the event mechanism.
- 5 7. The computer system of claim 6 wherein the NSP further comprises a radio correlator coupled to the DSP.
8. The computer system of claim 7 wherein the radio correlator is a wireless Bluetooth radio.
9. A non-symmetric processor (NSP) comprising:
10 a digital signal processor (DSP);
an event mechanism coupled to the DSP; and
an event timer coupled to the event mechanism, wherein the NSP is integrated on the same semiconductor die as a central processing unit (CPU).
10. The computer system of claim 9 wherein the NSP further comprises a radio
15 correlator coupled to the DSP.
11. The computer system of claim 10 wherein the radio correlator is a wireless Bluetooth radio.
12. A computer system comprising:
a central processing unit (CPU); and
20 a digital signal processor (DSP), wherein the DSP is integrated on the same

semiconductor die as the CPU.

13. The computer system of claim 12 wherein the CPU implements a general purpose operating system and the DSP implements a real-time operating system.

14. The computer system of claim 13 wherein general purpose operating
5 system communicates with the real-time operating system as an input/output subsystem.

15. The computer system of claim 12 wherein the CPU and the DSP share access to a memory system.