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(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NJ 10504 (US).

(72) Inventors: **POGGE, Bernhard, H.**; 11 LaDue Road, Hopewell Junction, NY 12533 (US). **YU, Roy**; 18 Hankin Loop, Poughkeepsie, NY 12601 (US). **PRASAD, Chandrika**; 29 Sherwood Heights, Wappingers Falls, NY 12590 (US). **NARAYAN, Chandrasekhar**; 62 Kensington Drive, Hopewell Junction, NY 12533 (US).

(74) Agent: **ANDERSON, Jay, H.**; International Business Machines Corporation, Dept. 18G / Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

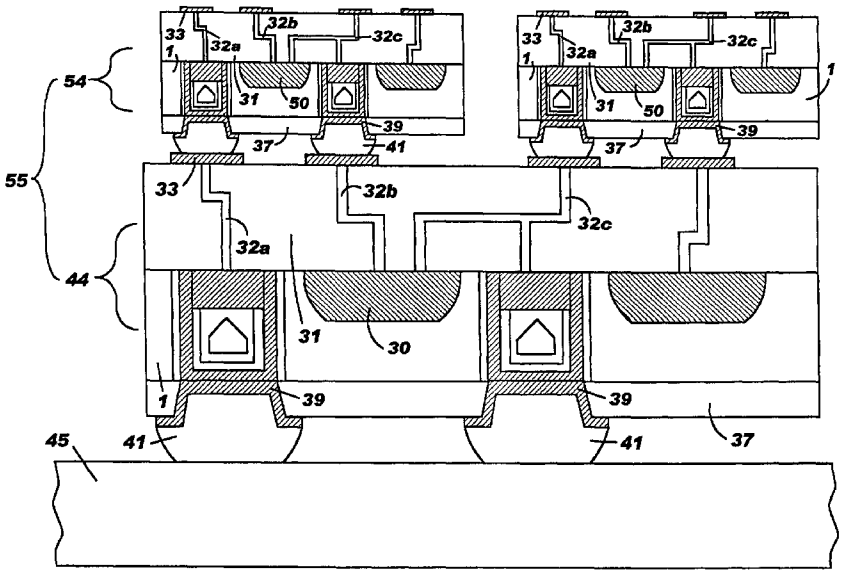
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(54) Title: CHIP AND WAFER INTEGRATION PROCESS USING VERTICAL CONNECTIONS



(57) Abstract: A process is described for semiconductor device integration at chip level or wafer level, in which vertical connections are formed through a substrate (1). A metallized feature (2) is formed in the top surface of a substrate, and a handling plate (35) is attached to the substrate. The substrate is then thinned at the bottom surface thereof to expose the bottom of the feature, to form a conducting through-via (20). The substrate may comprise a chip (44) having a device (30), e.g. a PE chip. The plate may be a wafer (65) attached to the substrate using a vertical stud/via interconnection. The substrate and plate may each have devices (30,60) fabricated therein, so that the process provides vertical wafer-level integration of the devices.

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