ABSTRACT

Embodiments of the present application provide an integrated circuit and a layout method thereof. First, a first pitch (P) of a first standard cell having a maximum gate length (X) in multiple standard cells (10) in an integrated circuit is determined. The first pitch (P) is a distance between a central axis of a polysilicon gate (21) in the first standard cell and central axes of virtual polysilicon gates (22) in the first standard cell. Then, a distance between a polysilicon gate (11) and virtual polysilicon gates (12) in each of the standard cells (10) is adjusted by using the first pitch (P) and a gate length (X) of each of the standard cells (10). After the adjustment, a distance between a central axis of the polysilicon gate (11) in each of the standard cells (10) and central axes of the virtual polysilicon gates (12) in each of the standard cells (10) is the same as the first pitch (P). In this way, after standard cells (10) having different gate lengths (X) are integrated, a size of a space occupied by each of the standard cells (10) is not affected by the gate length (X), thereby effectively reducing errors in key graphic dimensions during integrated circuit production and improving performance of the integrated circuit.

FIG. 3