

CLAIMS

What is claimed is:

- 5 1. An apparatus, comprising:
 one or more measurement sensors disposed to measure voltage applied to, or current
coupled to, one or more process stations of the apparatus;
 one or more analog-to-digital converters, coupled to an output port of a corresponding
one of the one or more measurement sensors, to provide a digital representation of a radio
10 frequency (RF) signal measured by the one or more measurement sensors; and
 a processor configured to:
 convert the digital representation of the RF signal measured by the one or more
measurement sensors from a time domain to a frequency domain representation; and to
 process the frequency domain representation of the RF signal by a sensor transfer
15 function to invert a phase lag of the one or more measurement sensors.
2. The apparatus of claim 1, wherein the processor is configured to invert the phase lag
of the one or more measurement sensors by multiplying an inverted transfer function of the one
or more measurement sensors by a frequency response of the one or more measurement sensors.
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3. The apparatus of claim 1, wherein the processor is configured to invert the phase lag
of the one or more measurement sensors by dividing a transfer function of the one or more
measurement sensors by a frequency response of the one or more measurement sensors.
- 25 4. The apparatus of claim 3, wherein the processor is configured to convert the digital
representation of the RF signal measured by the one or more measurement sensors from a time
domain to a frequency domain utilizing two or more Fast Fourier transform blocks arranged in
parallel.
- 30 5. The apparatus of claim 4, wherein each of the two or more Fast Fourier transform
blocks is arranged in parallel with a corresponding delay circuit.

6. The apparatus of claim 4, further comprising a digital inverter, wherein the digital inverter comprises a logic circuit to convey an output signal from the one or more measurement sensors to a first of the two or more Fast Fourier transform blocks during a first clock portion and
5 to convey the output signal from the one or more measurement sensors to a second of the two or more Fast Fourier transform blocks during a second clock portion.

7. The apparatus of claim 4, wherein the digital inverter comprises a concatenation block configured to join output signal representations from the two or more Fast Fourier transform
10 blocks arranged in parallel into a single output signal representation.

8. The apparatus of claim 7, further comprising a truncation block configured to truncate a size of the single output signal representation.

15 9. The apparatus of claim 8, wherein the truncation block comprises a sliding window configured to adjust binary digits of the single output signal representation.

10. The apparatus of claim 1, wherein the processor is configured to compute elements of a frequency response function during a calibration phase, and wherein inversion of
20 the frequency response function to provide the phase lag of the one or more measurement sensors occurs during a process performed by the one or more process stations of the apparatus.

11. An apparatus configured to a null out of a measurement sensor, comprising:
one or more analog-to-digital converters, coupled to an output port of a corresponding
25 one of one or more measurement sensors, to provide a digital representation of a radio frequency (RF) signal measured by the one or more measurement sensors; and
a processor, coupled to a memory, configured to convert the digital representation of the RF signal measured by the one or more measurement sensors from a first domain to a second domain and to process the signal converted to the second domain by a sensor transfer function to
30 invert a phase lag of the one or more measurement sensors.

12. An apparatus adapted to null out a phase lag of one or more measurement sensors, comprising:

- an analog-to-digital converter to convert an analog signal, obtained from one or more
5 output ports of a corresponding number of the one or more measurement sensors to measure power coupled to a multi-station integrated circuit fabrication chamber, to a digital representation;
- a detector to detect a frequency content of output signals of the one or more measurement sensors; and
- 10 a processor coupled to a memory to convert the digital representation of an RF signal measured by the one or more measurement sensors from a time domain to a frequency domain representation and process the frequency domain representation of the RF signal by a sensor transfer function to invert the phase lag of the one or more measurement sensors.

13. The apparatus of claim 12, wherein the detecting the frequency content of the output signals comprises determining a crossing of the digital representation of the output signal with a reference signal level; and

determine, utilizing the crossing of the digital representation of the signal measured by the one or more measurement sensors, a frequency content of the RF signal and the nulling-out
20 of the phase lag of the one or more measurement sensors.

14. The apparatus of claim 13, wherein the crossing corresponds to a RF signal ground.

15. The apparatus of claim 12, wherein the one or more measurement sensors comprises
25 a capacitive voltage transformer operating at any frequency between about 300 kHz and about 100 MHz.

16. The apparatus of claim 12, wherein the one or more measurement sensors comprises a current measurement sensor operating at a frequency of between about 300 kHz and about 100
30 MHz.

17. The apparatus of claim 12, wherein the nulling-out of phase lag of the one or more measurement sensors corresponds to canceling phase lag introduced by the one or more measurement sensors.

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18. The apparatus of claim 17, wherein a frequency response forms a frequency response function.

19. The apparatus of claim 18, wherein the processor is further configured to provide an estimate of RF power coupled to the multi-station integrated circuit fabrication chamber utilizing a signal received from the one or more measurement sensors that is advanced by an amount corresponding to the phase lag.

20. An apparatus adapted to measure a current signal or voltage signal, comprising:
an analog-to-digital converter to convert an analog signal, obtained from one or more output ports of a corresponding number of one or more measurement sensors to measure power coupled to a multi-station integrated circuit fabrication chamber, to a digital representation;
a detector to detect a frequency content of output signals of the one or more measurement sensors; and
a processor coupled to a memory to determine, in response to detecting the frequency content of the output signals of the one or more measurement sensors, a frequency response function of the one or more measurement sensors, the processor coupled to the memory additionally to null out a phase lag of the one or more measurement sensors by inverting a frequency response function of the one or more measurement sensors.

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21. The apparatus of claim 20, wherein the detecting the frequency content of the output signals of the one or more sensors comprises detecting a crossing of the digital representation of the obtained analog signal with a reference signal.

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22. The apparatus of claim 21, wherein the reference signal corresponds to a radio frequency (RF) ground.

23. The apparatus of claim 22, wherein a first measurement sensor of the corresponding number of the one or more measurement sensors comprises a voltage measurement sensor.

24. The apparatus of claim 23, wherein a second measurement sensor of the
5 corresponding number of measurement sensors comprises a current measurement sensor.

25. The apparatus of claim 24, wherein the processor applies a phase lag correction to measurements performed by the voltage measurement sensor and the current measurement sensor to obtain a corrected instantaneous voltage measurement and corrected instantaneous
10 current measurement.

26. The apparatus of claim 20, wherein the processor further operates to compute RF power delivered to the multi-station integrated circuit fabrication chamber by computing a product of a corrected instantaneous voltage and a corrected instantaneous current.
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27. The apparatus of claim 20, wherein the processor further operates to compute a moving average of successive computations of RF power delivered to the multi-station integrated circuit fabrication chamber to estimate average RF power delivered to the multi-station integrated circuit fabrication chamber.
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28. The apparatus of claim 20, wherein the processor further operates to compute real-time power delivered to a multi-station integrated circuit fabrication chamber utilizing real-time phase-corrected instantaneous voltage and real-time phase-corrected instantaneous current.

29. The apparatus of claim 28, wherein the processor further operates to modify an amount of power generated by a power generator, for coupling to the multi-station integrated circuit fabrication chamber, responsive to computing the real-time power delivered.
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30. The apparatus of claim 20, wherein the phase lag of the one or more measurement
30 sensors is determined in terms of clock periods.

31. An apparatus to estimate radio frequency (RF) power coupled to a load, comprising:
a current sensor having a current sensor frequency response function and a voltage sensor
having a voltage sensor frequency response function;
a first analog-to-digital converter coupled to an output port of the current sensor;
5 a second analog-to-digital converter coupled to an output port of the voltage sensor; and
a processor coupled to a memory to:
 obtain digital representations of instantaneous current and to obtain digital
 representations of instantaneous voltage;
 obtain a phase lag of the instantaneous current and the instantaneous voltage;
10 and
 invert the frequency response function of the current sensor and the frequency
 response function of the voltage sensor to counteract for the obtained phase lag of the
 instantaneous current and the instantaneous voltage.
- 15 32. The apparatus of claim 31, wherein the current sensor comprises an inductive current
transformer.
33. The apparatus of claim 31, wherein the voltage sensor comprises a capacitive voltage
transformer.
- 20 34. The apparatus of claim 31, wherein the current sensor and the voltage sensor operate
at any frequency between about 300 kHz and about 100 MHz.
35. An apparatus adapted to determine a phase lag of one or more measurement sensors,
25 comprising:
 an analog-to digital converter to convert an analog signal, obtained from one or more
 output ports of a corresponding number of the one or more measurement sensors to measure
 power coupled to a multi-station integrated circuit fabrication chamber, to a digital
 representation;
30 a detector to detect a sensor response characteristic from the digital representation of the
obtained analog signal; and

a processor coupled to a memory to determine, in response to detecting the sensor response characteristic, at least one frequency component present in the digital representation of the obtained analog signal, the processor coupled to the memory additionally to null out the phase lag of the one or more measurement sensors by inverting a frequency response function of the one or more measurement sensors.

36. The apparatus of claim 35, wherein the detector detects the sensor response characteristic by determining a crossing of the digital representation of the obtained analog signal with a reference signal.

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37. The apparatus of claim 36, wherein the detector detects the sensor response characteristic utilizing an analog representation of the reference signal.

38. The apparatus of claim 36, wherein the detector detects the sensor response characteristic utilizing a digital representation of the reference signal.

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39. The apparatus of claim 36, wherein the processor coupled to the memory determines the at least one frequency component present in the digital representation of the obtained analog signal in response to detecting the crossing of the digital representation of the obtained analog signal with the reference signal.

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40. The apparatus of claim 35, wherein the processor coupled to the memory performs the inverting of the frequency response function of the one or more measurement sensors in a frequency domain.

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41. The apparatus of claim 35, wherein the processor coupled to the memory performs the inverting of the frequency response function of the one or more measurement sensors in a time domain.

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