(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 July 2005 (07.07.2005)

PCT

(10) International Publication Number
WO 2005/060450 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2004/037059

(22) International Filing Date:
4 November 2004 (04.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/731,831 9 December 2003 (09.12.2003) US

(71) Applicant *(for all designated States except US)*: **FREESCALE SEMICONDUCTOR, INC.** [US/US]; 6501 William Cannon Drive West, Austin, TX 78735 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **SHIU, Hei Ming** [CN/CN]; 22G Blk. 5, Belvedere Garden Ph2,, Tsuen Wan, Hong Kong (CN). **CHOW, Wai Wong** [CN/CN]; 162C, 2/F, Jockey Club Road, Hong Kong (CN). **XU, Nan** [CN/CN]; NanKai HuaYuan Tian Hua Li 22-5-101#, Tianjin 300384 (CN).

(74) Agents: **KING, Robert, L.** et al.; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

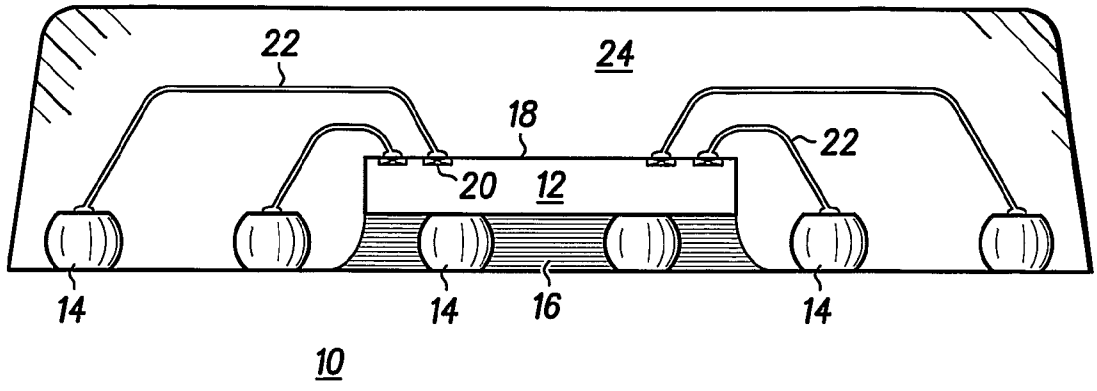
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME



(57) Abstract: A method of packaging an integrated circuit die (12) includes the steps of forming an array of soft conductive balls (14) in a fixture (30) and flattening opposing sides of the balls. The flattened balls are then transferred from the fixture to a mold masking tape (36). A first side of the IC die is attached to the balls with a die attach adhesive (16) and then wire bonding pads (20) on the die are electrically connected directly to respective balls with wires (22). An encapsulant (24) is formed over the die, the electrical connections, and a top portion of the formed balls. The tape is removed and adjacent, encapsulated dice are separated via saw singulation. The result is an encapsulated IC having a bottom side with exposed balls.

WO 2005/060450 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.