

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) IMPROVED RING COUNTER

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 5 Nagaike-cho, Abeno-ku, Osaka, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the
 10 following statement:—

The invention relates in general to a ring counter of radix n comprising a chain of n delay memory elements, and more particularly to a counter having circuits capable of
 15 production by the integrated circuit technique.

One of the current trends in the world electronic industries is the strenuous research in every branch of the industry into the so-called integrated circuits with a view
 20 to incorporation of the individual parts of a circuit into a single semi-conductive crystal. This is most important in the field of electronic computer engineering where various and systematic researches are
 25 being carried out for the application of integrated circuit techniques to the principal parts making up the electronic computer. This applies, for example, to ring counters applicable as timing counters and address counters, both of which are indispensable to the set up
 30 of an electronic computer.

Generally, the use of m flip-flop circuits is needed in setting up a counter of radix n (where $n \leq 2^m$); for example a decimal
 35 counter requires a minimum four flip-flop circuits to represent each of the decimal digits. In this decimal counter, the design is such that every input decimal digit gives rise to a different state of four bits of said
 40 circuits, for example the decimal digits 1, 2 3 and 4 give the states, as 0001 0010 0011 0100 Therefore, such a decimal counter must be provided with a decoder comprising ten AND gate circuits of the 4-input
 45 terminal type; this makes the application of

the counter impracticable for small circuit integration comprising a number of logic gate circuits.

In other words, the package of an integrated circuit has limited dimensions, so
 50 that the maximum number of the terminals is naturally limited for reasons of the space available for the package installation. A logical gate circuit, however, must inherently have
 55 at least a plurality of input terminals equivalent to the number of the inputs, one output terminal and another terminal or terminals required for the supply of power, and as a result is very likely to have an excessive number
 60 of the terminals. This is obviously not acceptable for obtaining a satisfactory integrated circuit due to the practical limitation on the maximum number of the terminals thereof, from the stand point of assuring
 65 improved integration density. As a practical example of a block of an integrated circuit, a large number of flip-flop circuits having 16-bit capacity can be contained in a register, while only two 2 AND gate circuits or two
 70 OR-gate circuits are acceptable in a logical gate circuit. For making a binary coded decimal counter, the maximum total number of the states realizable by four flip-flop circuits are $2^4 = 16$, so that six states must be reset
 75 to "0" by providing a feedback circuit including logical gate circuits. This also provides another source of difficulty preventing successful integration of the circuit.

On the other hand, a radix n ring counter having to comprise 'n' flip-flop circuits has an
 80 advantage that it needs no decoder for obtaining necessary decimal output. On the other hand there is the disadvantage that control of input-output between individual stages is usually complicated, in that the number of
 85 logical gate circuits which are needed results in unacceptability for miniaturization of the counter. The need for including logical gate circuits in the ring counter mentioned above is for the introduction of both setting input and
 90

resetting input into the counter as well as for resetting a flip-flop circuit whenever brought to the reset state. Besides the above mentioned essentials, a device must be incorporated to equalize the initial state of all the individual flip-flop circuits and more specifically, a suitable circuit capable of automatically correcting errors, if any, to the correct state at a high degree of reliability and accuracy.

5 The present invention provides a ring counter of radix n comprising a chain of delay memory elements which are connected in series and each of which has an output capable of assuming either of two states, said chain being capable of transferring an output state of the first of the elements sequentially to the remaining elements in response to a train of clock pulses applied to said elements, each element comprising a field effect transistor having a gate internal capacitance in which signals producing one of the output states are stored, said field effect transistor being capable of storing said signals only for a predetermined time and the counter therefore being operable only in response to clock pulses having a spacing less than said predetermined time to avoid loss of said signals; and a logical gate circuit controlled only by a plurality of said elements including the $n-1^{\text{th}}$ element to feed back a repeat signal to the first element and to cause the condition in which the output of only one memory element of the chain assumes a first of its states at any one time while the output of each of the remaining elements assumes the second of its states and to correct automatically any spurious departure of the memory elements from said condition.

10 In certain embodiments, the invention, as will become apparent from the following description relating to the accompanying drawings may make it possible to alleviate the difficulties mentioned by minimizing the necessary number of logical gate circuits in order to make a radix n counter acceptable for realization of a miniature integrated circuit, by avoiding the need for bringing a memory element (flip-flop) to the reset state thereof whenever a preceding memory element has been reset, by ease of carry-over of a given state in sequence along the chain of elements, by eliminating the need for special means to take care of the initial states of individual memory elements, and by enabling automatic correction of any errors which may occur when the counter is in operation.

15 Preferred embodiments of the invention will now be described with reference to the accompanying drawings in which,

Figure 1 shows a block diagram representing a first embodiment of the invention. 60

Figure 2 illustrates a full circuit diagram of the above mentioned first embodiment of the invention. 65

Figure 3 shows the wave form of potential at various points in the circuit illustrated in Figure 2. 70

Figure 4 illustrates a full circuit diagram representing a second embodiment of the invention. 75

Figure 5 shows a full circuit diagram representing a third embodiment of the invention. 80

Figure 6 is a full circuit diagram representing a fourth embodiment of the invention. 85

Figures 7a, 7b and 7c illustrate the circuits of three other examples of memory elements (flip-flop circuits) which can be used in the counter according to the present invention. 90

In the first embodiment of the invention shown in Figure 1, $x_1, x_2, \dots, x_{n-1}, x_n$ are individual delay memory elements (specifically delay flip-flop circuits) and the output signal of an element is carried over to the element subsequent thereto in the series, the input terminal of each element being connected to the output terminal of the preceding element, so as to cause or allow the successive carry-over of the state of a memory element through to the last element. A common clock pulse is applied to all the memory elements for controlling their function. G represents an $(n-1)$ input OR gate circuit, i.e. subject to inputs from all the memory elements except one in the last stage, the output thereof being fed back to the memory element in the first stage. I is an inverter having a characteristic NOT function and serving to cause a feedback of the output of the above mentioned gate circuit to the memory element in the first stage. 95

Assume now that the output state of each memory is characterized by denoting the binary digits "1" and "0". The binary digit "1" obtained from the memory element in the first stage in an initial state is carried successively over to the subsequent elements, in synchronism with the clock pulses, until the last element is reached, when all the memory elements except the last is in the "0" state. Then binary digit "1" is applied again to the first stage element. The changes of the state in the memory elements are listed below, which in themselves are not new and are the same as those of the conventionally known ring counter. 100 105 110

Change of State

Time	x_1	x_2	x_3	$x_4 \dots x_{n-1}$	x_n
t_0	1	0	0	0 0	0
t_1	0	1	0	0 0	0
t_2	0	0	1	0 0	0
t_3	0	0	0	1 0	0
$\vdots$					
t_{n-2}	0	0	0	0 1	0
t_{n-1}	0	0	0	0 0	1

The example shown above is an embodiment of the invention where at any one time, only one of the memory elements is allowed to be in state of "1" and all the remainder are in a state of "0", in which case the following equation is applicable for individual memory elements;

$$x_1^{t+1} = \frac{1}{(x_1 + x_2 + \dots + x_{n-1})^t}$$

$$x_2^{t+1} = x_1^t$$

$$x_3^{t+1} = x_2^t$$

$$\vdots$$

$$x_n^{t+1} = x_{n-1}^t$$

in which: $t, t+1$ represent consecutive time intervals.

As is readily seen from above, it is sufficient to connect the output of the logical gate circuit to the first of the memory elements only, the remainder of the memory elements being so made that they perform the function of shifting only. It is to be noted that in this embodiment of the invention the state of the output from the last of the memory elements is not taken account of in establishing the application equation described above.

An embodiment of the invention according to the foregoing example and comprising elements of a type which is acceptable for inclusion into an integrated circuit, including a field effect transistor, type MOS, characterized by P channel enhancement, will be explained in detail in conjunction with Figure

2 in which the sections enclosed by the dash line are delay flip-flop circuits having an identical diagrammatic construction. The flip-flop x_2 in the second stage is chosen for explanation in the following description. The transistors T_{21}, T_{22} and T_{23} operate as a memory element functioning according to the storage of the internal capacity of their gate electrodes, while other transistors T_{24}, T_{25} and T_{26} serve as a switching means operating either to open or to close electronically, depending on whether the clock pulses ϕ_1 and ϕ_2 are present or not. The gate electrodes of the transistors T_{21}, T_{22} and T_{23} are each connected to the output terminal drain of the transistor stage which precedes it, while the source electrodes of the same transistors are earthed and the drain electrodes thereof are connected to the source of potential $-V_{DD}$ through a load resistance. The gate electrodes of the switching transistors T_{24} and T_{26} are connected to the terminal for introduction of the clock pulses ϕ_1 and the gate electrode of the transistor T_{25} is connected to the source of clock pulses ϕ_2 , while their source electrodes and the drain electrodes are placed in the information route in the flip-flop circuit.

The operating principle of the circuit set up by the above mentioned transistors and connections is as described below.

For better understanding of the disclosure which follows hereinbelow, the potential of the information signals is assumed to correspond to "0" or "1" in binary digits to provide a positive logical system in which 0 volts and $-V_{DD}$ volts represent the states of "1" and "0" respectively and which operate as follows.

The input information is applied to the source electrode of the transistor T_{24} and the clock pulse ϕ_1 having been applied to the

switching transistors at the time t_1 , the transistor T_{24} becomes conductive (ON), resulting in application of the potential representing the input information to the gate electrode (at Point A) of the transistor T_{21} , with no drop of voltage whatsoever. If the input information is a potential of 0 volts (corresponding to binary "1"), the transistor T_{21} becomes non-conductive (OFF), resulting in no accumulation whatsoever of the charge by the internal capacity of the gate electrode. Under such condition, the transistor T_{21} itself is rendered resistive, and resultantly the drain potential (at Point B) is approximately $-V_{DD}$ volts.

Then at the second time of t_2 , the clock pulse ϕ_2 is applied to the gate electrode of the transistor T_{25} which becomes conductive to cause the circuit to be closed, and subsequently, the drain potential of the transistor T_{21} is carried over to the gate electrode (at Point C) of the transistor in the subsequent stage. The drain potential of the transistor T_{21} is now $-V_{DD}$ volts, so that the transistor T_{22} is changed in the conductive state and as a result charge is accumulated by the internal capacity of the gate electrode until the gate potential become $-V_{DD}$ volts. Even after having been rendered electronically opened by the transistor T_{25} , the information is stored by the internal capacity of the gate electrode of said transistor. Under such condition of the transistor T_{25} , the drain potential (at point D) becomes 0 volts, if the internal resistance of the other transistor T_{22} is neglected. This corresponds to a binary digit "1" and means that the state of the drain potential corresponds to the input information occurring with a delay time equivalent to one cycle (1 bit time) of the clock pulse.

On the other hand, if the input information is a potential of $-V_{DD}$ volts (corresponding to binary "0") the transistor T_{21} becomes conductive (ON) with the application of the clock pulse ϕ_1 and the drain potential (at point B) becomes, therefore, approximately 0 volts. At this time, a negative potential charge is stored in the internal capacitance of the gate electrode of the transistor T_{21} . Then, while the clock pulse ϕ_2 is impressed on the transistor T_{25} , a zero potential is transmitted through the transistor T_{25} to the gate electrode of the transistor T_{22} and the transistor T_{22} becomes non-conductive (OFF). As a result the drain potential (at point D) becomes $-V_{DD}$ volts, which corresponds to a binary digit "0".

The clock pulses ϕ_1 and ϕ_2 are regularly periodical as illustrated in the accompanying drawing which results in the consecutive operation of the memory elements.

Further, in conjunction with the above described example of the embodiment of the invention, in order to counteract leakage of the stored charge due to the characteristic limit imposed on the effective storage time by

the internal capacity of the gate electrode inherent in a MOS type of field effect transistor, an information recirculation loop is established by connection of the transistor T_{23} to the input side (gate electrode) of the transistor T_{22} through the transistor T_{26} , which effects electronic switching in synchronism with the clock pulse ϕ_1 through the feedback loop to the gate of the preceding transistor T_{22} .

The information transfer within the memory element X2 is as follows:—

The information stored in the transistor T_{21} is transferred, synchronized with the clock pulse ϕ_2 applied to switching transistor T_{25} , to another transistor T_{22} as well as to the transistor T_{23} . It should be noted that the transfer of the information from said transistor T_{22} is accomplished, with the phase of the pulse inverted.

For example, in the case where the transistor T_{21} has stored a negative charge in the internal capacitor of its gate electrode and remained in the conductive state, the zero potential then existing at the drain terminal (point B) of the transistor T_{21} is transferred to the gate electrode of the transistor T_{22} , by the switching on of transistor T_{25} so that T_{22} then reverts into the non-conductive state. A negative potential at said drain terminal of the transistor T_{21} gives rise directly to the change of the transistor T_{22} into the conductive state and the simultaneous starting of storing the negative charge in the internal capacitor of the transistor T_{22} .

There is, however, the possibility of the premature decay of the stored charge on the transistor gate due to the presence of the leak impedance in the gate internal capacitance, resulting in the exhaustion of the memory information. This means that the clock pulse period is subject to a certain limit.

In view of this, a feed back loop is established to operate upon arrival of the pulse ϕ_1 , to the transistor T_{22} , thereby enabling clock pulse period, so that said loop serves to feed back the information stored in the transistor T_{23} , in synchronism with the clock pulse ϕ_1 , to the transistor T_{22} , thereby enabling the renewed writing of the same information as in the previous period in the transistor T_{22} .

That is to say that the drain potential (zero) of the transistor T_{23} , the gate thereof having been negatively charged, causes the transistor T_{22} to be turned into the non-conductive state through the switching transistor T_{26} , while the resulting negative potential at the drain terminal of the transistor T_{22} causes the transistor T_{23} to regain the same conductive state as before the application of the previous clock pulse ϕ_1 .

Repetition of the electronic action synchronised with the clock pulse ϕ_1 as mentioned above allows the maintenance of the information circulated in the flip flop circuit,

and accordingly the proper action of the circuit is not subject to any limitation whatsoever imposed upon the storage time of the information in the transistor.

To the output side of the flip-flop circuits, except one in the last stage, are connected the diodes $D_{11}, D_{12}, \dots, D_{1n-1}$, to set up the OR gate circuit to which the source voltage is through a suitable resistance. This OR gate circuit provides a gating function in a manner as described below.

When the counter is being operated to perform normal counting at zero output voltage of one of the memory elements, the diode D_{1i} ($1 \leq i \leq n-1$) connected to a memory element where output is in the binary "1" state becomes conductive (ON), and the OR gate output assumes the state "1". Between the logical gate circuit and the first memory element is an inverting transistor T_{11} (corresponding to the inverter I of Fig. 1) which is then cut off and accordingly has no effect whatsoever on the first memory element. On the other hand, when the output of all the memory elements, other than the last, are in "0" state, all the diodes $D_{11}, D_{12}, \dots, D_{1n-1}$ becomes nonconductive, giving rise to a drop of the gate potential of the transistor T_{11} down to $-V_{DD}$ volt, which in its turn causes the transistor T_{11} to become conductive and the drain potential to rise up to 0 volt. In this way, the information "1" is put into the first memory element to initiate the ring counting action of the counter, which is repeated by subsequent inputs of the information signal.

The arrangement of the circuit disclosed hereinabove offers various counting advantages as described below:

First, any counter of conventional design, composed of binary memory elements (flip-flop circuits) and a decoder, has the inherent disadvantage that any change of the number, results in an appreciable change of the input condition of the logical gate circuit, and sometimes needs even an additional memory element or elements and a large change of the matrix for the decoder. However in the arrangement according to the present embodiment of the invention, a change of the number requires only a minus or plus change of the number of the memory elements, apart from the change of the number of the input to the NOR gate circuit (OR gate circuit plus the inverter). This is a great advantage inherent to the counter in accordance with the invention in that an unusually easy-to-make circuit may be had by a combination of n-bit shift registers and a single logical gate circuit.

Second, considering the composition of the extra-small integrated circuit in a counter, a large number of integrated circuit devices is needed for making the decoder in the conventional type of counter, which comprises a

large number of the logical gate circuits. Generally, only two AND gate circuits can be contained in one block of a conventional integrated circuit. However, four flip-flop circuits may be accommodated with ease in such a circuit. The present embodiment of the invention eliminates the necessity for increasing the number of the blocks of the integrated circuits in excess of the number used with a conventional counter.

Thirdly, this embodiment of the invention involves the use of n delay memory elements which, unlike a counter comprising R—S memory elements (R—S type of flip-flop circuit), is free from the need for control of state in the individual stages.

Fourthly, in accordance with this embodiment of the invention, the operative state is defined by the equation

$$x_{i+1} = \frac{1}{(x_1 + x_2 + \dots + x_{n-1})^2},$$

so that the required operating condition is not affected by the initial state of the elements, with the result that the state of the memory elements can always be kept correct. Mistakes, if any, taking place during the counting, are likewise concerned automatically.

As will be evident from the foregoing description with reference to the first embodiment the logical design of the gate circuit G is such as to achieve a unique memory state of only one of the individual memory elements, at any given time, i.e. a state different from that of remainder, whenever the output side of a memory element, for example, the transistor T_{23} of the memory element X_2 is in the conductive state, the transistor on the output side of all the other memory elements become, according to this invention, non-conductive.

This is accomplished in the embodiment of the invention, represented by Fig. 2, according to a logic design of the logic gate with the characteristic in accordance with the above equation. Such an embodiment affords the possibility, as an advantageous feature of this invention of correcting automatically a spurious state of the counter contrary to the above mentioned rule, as will be understood by reference to the "states" table appearing hereunder.

Such errors may be developed by external influence, such as excessive fluctuation of the source voltage and occurrence of abnormal noise etc. in the course of the counting operation.

This advantage contrasts with known ring counters, wherein, if any abnormal state occurs, it is not corrected.

Another advantage which is achieved is the possibility of starting the counting operation upon the application of the source voltage,

without need for a special signal to be applied from outside. The significance of this is that even when more than one of the memory elements have assumed a state different from

the remainder, the pre-starting state of equality of all the memory elements can be automatically achieved.

5

Change of State

Time	x_1	x_2	x_3	x_4	x_5
t_0	1	0	1	1	0 ...
t_1	0	1	0	1	1
t_2	0	0	1	0	1
t_3	0	0	0	1	0 ...
t_4	0	0	0	0	1
t_5	1	0	0	0	0

...Erroneous state

...State after correction

10 Fifthly, there is no need for use of a decoder because only one of n memory elements is in state of "1" while all others are in state of "0". This advantage in turn contributes greatly to the minimization of the difficulty of cross over of the congested information lines, for example on a printed circuit base on which a counter could be mounted, besides the reduction of total space required for installation of said elements on the printed circuit base. It is to be noted that this advantage is true not only in case of the embodi-

ment of the invention described precedingly, but also, in other cases of the embodiments as will be disclosed hereinafter.

25 In the second embodiment of the invention the operating principle is the same as in the preceding first example, with the difference that, in this second example, only one of the memory elements is in the state of "0", all others being in the state of "1", as illustrated in the following chart of output states covering all the flip-flop circuits.

25

30

Time	x_1	x_2	x_3	$x_4 \dots \dots x_{n-1}$	x_n
t_0	0	1	1	1	1
t_1	1	0	1	1	1
t_2	1	1	0	1	1
t_3	1	1	1	0	1
$\vdots$					
$\vdots$					
$\vdots$					
t_{n-2}	1	1	1	1	0
t_{n-1}	1	1	1	1	1

The equation for any stage of flip-flop circuit can be given by

$$x_1^{t+1} = \frac{1}{(x_1 \quad x_2 \dots x_{n-1})^t}$$

$$x_2^{t+1} = x_1^t$$

⋮

⋮

$$x_n^{t+1} = x_{n-1}^t$$

A specific description for this type of example embodying the invention where MOS type field effect transistors are incorporated as in the preceding example will be described with reference to Figure 4.

In this example only the logical gate circuit differs from the preceding example, the memory elements as a whole being the same, in that to the output side of all the flip-flop circuits except that in the last stage are connected the diodes $D_{21}, D_{22}, \dots, D_{2n-1}$ with the polarity thereof reversed relating to the preceding example. These diodes are earthed through a resistance.

Gate action in this circuit is performed according to the following principle:

When normal counting is being carried out,

one of the memory elements is delivering an output voltage of $-V_{DD}$, and only the diode D_{21} ($1 \leq i \leq n-1$) which is connected to this memory element is conductive, the logical gate output thereof being in the state "0" (V_{DD} volts). The negative potential output of said memory element is applied to the inverting transistor T_{11} which then becomes conductive. The drain potential of the transistor T_{11} is 0 volts, thus exerting no effect whatsoever on the first memory element. However, when all the memory elements except that in the last stage are in the state "1", all the diodes $D_{21}, D_{22}, \dots, D_{2n-1}$ are non-conductive, resulting in absence of negative potential applied to the gate electrode of the transistor T_{11} which in turn brings the transistor to its non-conductive state. Under such condition, the drain potential of the transistor T_{11} is $-V_{DD}$ volts, causing the application of the binary digit "0" to the first memory element thus transmitting the order for continuation of the counting operation.

A third embodiment of the invention is a counter having a simpler logical gate circuit and representing a version of the first example already described. In this third embodiment all of the n memory elements are brought into the state "1" simultaneously, when the source voltage is applied. The example of the change of states in individual stages and the truth value are as listed below:

Change of State

Time	x_1	x_2	x_3	$x_4 \dots x_{n-1}$	x_n
t_0	1	1	1	1	1
t_1	0	1	1	1	1
t_2	0	0	1	1	1
t_3	0	0	0	1	1
t_{n-1}	0	0	0	0	1
t_n	0	0	0	0	0
t_{n+1}	0	1	0	0	0
t_{n+2}	0	0	1	0	0
t_{n+3}	0	0	0	1	0

repeated
subsequently

Truth Table

Time t		Time (t+1)
x_{n-1}	x_n	x_1
1	1	0
1	0	0
0	1	1
0	0	0

The application equations applicable to the individual memory elements may be expressed as follows, from the above example of change of state and listed truth values.

$$x_1^{t+1} = \frac{1}{(x_{n-1} \cdot x_n)^t}$$

$$x_2^{t+1} = x_1^t$$

$$\vdots$$

$$x_n^{t+1} = x_{n-1}^t$$

- 5 An example of the third embodiment will be described with reference to Figure 5. In this example of the invention the difference from the first example lies only in the logical gate circuit and the switch determining the initial state of individual memory elements.
- 10 The logical gate circuit comprises four transistors, T_{31} to T_{34} of which the gate electrode, the source electrode and the drain electrode of the transistor T_{31} are connected to the output side of the last memory element, earth and the $-V_{DD}$ source respectively. The transistor T_{32} and its gate electrode connected to the (n-1)th memory element through the transistor T_{33} . Both transistor T_{31} and T_{32} jointly set up an AND input gate. The transistor T_{33} offers a "NOT" action and has its gate electrode connected direct to the drain electrode of the transistor T_{22} of the (n-1)th memory element. The transistor T_{34} provides an outlet for output delivery of the gate circuit and has its gate electrode in direct connection to the drain electrodes of the transistors T_{31} and T_{32} .

In this type of circuit connection, when the output (the drain potential of transistor T_{22}) of the (n-1)th memory element is 0 volts and that of the nth memory element is $-V_{DD}$ volts, the transistors T_{31} and T_{32} are conductive and the gate potential of the transistor T_{34} is raised up to 0 volts, so that the transistor T_{34} on the output side of the logical gate is rendered non-conductive. This means that the binary digit "0" is applied to the first memory element and no order for counting is given through the transistor T_{34} . But, in the case where the last two memory elements are in the reverse state to that described above both transistors T_{31} and T_{32} are non-conductive, so that the binary digit "1" is applied to the first memory element.

A switch S_{31} is connected to the transistor T_{34} to set the initial state of the circuit. The switch has one of its terminals earthed and the other connected to the first memory element. This means that the information "1" i.e. 0 volts is applied to the first memory element through the switch S_{31} , throughout the period that the switch is kept closed (at least n-bit times), in order to keep the whole circuit in the state "1" for that period.

A fourth example embodying the invention provides a counter comprising a logical gate of a type made simpler than that in the second example for bringing all of the n flip-flop circuits to an initial state "0". An example of the change of state in the individual memory elements of the counter operating with the initial state properly established for the memory elements and the truth table therefore are as follows:

Change of State

Time	x_1	x_2	x_3	$x_4 \dots x_{n-1}$	x_n
t_0	0	0	0	0 0	0
t_1	1	0	0	0 0	0
t_2	1	1	0	0 0	0
t_3	1	1	1	0 0	0
t_{n-1}	1	1	1	1 1	0
t_n	0	1	1	1 1	1
t_{n+1}	1	0	1	1 1	1
t_{n+2}	1	1	0	1 1	1
t_{n+3}	1	1	1	0 1	1

repeated
subsequently

Truth Table

Time t		Time (t,1)
x_{n-1}	x_n	x_1
1	1	1
1	0	0
0	1	1
0	0	1

From the above change of state and the truth table, the application equation for all the flip-flop circuits may be described as given in the following:

$$x_1^{t+1} = \overline{(x_{n-1} x_n)^t}$$

$$x_2^{t+1} = x_1^t$$

$$\vdots$$

$$\vdots$$

$$x_n^{t+1} = x_{n-1}^t$$

from the preceding third example only in that the logical gate and the switch defining the initial state are somewhat dissimilar from the ones in the third example, and comprise a transistor T_{41} for "NOT" action and three other transistors T_{42} , T_{43} and T_{44} to set up an OR logical gate. A switch S_{41} designed for determining the initial state is to apply the information of state "0" to the first memory element. When switch S_{41} is closed, the gate potential of the transistor T_{44} is held at 0 volts thus keeping the transistor in the non-conductive state. The drain potential of T_{44} is thus $-V_{DD}$, corresponding to binary digit "0" which is thus applied to the input of the first memory element for as long as the switch S_{41} is held closed.

This embodiment is illustrated in conjunction with Figure 6. This embodiment differs

In operation, when the outputs of both stages x_{n-1} and x_n are at 0 volts, i.e. binary digit "1", transistors T_{41} and T_{43} are non-conductive, and transistor T_{42} is conductive. Transistor T_{44} is thus conductive due to the source potential $-V_{DD}$ applied to its gate electrode and a potential of 0 volts is applied to the input of the first memory element. When however the output of memory element x_n is at $-V_{DD}$ volts, transistor T_{43} becomes conductive, thus connecting the source of transistor T_{42} and hence the gate of transistor T_{44} to earth. Transistor T_{44} is now non-conductive and a voltage $-V_{DD}$ is re-applied to the input of the first memory element. If the outputs of both stages x_n and x_{n-1} are at $-V_{DD}$ volts, transistor T_{41} becomes conductive, thus connecting the gate of transistor T_{42} to earth and rendering it non-conductive thus preventing the switching-off of transistor T_{44} so that 0 volts continue to be applied to the input of the first memory element.

Figures A—C illustrate three alternative embodiments for the delay memory elements for the counter which can be used in place of the elements shown in Figures 2—6. In Figure 7A, transistors T_{51} and T_{52} are connected between the drain and gate of transistor T_{21} to replace the transistors T_{23} and T_{24} of the previously described embodiments. In Figure 7B a third clock pulse ϕ_3 is introduced to control the action of a transistor T_{53} connected between the drain of transistor T_{22} and the gate of transistor T_{21} . The action of the transistor T_{53} is to provide a feedback path to ensure that the circuit remains in the state in which it is set by the input signal. At the time of the clock pulse ϕ_3 , T_{53} becomes conducting to transmit the drain potential of T_{22} to the gate of T_{21} .

In Figure 7C, transistors T_{54} , T_{55} and T_{56} are connected as shown. The operation of this circuit is such that only one source of clock pulses ϕ_2 , is required.

These examples in Figures 7A—C correspond, in the general principle of wiring connection and function, to all other examples illustrated in the preceding figures of circuit diagrams. Any section in Figure 7 not similarly shown in the circuit diagrams in the previous figures is of no special significance in connection with the invention.

WHAT WE CLAIM IS:—

1. A ring counter of radix n comprising a chain of delay memory elements which are connected in series and each of which has an output capable of assuming either two states, said chain being capable of transferring an output state of the first of the elements sequentially to the remaining elements in response to a train of clock pulses applied to said elements, each element comprising a field effect transistor having a gate internal capacitance in which signals producing one of the output states are stored, said field effect

transistor being capable of storing said signals only for a predetermined time and the counter therefore being operable only in response to clock pulses having a spacing less than said predetermined time to avoid loss of said signals; and a logical gate circuit controlled by a plurality of said elements including the $n-1^{\text{th}}$ element to feed back a repeat signal to the first element and to cause the condition in which the output of only one memory element of the chain assumes a first of its states at any one time while the output of each of the remaining elements assumes the second of its states and to correct automatically any spurious departure of the memory elements from said condition.

2. A ring counter as claimed in claim 1, wherein each delay memory element includes further transistors through which said signals are applied to said internal gate capacitance in response to the clock pulses.

3. A ring counter as claimed in claim 1 or 2, wherein each delay memory element includes an internal feed back loop to renew the stored signal in response to succeeding clock pulses in accordance with the state of the output of the element.

4. A ring counter as claimed in any preceding claim, wherein the logical gate circuit operates such that said first state is the state corresponding to the presence of a signal stored in said internal capacitance and said second state is the state corresponding to absence of a signal stored in said gate internal capacitance.

5. A ring counter as claimed in claim 4, wherein the logical gate circuit comprises a plurality of mono-directional conductive elements which each have one end connected to the output of a respective one of said memory elements except for the n^{th} delay element, the other ends of said mono-directional conductive elements being connected together to make up a logical circuit for "OR" gating, the output thereof being fed back to the input of the first of said memory elements through an element to provide a "NOT" function.

6. A ring counter as claimed in any preceding claim, wherein the logical gate circuit operates such that said first state is the state corresponding to absence of a signal stored in said internal capacitance and said second state is the state corresponding to the presence of a signal stored in said internal capacitance.

8. A ring counter as claimed in claim 7, wherein the logical gate circuit comprises a plurality of mono-directional conductive elements which each have one end connected to the output of a respective one of said memory elements except for the n^{th} delay element, the other end of said mono-directional conductive elements being connected together to make up a logical circuit for "AND" gating, the output thereof being fed back to the



In operation, when the outputs of both stages x_{n-1} and x_n are at 0 volts, i.e. binary digit "1", transistors T_{41} and T_{43} are non-conductive, and transistor T_{42} is conductive. Transistor T_{44} is thus conductive due to the source potential $-V_{DD}$ applied to its gate electrode and a potential of 0 volts is applied to the input of the first memory element. When however the output of memory element x_n is at $-V_{DD}$ volts, transistor T_{43} becomes conductive, thus connecting the source of transistor T_{42} and hence the gate of transistor T_{44} to earth. Transistor T_{44} is now non-conductive and a voltage $-V_{DD}$ is re-applied to the input of the first memory element. If the outputs of both stages x_n and x_{n-1} are at $-V_{DD}$ volts, transistor T_{41} becomes conductive, thus connecting the gate of transistor T_{42} to earth and rendering it non-conductive thus preventing the switching-off of transistor T_{44} so that 0 volts continue to be applied to the input of the first memory element.

Figures A—C illustrate three alternative embodiments for the delay memory elements for the counter which can be used in place of the elements shown in Figures 2—6. In Figure 7A, transistors T_{51} and T_{52} are connected between the drain and gate of transistor T_{21} to replace the transistors T_{23} and T_{26} of the previously described embodiments. In Figure 7B a third clock pulse ϕ_3 is introduced to control the action of a transistor T_{53} connected between the drain of transistor T_{22} and the gate of transistor T_{21} . The action of the transistor T_{53} is to provide a feedback path to ensure that the circuit remains in the state in which it is set by the input signal. At the time of the clock pulse ϕ_3 , T_{53} becomes conducting to transmit the drain potential of T_{22} to the gate of T_{21} .

In Figure 7C, transistors T_{54} , T_{55} and T_{56} are connected as shown. The operation of this circuit is such that only one source of clock pulses ϕ_2 , is required.

These examples in Figures 7A—C correspond, in the general principle of wiring connection and function, to all other examples illustrated in the preceding figures of circuit diagrams. Any section in Figure 7 not similarly shown in the circuit diagrams in the previous figures is of no special significance in connection with the invention.

WHAT WE CLAIM IS:—

1. A ring counter of radix n comprising a chain of delay memory elements which are connected in series and each of which has an output capable of assuming either two states, said chain being capable of transferring an output state of the first of the elements sequentially to the remaining elements in response to a train of clock pulses applied to said elements, each element comprising a field effect transistor having a gate internal capacitance in which signals producing one of the output states are stored, said field effect

transistor being capable of storing said signals only for a predetermined time and the counter therefore being operable only in response to clock pulses having a spacing less than said predetermined time to avoid loss of said signals; and a logical gate circuit controlled by a plurality of said elements including the $n-1^{\text{th}}$ element to feed back a repeat signal to the first element and to cause the condition in which the output of only one memory element of the chain assumes a first of its states at any one time while the output of each of the remaining elements assumes the second of its states and to correct automatically any spurious departure of the memory elements from said condition.

2. A ring counter as claimed in claim 1, wherein each delay memory element includes further transistors through which said signals are applied to said internal gate capacitance in response to the clock pulses.

3. A ring counter as claimed in claim 1 or 2, wherein each delay memory element includes an internal feed back loop to renew the stored signal in response to succeeding clock pulses in accordance with the state of the output of the element.

4. A ring counter as claimed in any preceding claim, wherein the logical gate circuit operates such that said first state is the state corresponding to the presence of a signal stored in said internal capacitance and said second state is the state corresponding to absence of a signal stored in said gate internal capacitance.

5. A ring counter as claimed in claim 4, wherein the logical gate circuit comprises a plurality of mono-directional conductive elements which each have one end connected to the output of a respective one of said memory elements except for the n^{th} delay element, the other ends of said mono-directional conductive elements being connected together to make up a logical circuit for "OR" gating, the output thereof being fed back to the input of the first of said memory elements through an element to provide a "NOT" function.

6. A ring counter as claimed in any preceding claim, wherein the logical gate circuit operates such that said first state is the state corresponding to absence of a signal stored in said internal capacitance and said second state is the state corresponding to the presence of a signal stored in said internal capacitance.

8. A ring counter as claimed in claim 7, wherein the logical gate circuit comprises a plurality of mono-directional conductive elements which each have one end connected to the output of a respective one of said memory elements except for the n^{th} delay element, the other end of said mono-directional conductive elements being connected together to make up a logical circuit for "AND" gating, the output thereof being fed back to the

input of the first of the memory elements through an element to provide a "NOT" function.

- 5 9. A ring counter as claimed in claim 5, wherein the logical gate circuit comprises a pair of mono-directional conductive elements which each have one end connected to the output of a respective one of said $n-1^{\text{th}}$ and n^{th} memory elements, the other end of one
10 said mono-directional conductive elements being connected to that of the other of said mono-directional conductive elements through a third element providing a "NOT" function, to make up a logical circuit for "AND" gat-
15 ing; and wherein a switch is connected to the input of the first of the memory elements for provision of an initial condition in which the outputs of all the memory elements are in said first state.
- 20 10. A ring counter as claimed in claim 7, wherein the logical gate circuit comprises a pair of mono-directional conductive elements which each have one end connected to the output of a
25 respective one of said $n-1^{\text{th}}$ and n^{th} memory

elements, the other end of one of said mono-directional conductive elements being connected to that of the other mono-directional conductive element through a third element providing a NOT function, to make up a
30 logical circuit for "OR" gating; and wherein a switch is connected to the input of the first of the memory elements for provision of an initial condition in which the outputs of all the memory elements are in said first state. 35

11. A ring counter substantially as described herein with reference to the accompanying drawings.

12. The combination of a ring counter according to any preceding claim and means
40 for generating clock pulses having a spacing less than said predetermined time whereby said counter operates without loss of said signal.

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