

**A SYSTEM LEVEL MECHANISM FOR INVALIDATING DATA STORED IN THE
EXTERNAL CACHE OF A PROCESSOR IN A COMPUTER SYSTEM**

ABSTRACT

A computer system is disclosed including a memory subsystem and a processor subsystem having an external cache and an external mechanism for
5 invalidating cached datablocks in the processor subsystem and for reducing false
invalidation operations . The processor subsystem issues a write invalidate
message to the memory subsystem that specifies a datablock and that includes
an invalidate advisory indication that indicates whether the datablock is present
in the external cache. The invalidate advisory indication determines whether
10 the memory subsystem returns an invalidate message to the processor
subsystem for the write invalidate operation.

(Figure 1)