FIG. 1

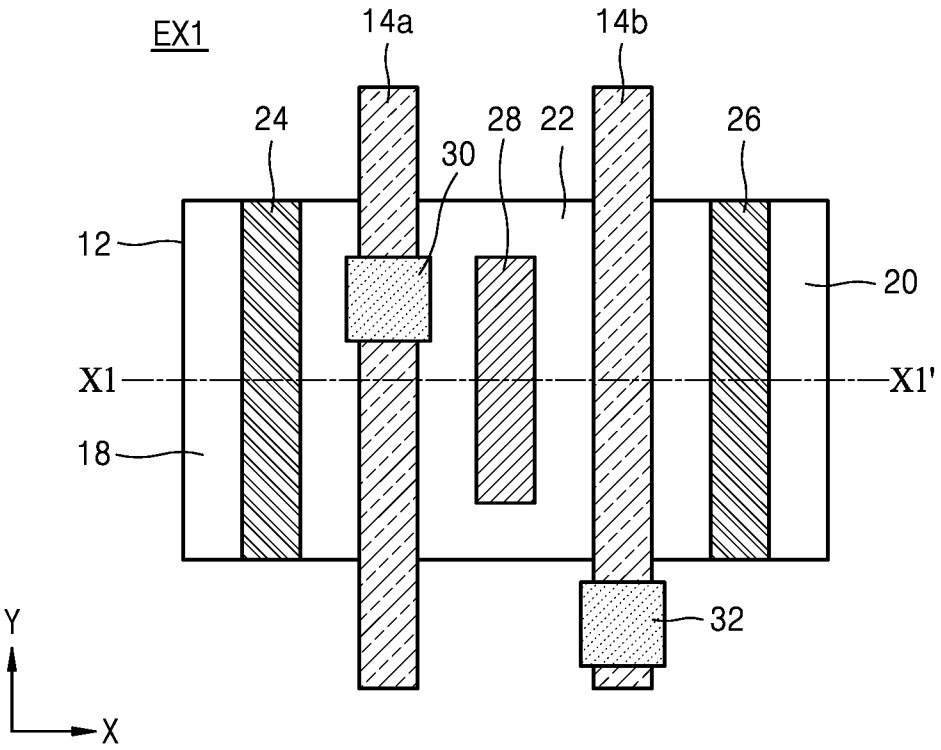


FIG. 2

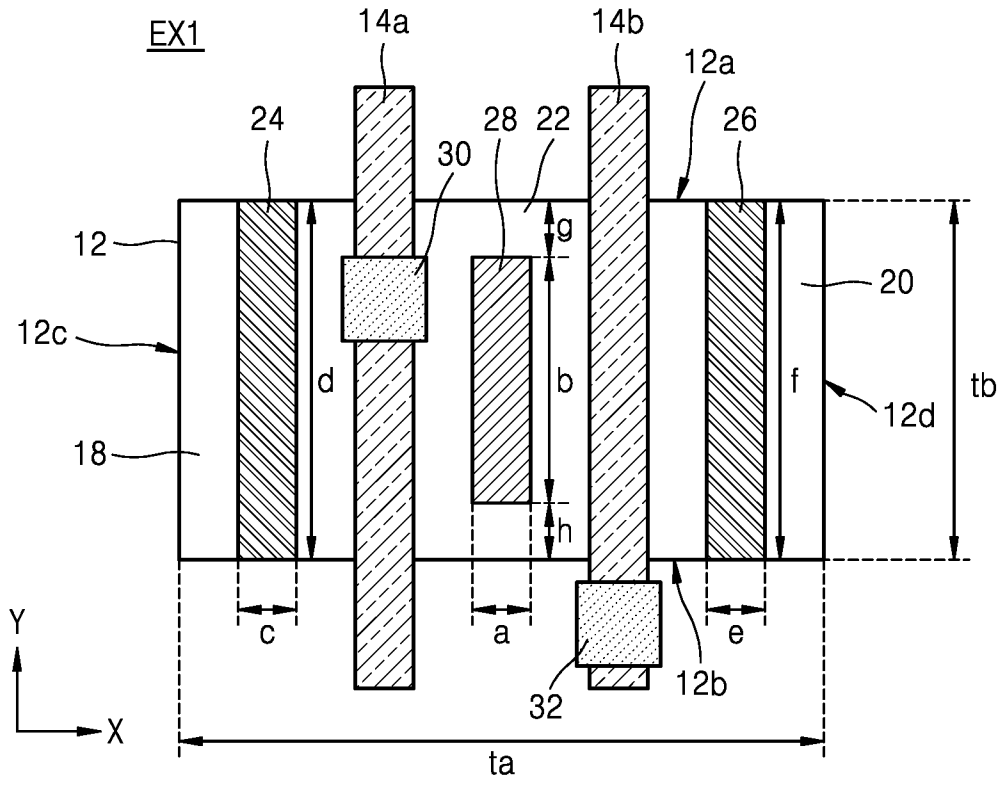

EX1
14a
14b
12a
24
28
22
26
30
12
g
20
12c
d
b
f
tb
12d
18
h
c
a
e
12b
32
Y
X
ta

FIG. 3

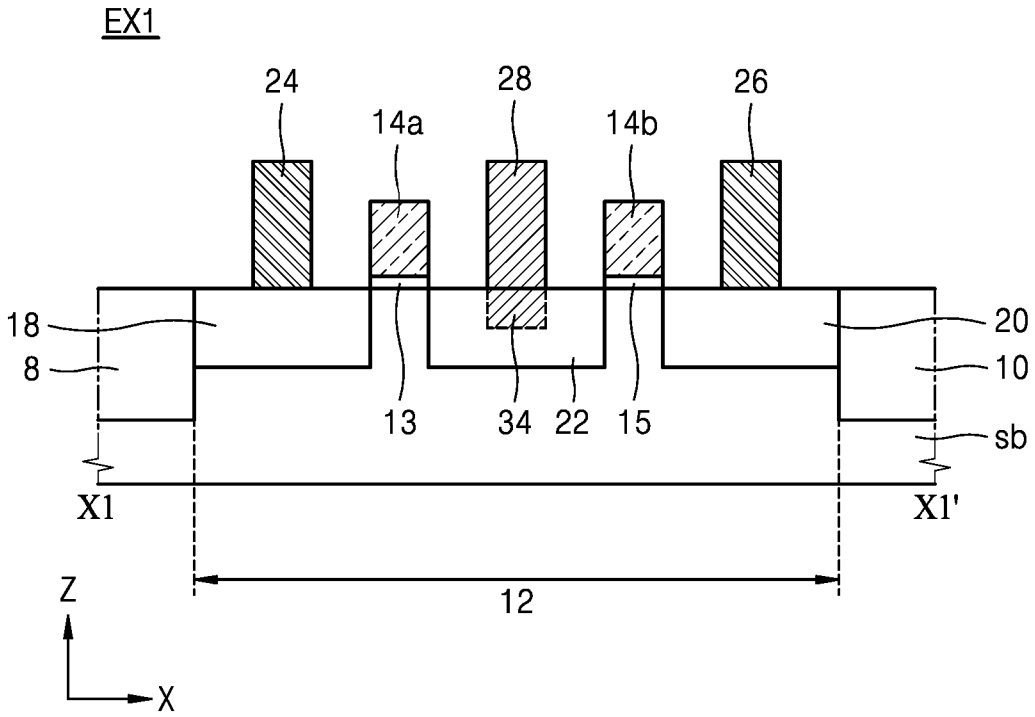


FIG. 4

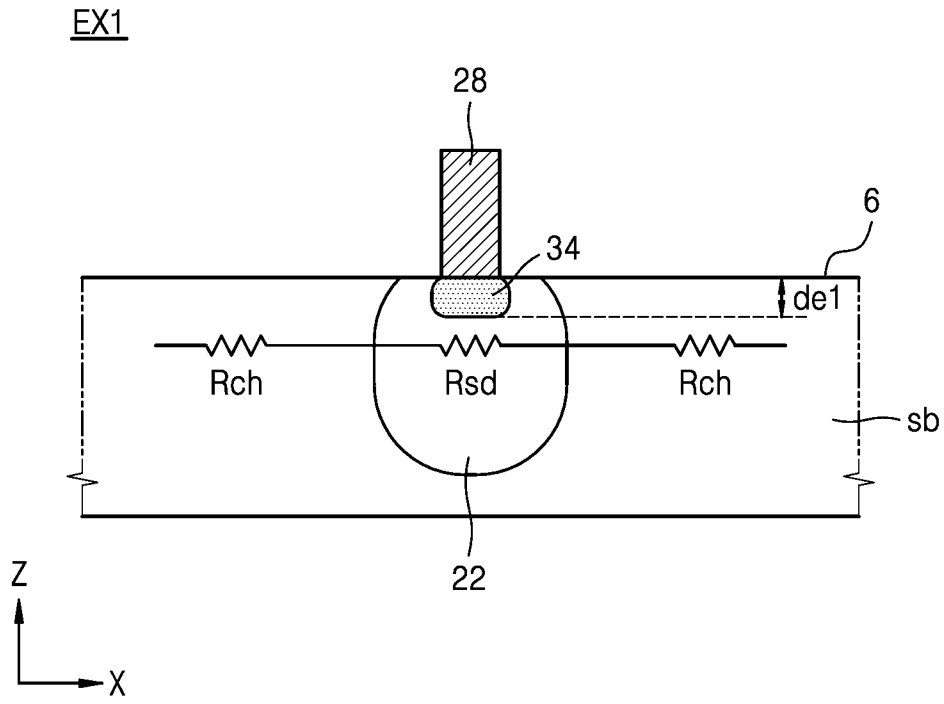


FIG. 5

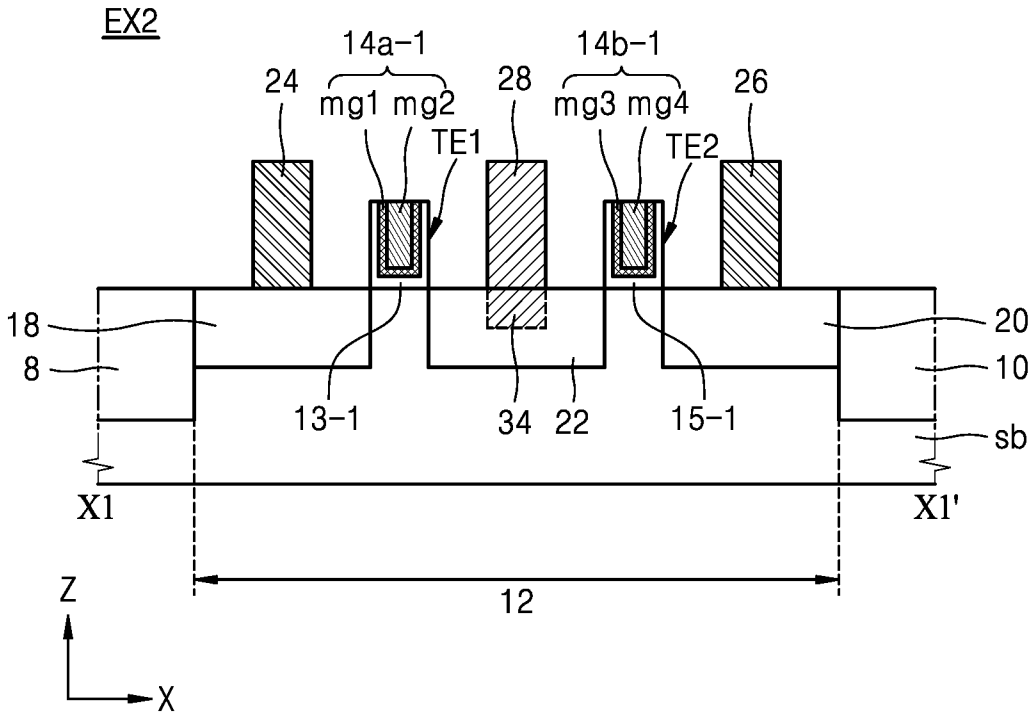

EX2
14a-1
14b-1
24
mg1 mg2
28
mg3 mg4
26
TE1
TE2
18
8
20
10
13-1
34
22
15-1
sb
X1
X1'
12
Z
X

FIG. 6

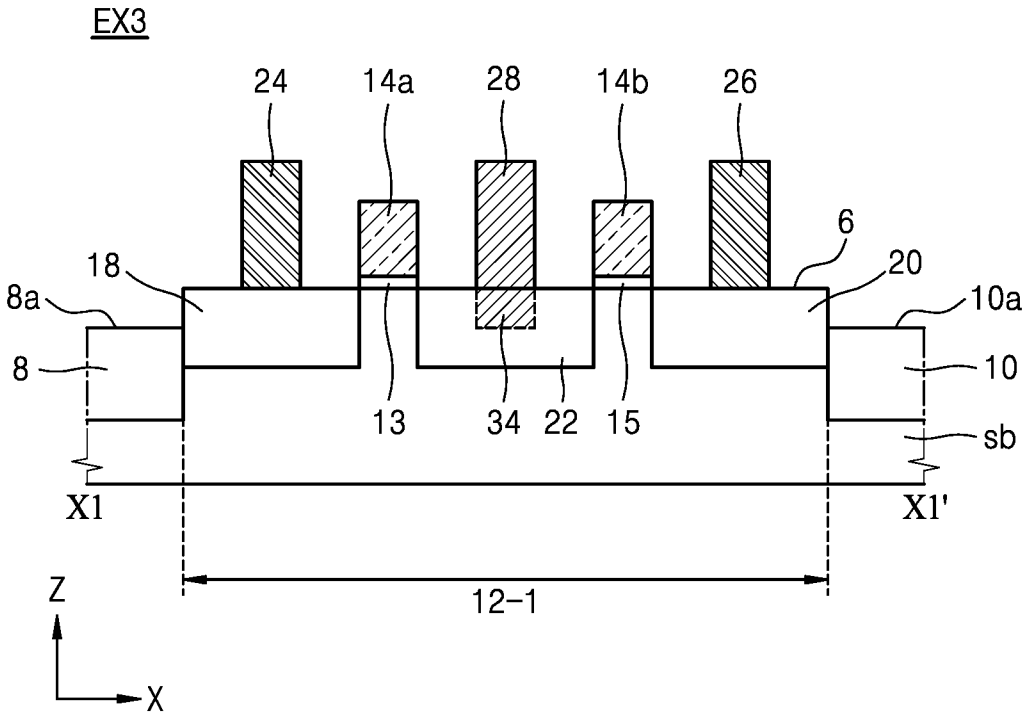


FIG. 7

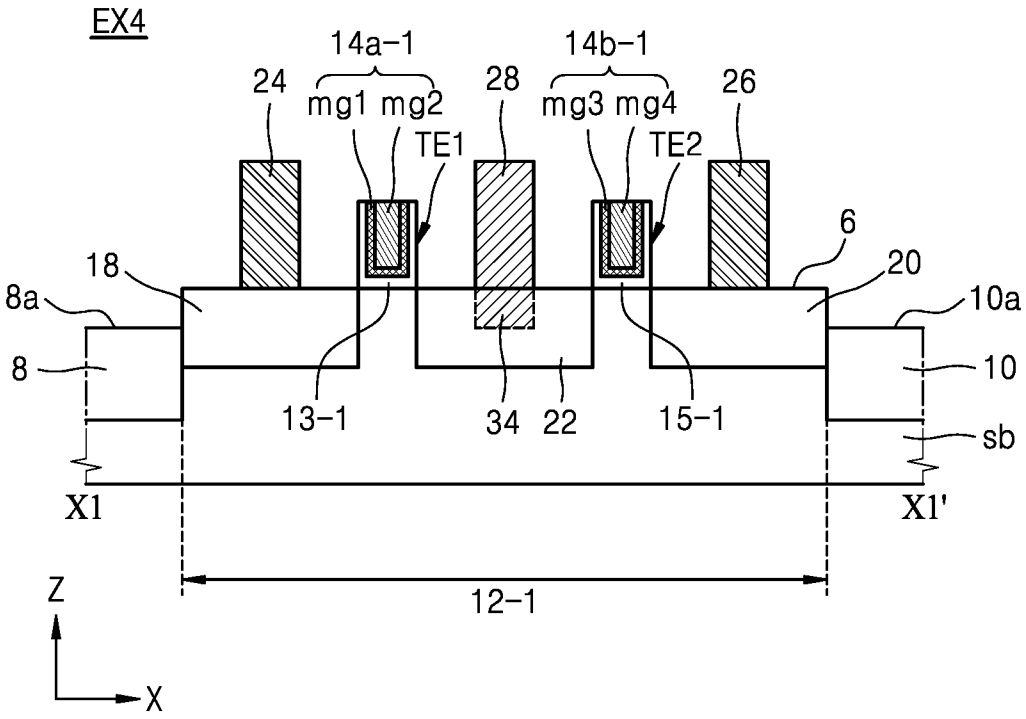

EX4
14a-1
14b-1
24
mg1 mg2
28
mg3 mg4
26
TE1
TE2
6
18
20
8a
10a
8
10
13-1
34
22
15-1
sb
X1
X1'
12-1
Z
X

FIG. 8

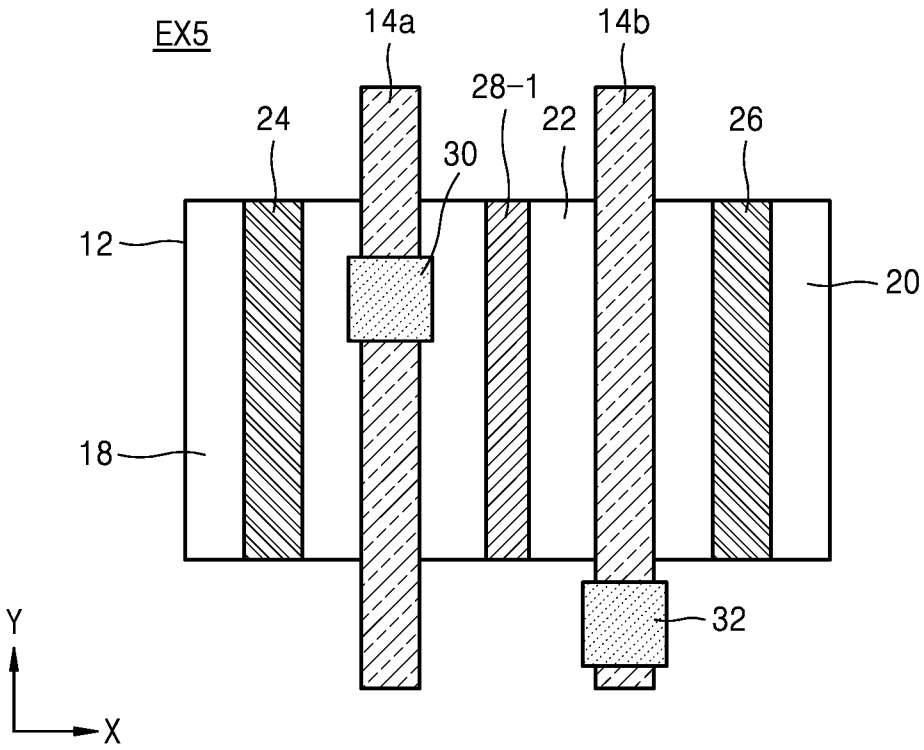


FIG. 9

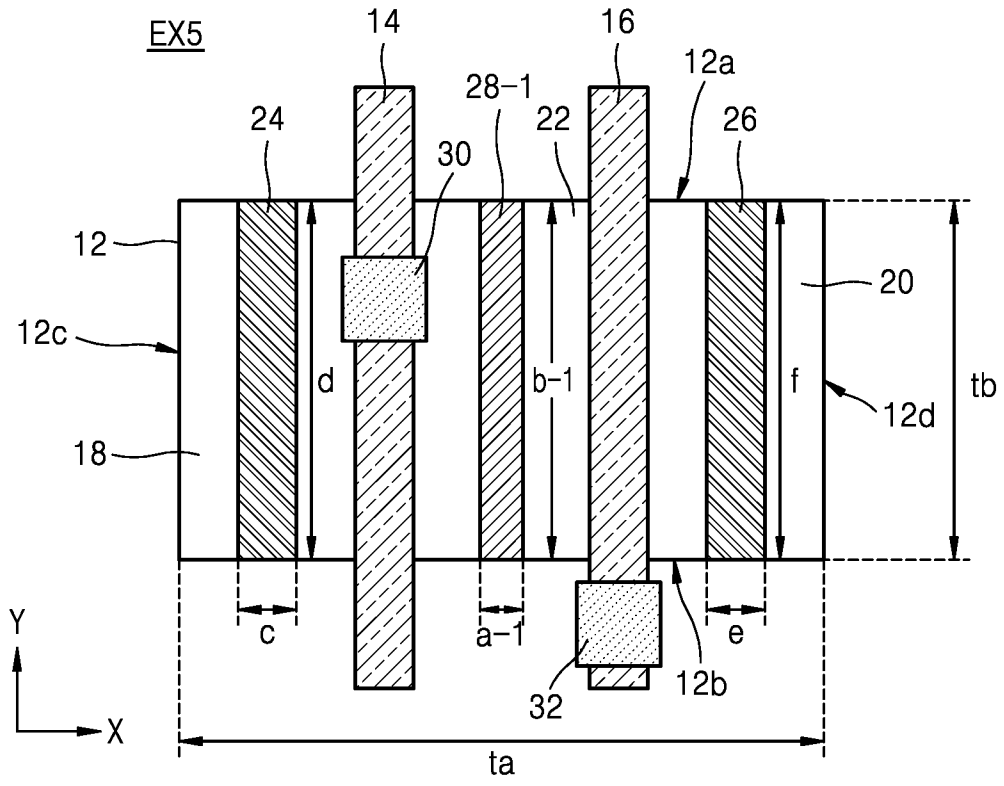

EX5
14
16
12a
28-1
24
22
26
30
12
20
12c
d
b-1
f
tb
12d
18
c
a-1
e
12b
32
Y
X
ta

FIG. 10

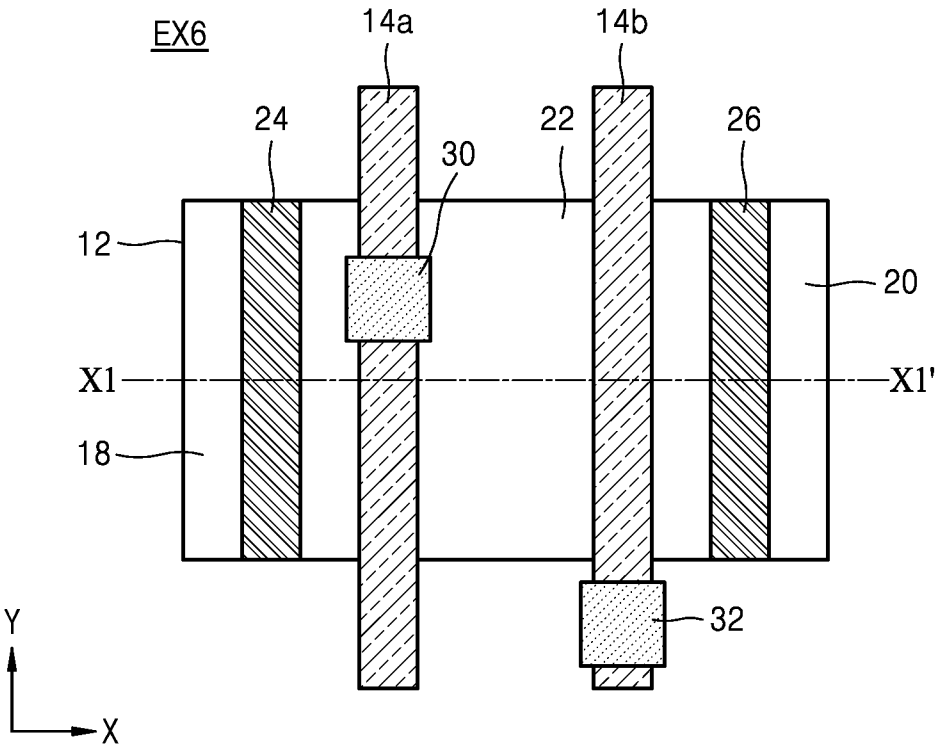


FIG. 11

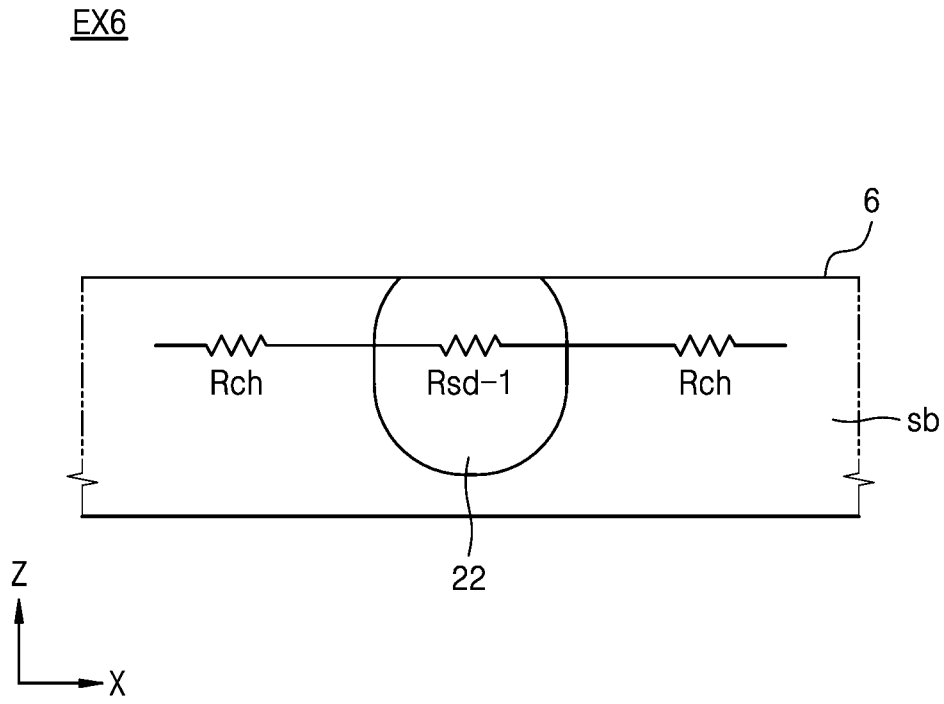


FIG. 12

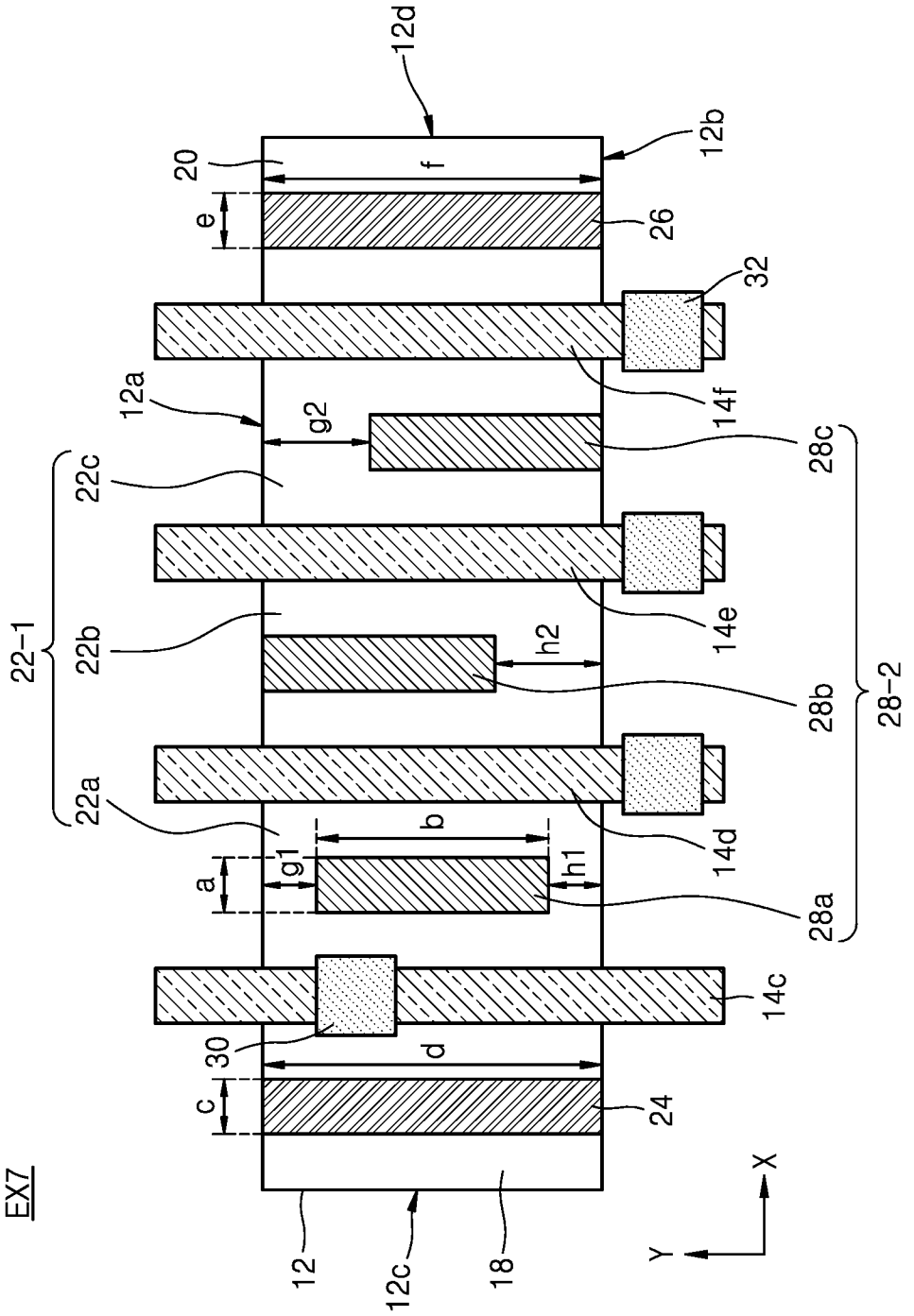

EX7
12d
12b
20
f
e
26
32
12a
g2
14f
28c
22c
22-1
22b
h2
14e
28b
28-2
22a
b
14d
g1
h1
a
28a
14c
30
d
c
24
12
12c
18
Y
X

FIG. 13

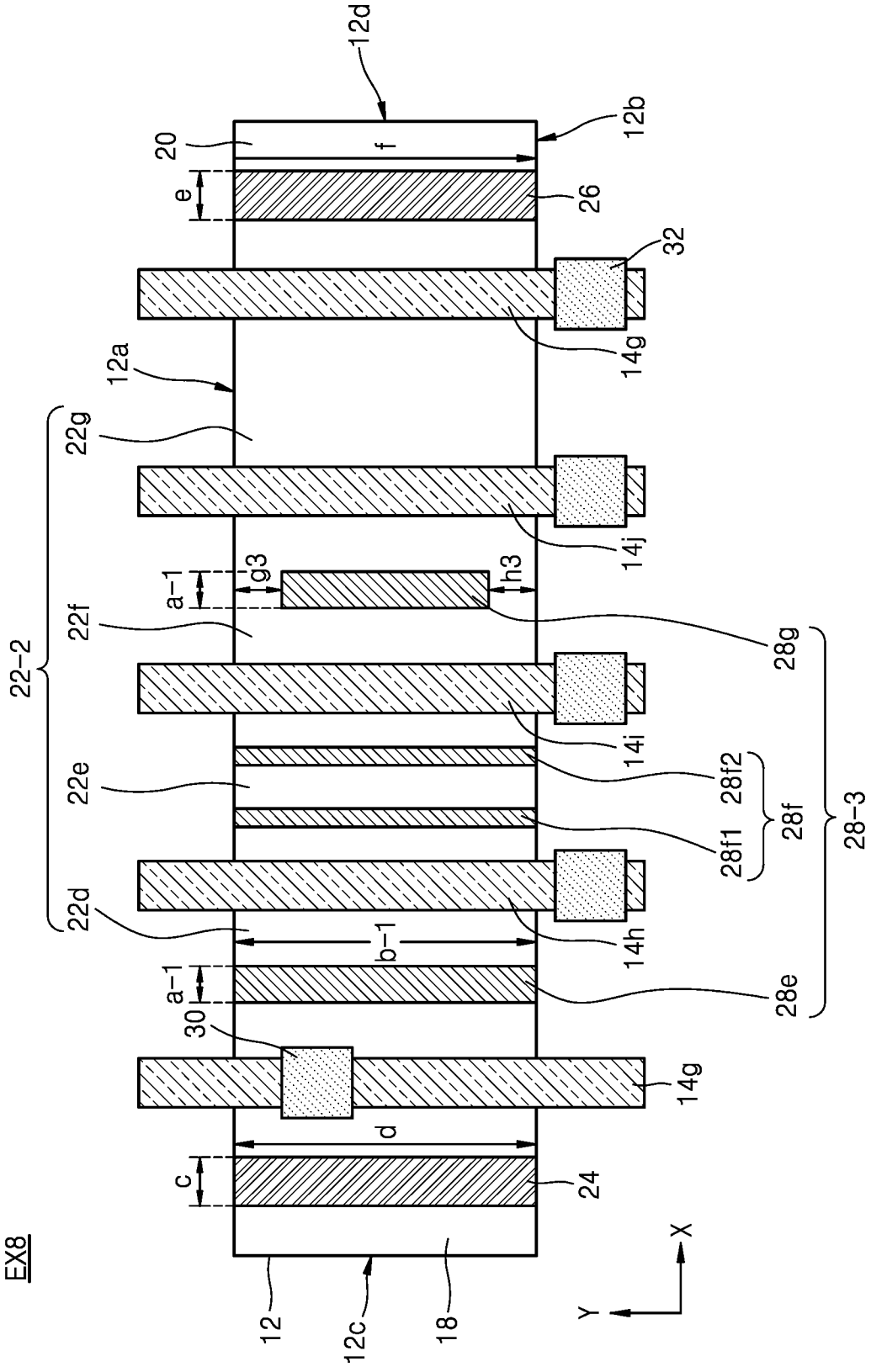

EX8
12d
12b
20
f
e
26
32
14g
12a
22g
14j
a-1
g3
h3
22f
28g
22-2
14i
28f2
22e
28f1
28f
28-3
22d
14h
b-1
a-1
28e
30
14g
d
c
24
12
12c
18
Y
X

FIG. 14

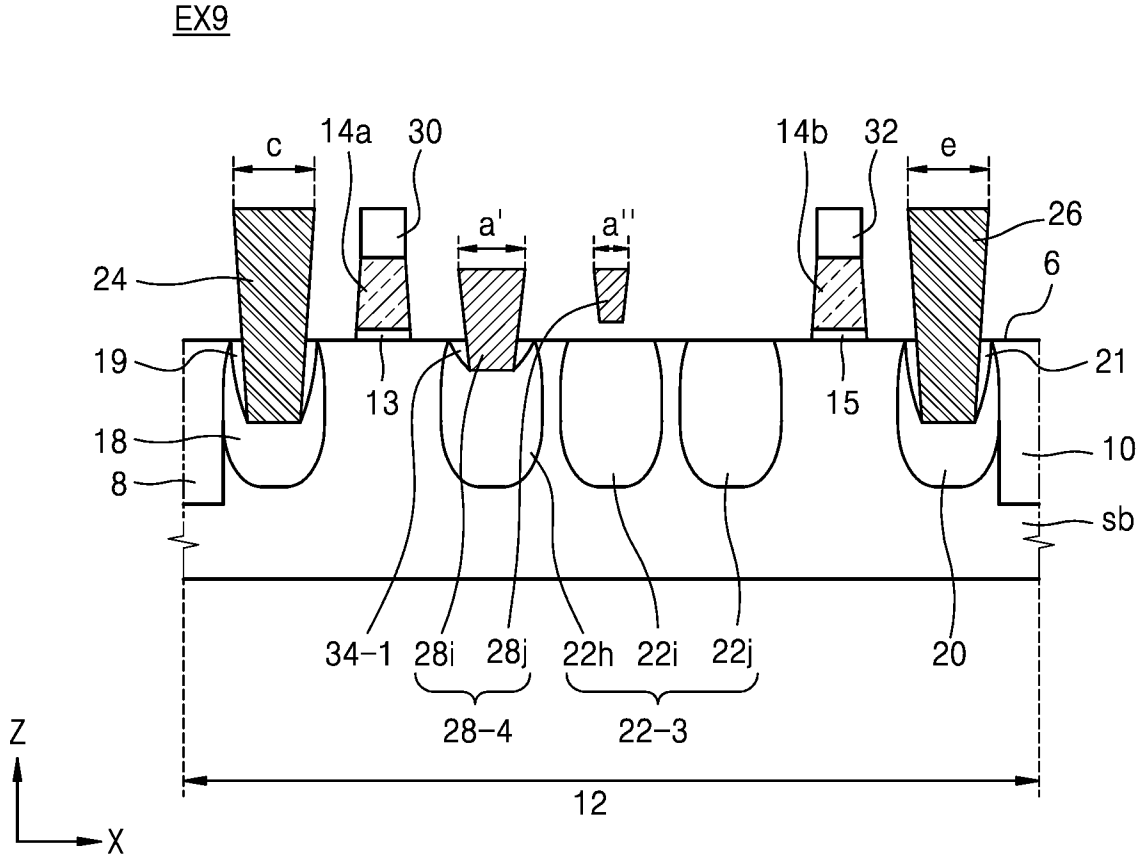

EX9
c
14a
30
14b
32
e
a'
a''
26
24
6
19
21
13
15
18
10
8
sb
34-1
28i
28j
22h
22i
22j
20
28-4
22-3
12
Z
X

FIG. 15

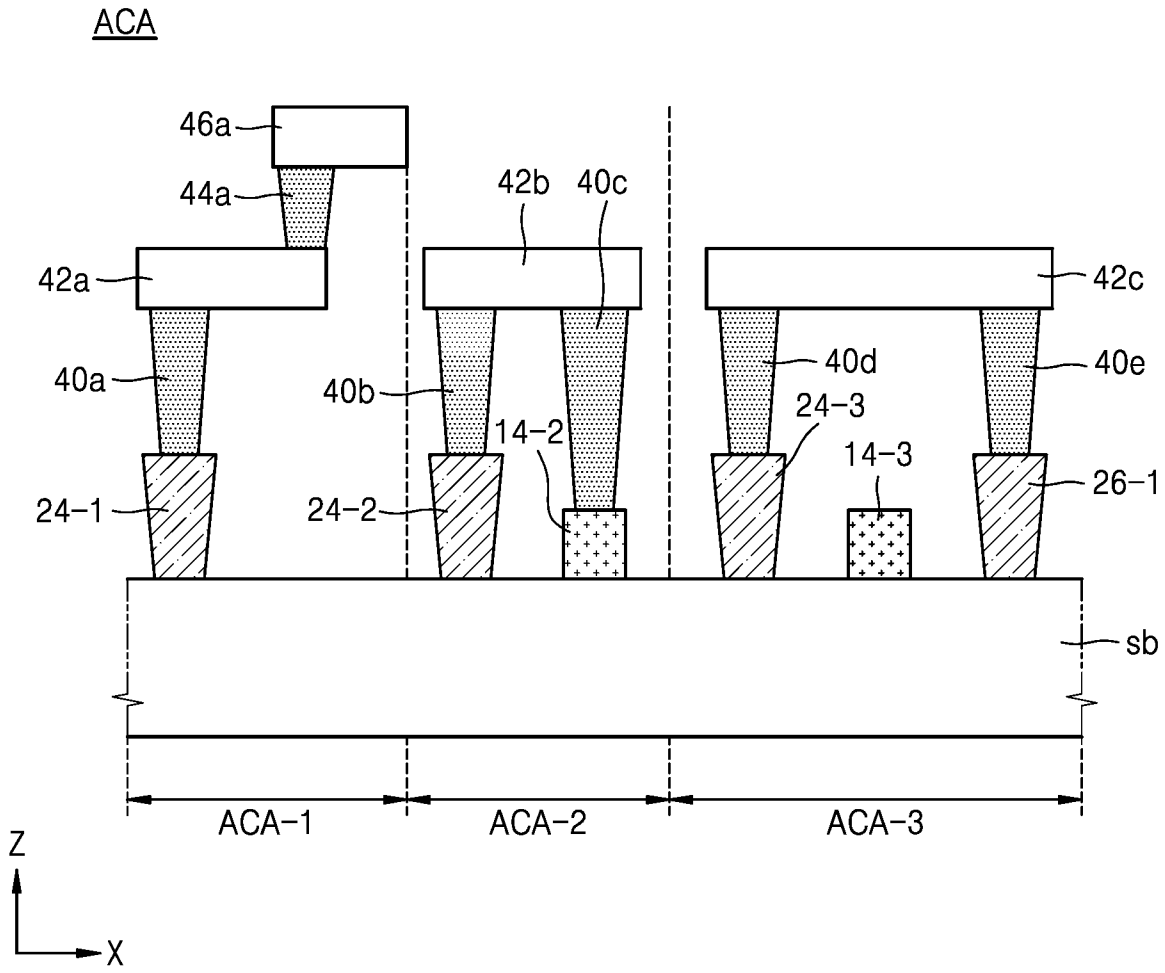

ACA
46a
44a
42a
40a
24-1
42b
40c
40b
24-2
14-2
42c
40d
24-3
14-3
40e
26-1
sb
ACA-1
ACA-2
ACA-3
Z
X

FIG. 16

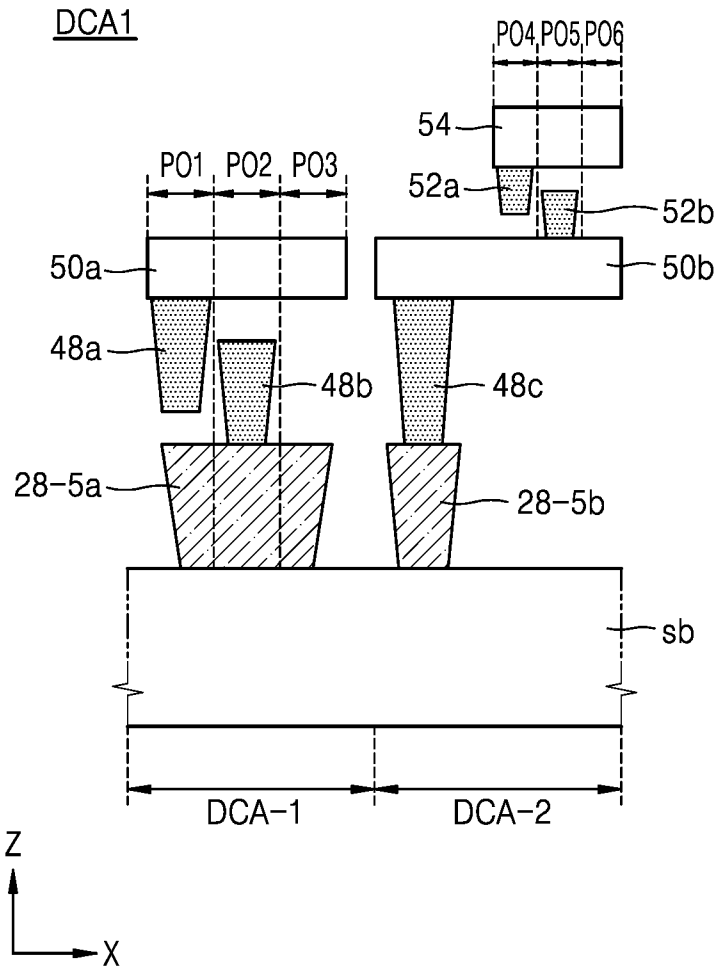

DCA1
P04 P05 P06
54
P01 P02 P03
52a
52b
50a
50b
48a
48b
48c
28-5a
28-5b
sb
DCA-1
DCA-2
Z
X

FIG. 17

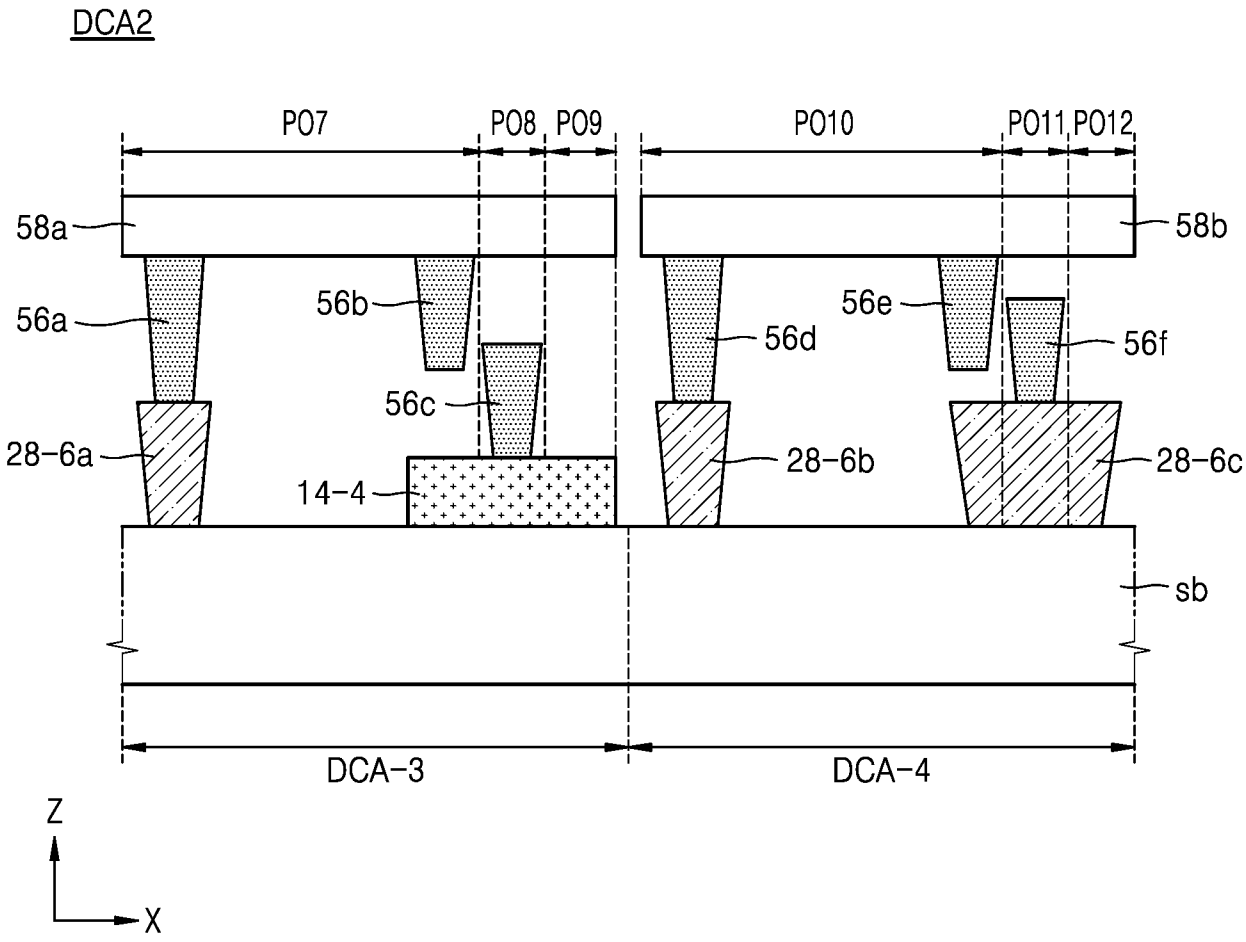
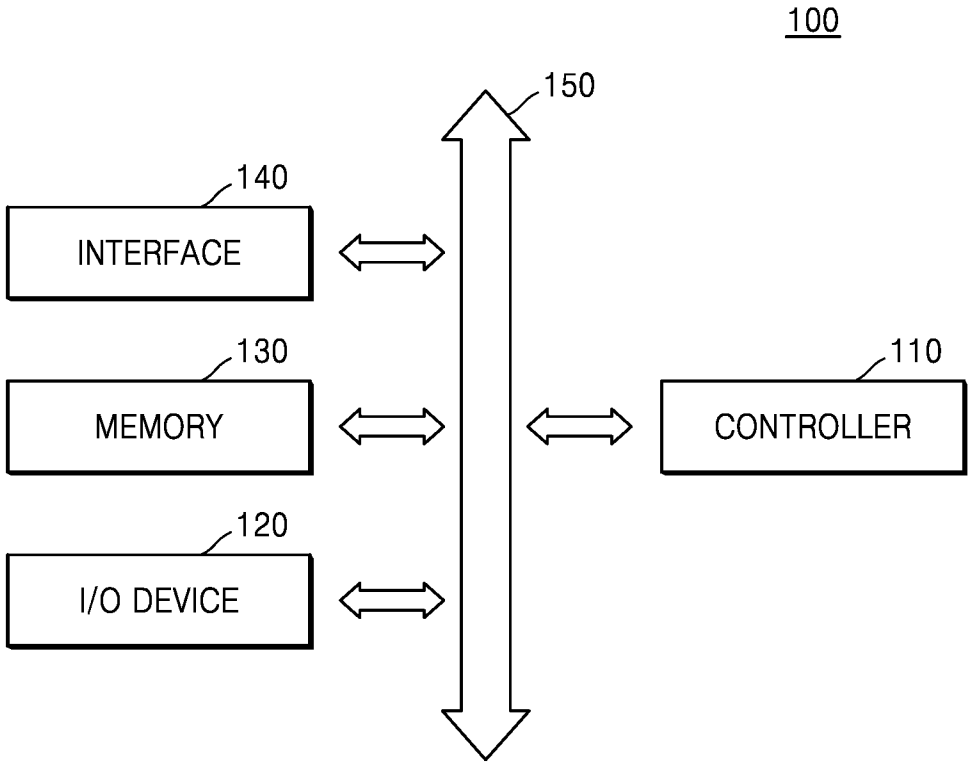

DCA2
P07
P08
P09
P010
P011
P012
58a
58b
56a
56b
56c
56d
56e
56f
28-6a
28-6b
28-6c
14-4
sb
DCA-3
DCA-4
Z
X

FIG. 18


100
150
140
INTERFACE
130
MEMORY
120
I/O DEVICE
110
CONTROLLER