

FIG. 1

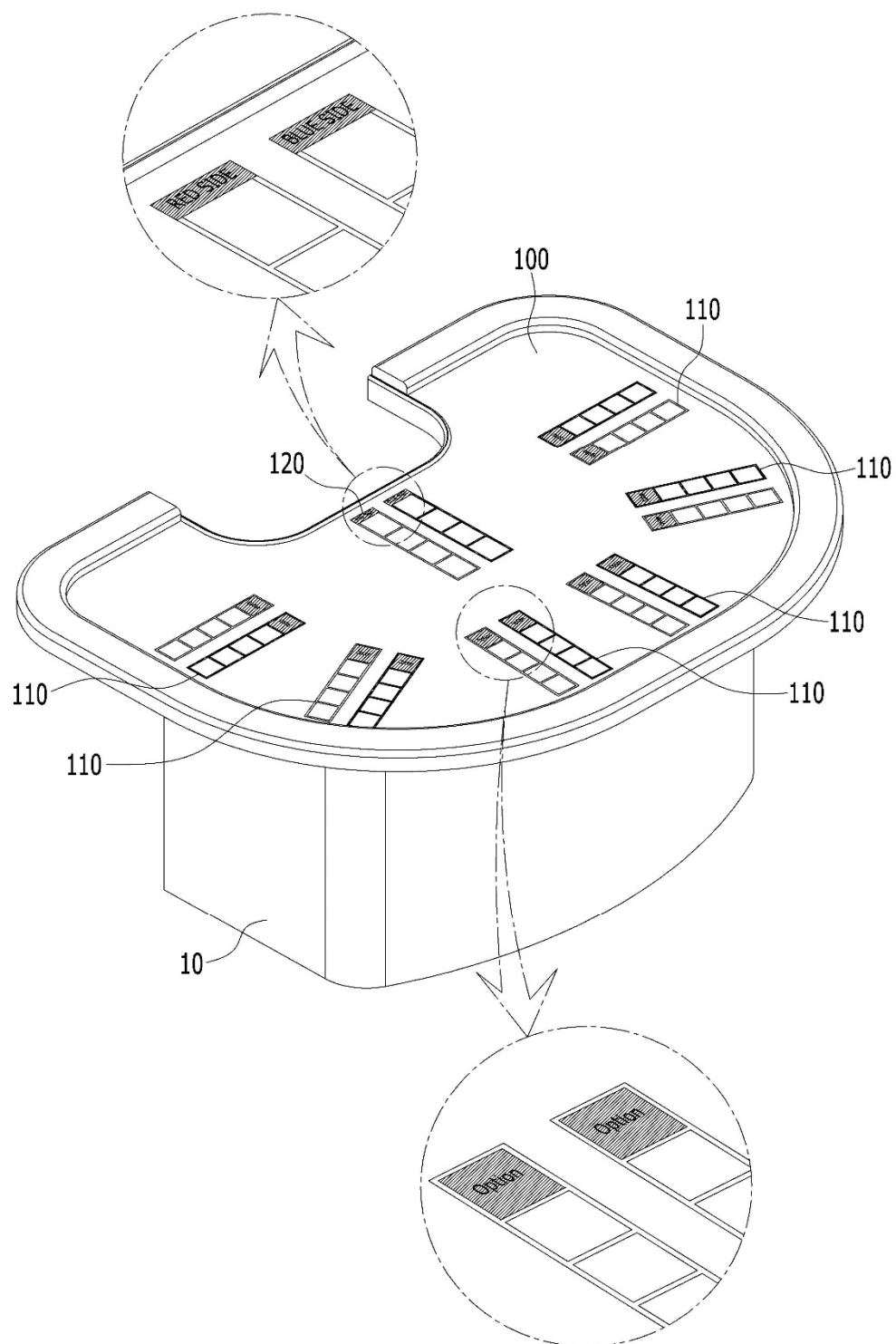


FIG. 2

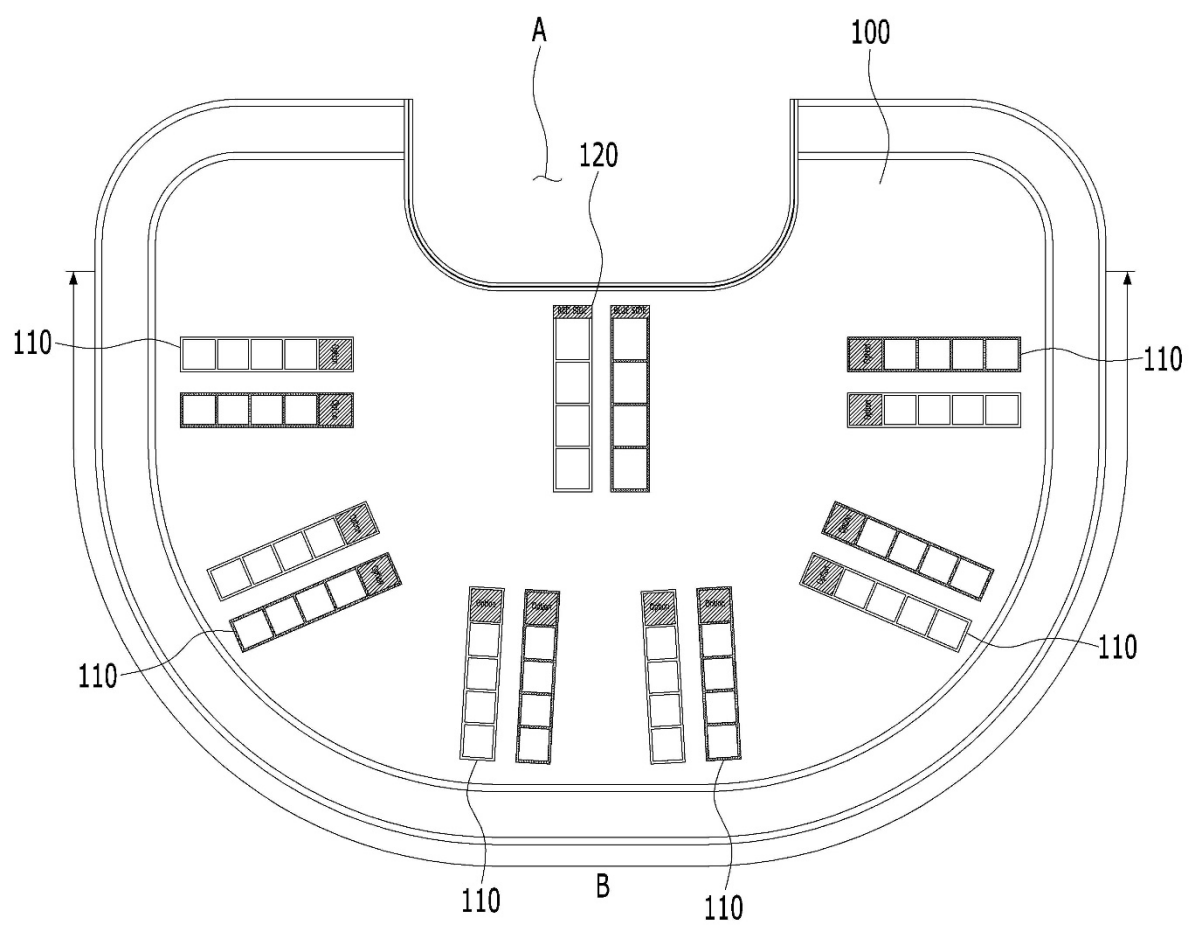


Figure 1 illustrates a semiconductor device in three states: P1, P2, and P5. The device consists of a stack of layers. In state P1, the stack includes layers 110a, 110b, and 300a. In state P2, the stack includes layers 110a, 110b, and 300b. In state P5, the stack includes layers 110a, 110b, and 300c. The diagrams show the relative positions and thicknesses of these layers, as well as the state of the device during different phases of operation.

FIG. 3B

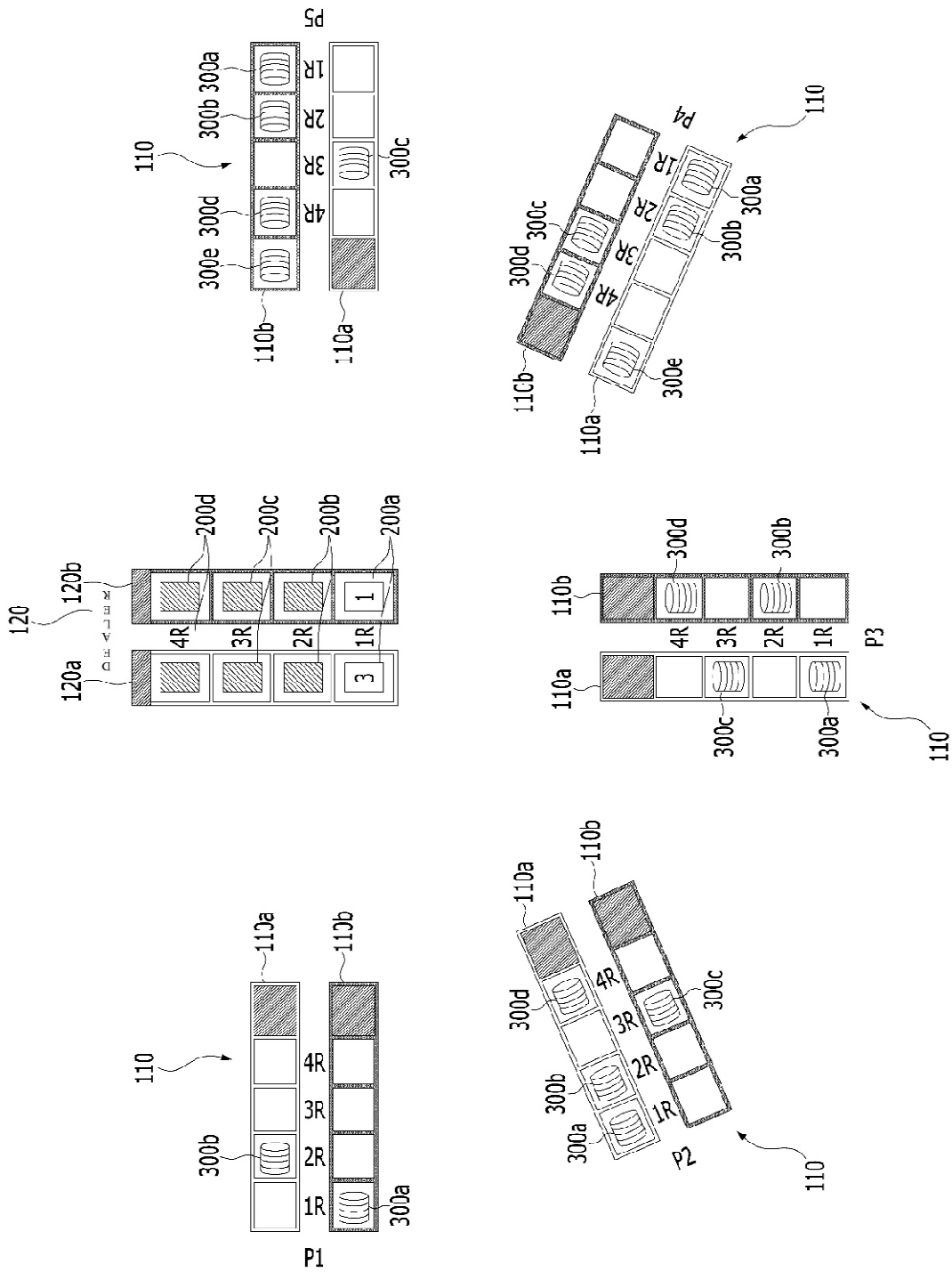


FIG. 3C

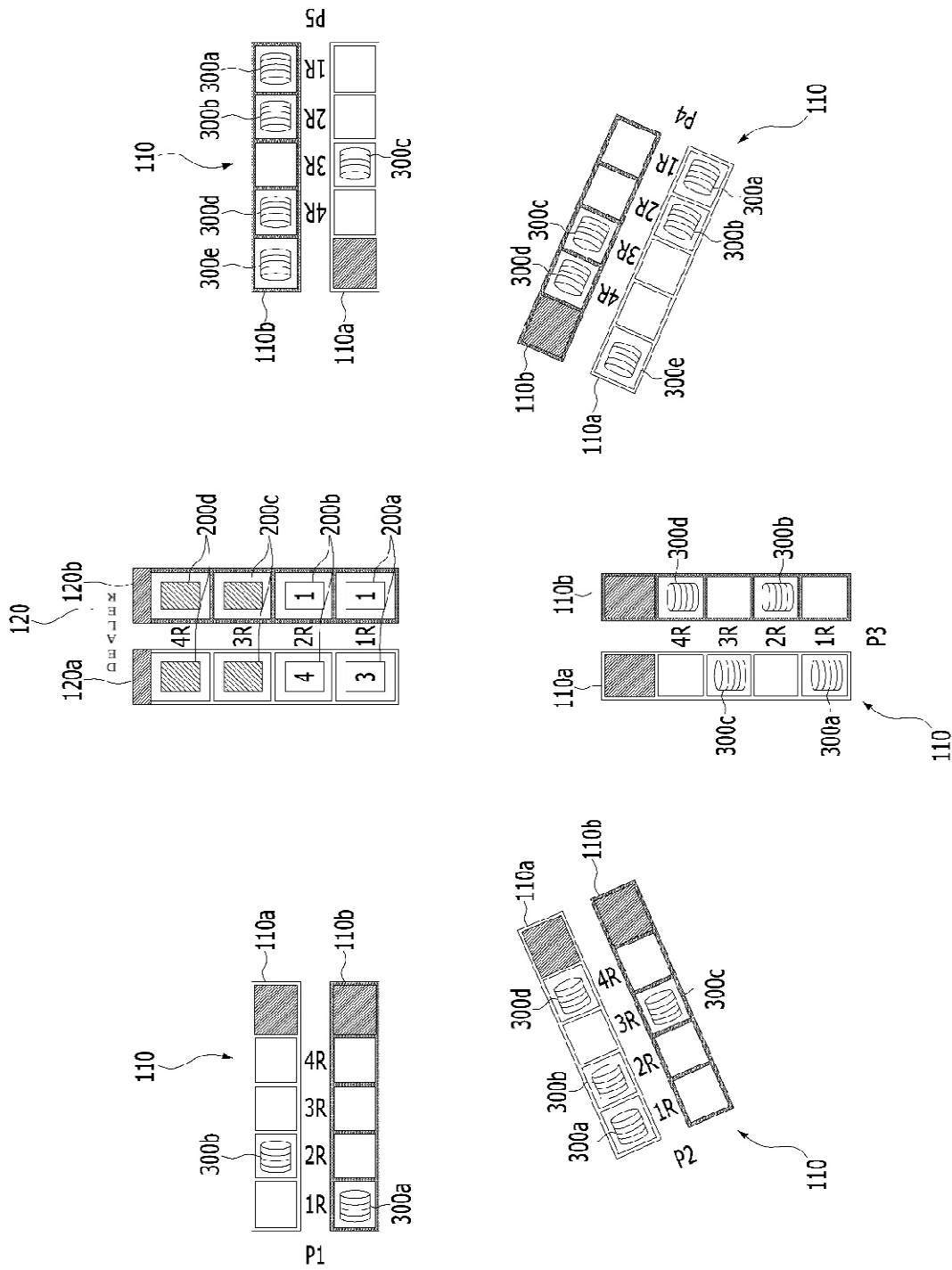


FIG. 3D

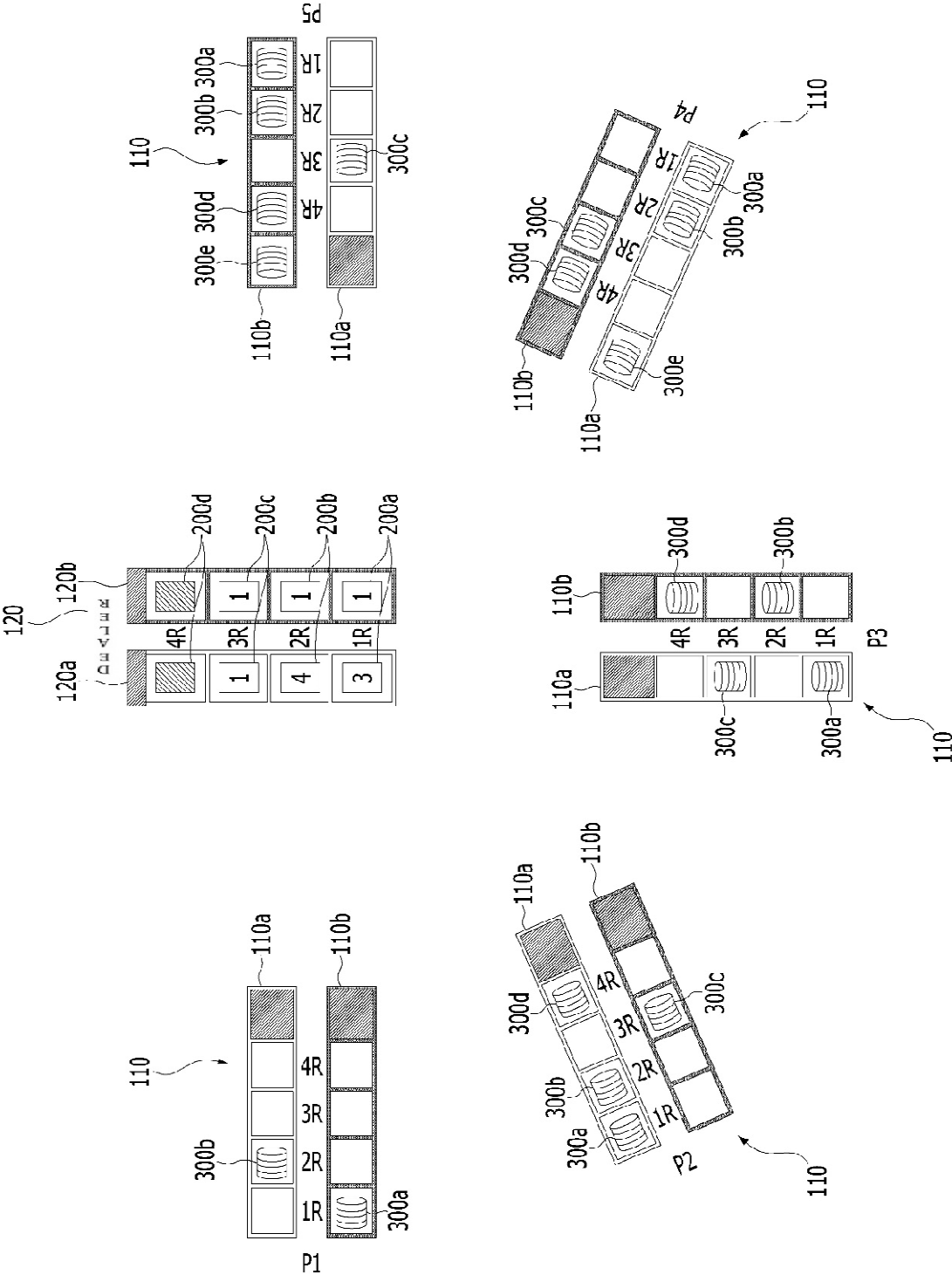


FIG. 3E

