

1/283

FIG. 1

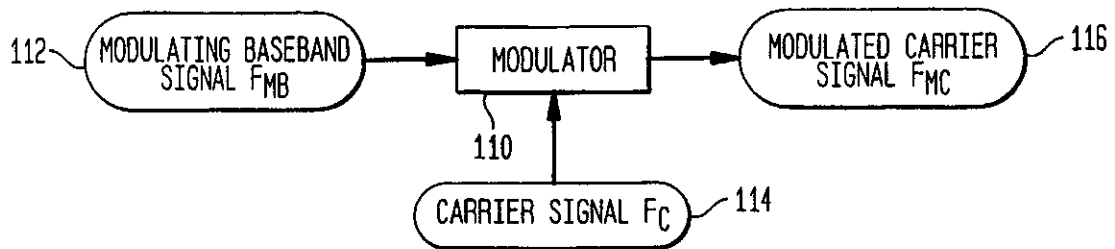


FIG. 2

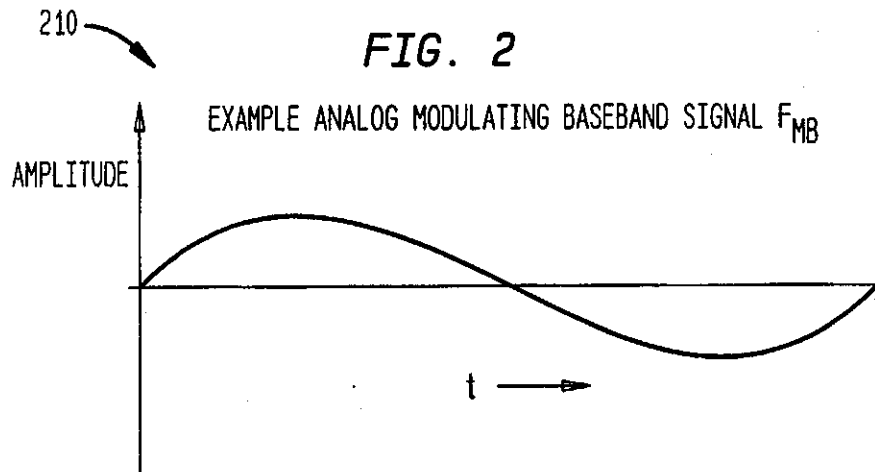


FIG. 3

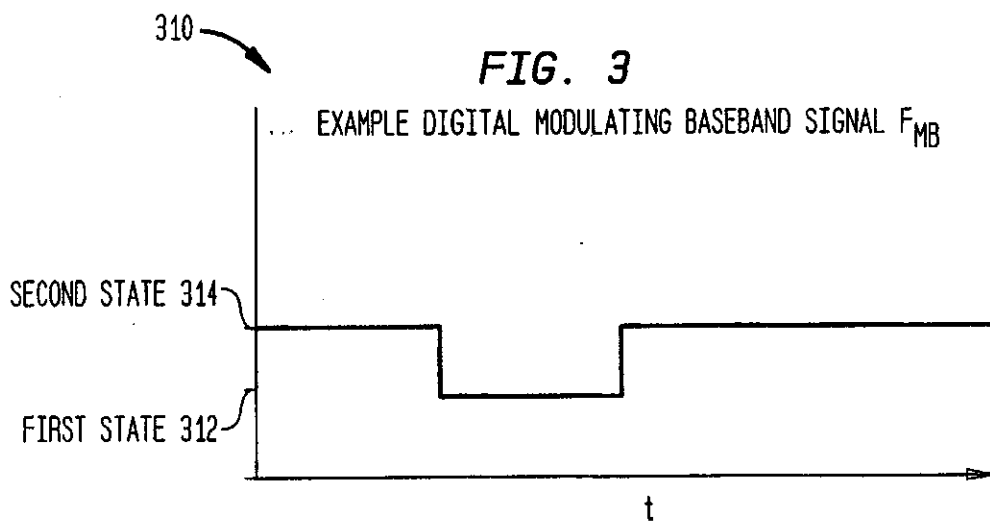
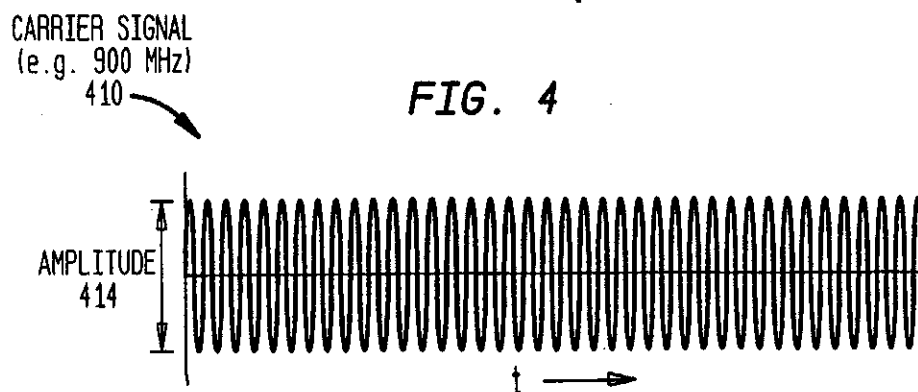


FIG. 4



2/283

ANALOG
BASEBAND SIGNAL
210

FIG. 5A

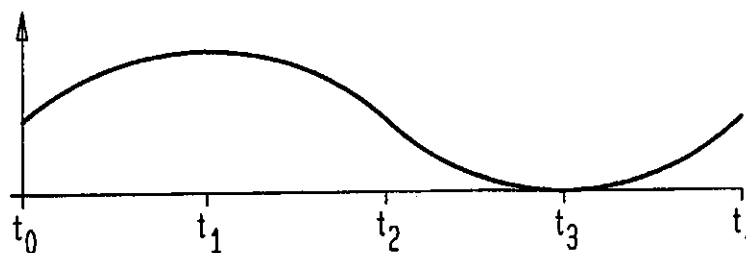
CARRIER SIGNAL
410

FIG. 5B

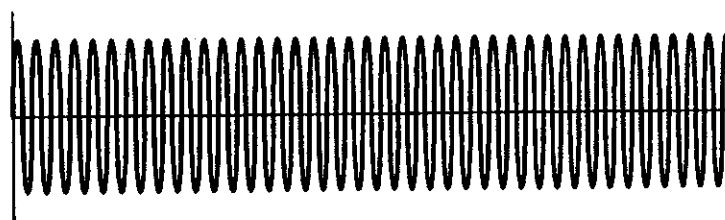
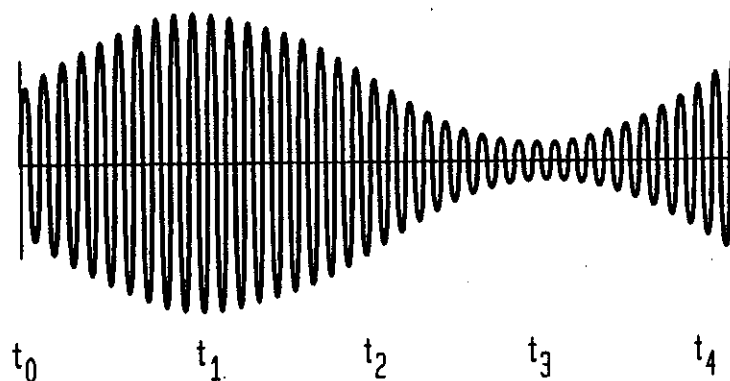
AM CARRIER
SIGNAL
516

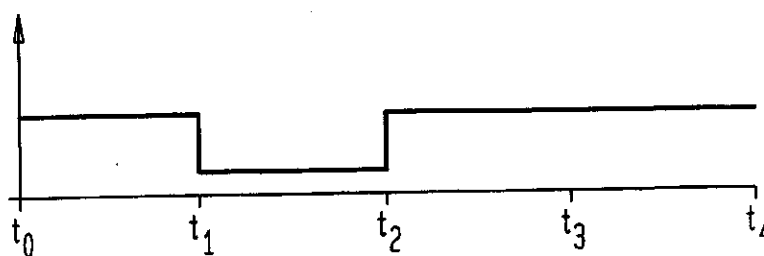
FIG. 5C



3/283

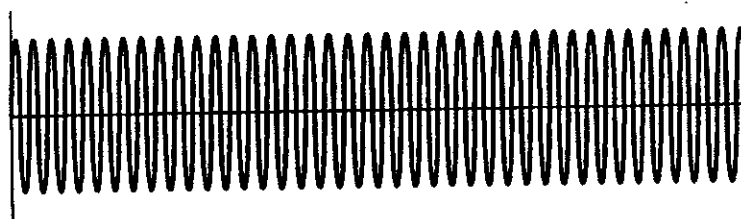
DIGITAL
BASEBAND SIGNAL
310

FIG. 6A



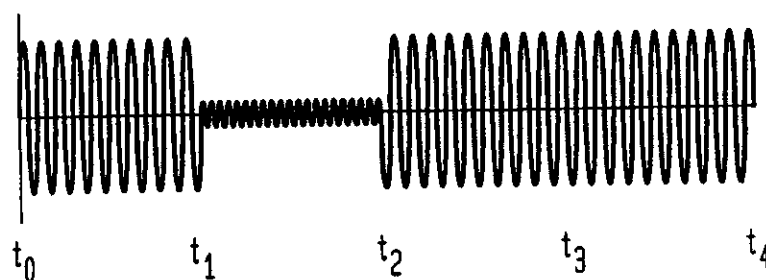
CARRIER SIGNAL
410

FIG. 6B



AM CARRIER SIGNAL
616

FIG. 6C



4/283

ANALOG
BASEBAND SIGNAL
210

FIG. 7A

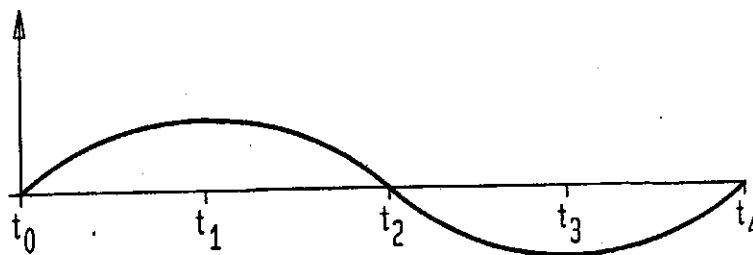
CARRIER SIGNAL
410

FIG. 7B

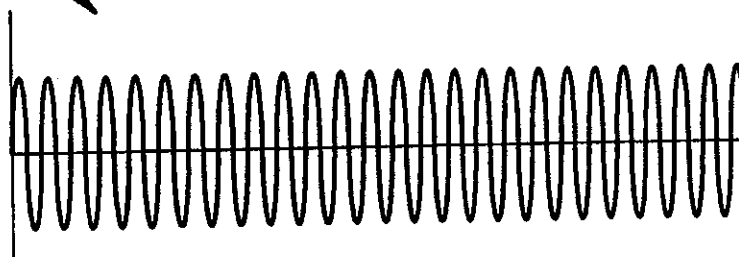
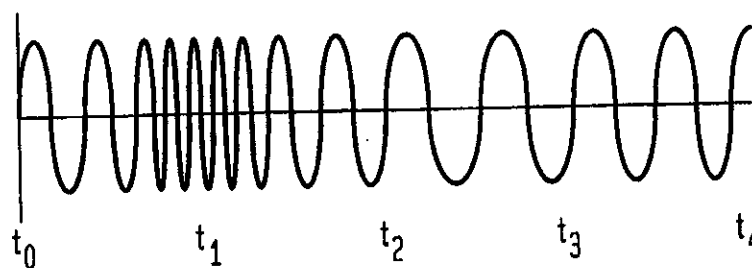
FM CARRIER SIGNAL
716

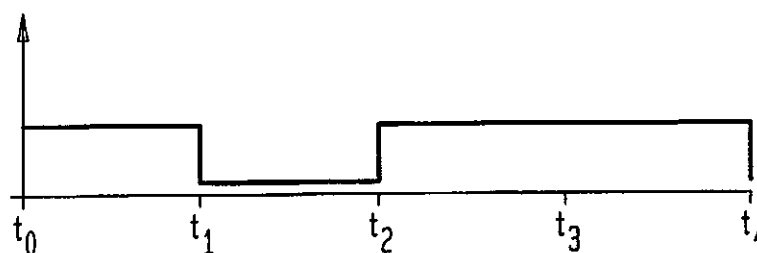
FIG. 7C



5/283

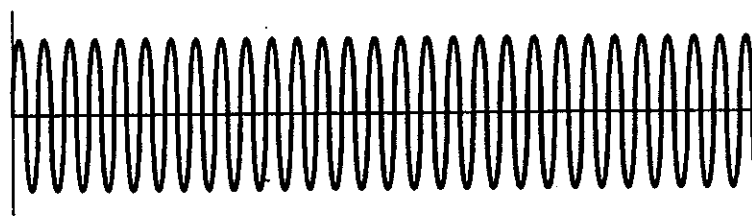
DIGITAL
BASEBAND SIGNAL
310

FIG. 8A



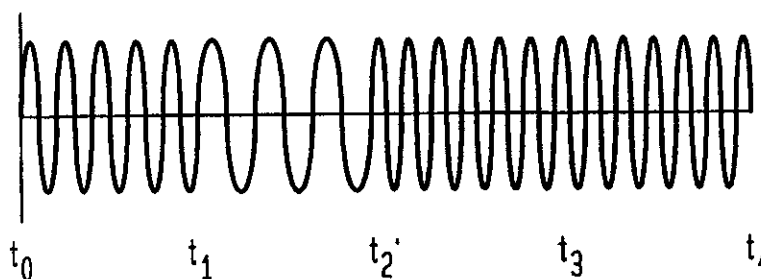
CARRIER SIGNAL
410

FIG. 8B



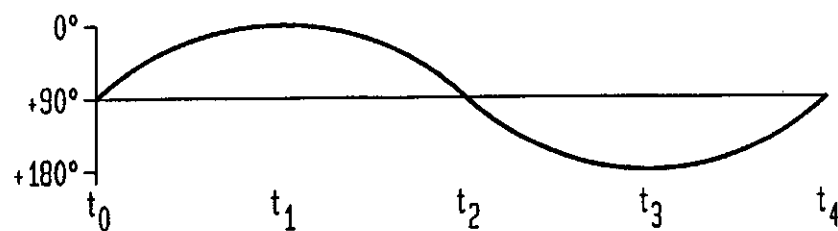
FM CARRIER SIGNAL
816

FIG. 8C

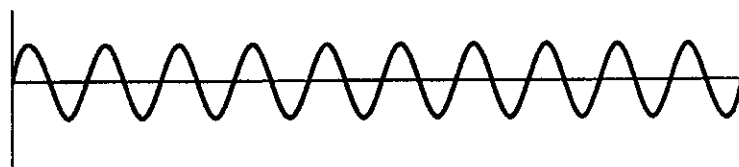


6/283

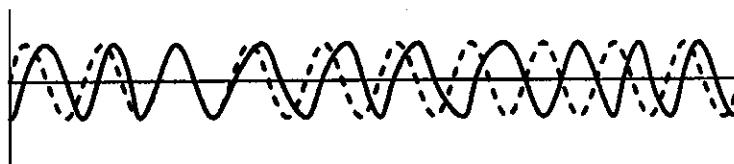
ANALOG
BASEBAND SIGNAL
210

FIG. 9A

CARRIER SIGNAL
410

FIG. 9B

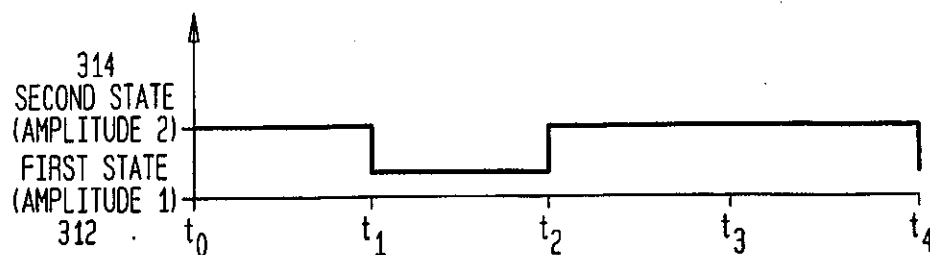
PHASE MODULATED
CARRIER SIGNAL
916

FIG. 9C

7/283

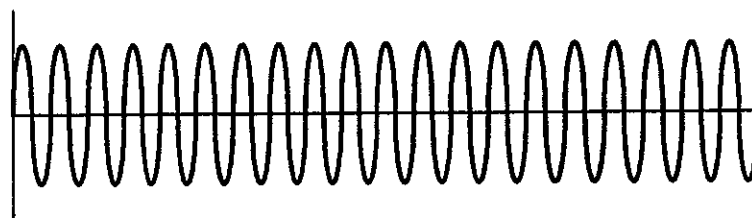
DIGITAL
BASEBAND SIGNAL
310

FIG. 10A



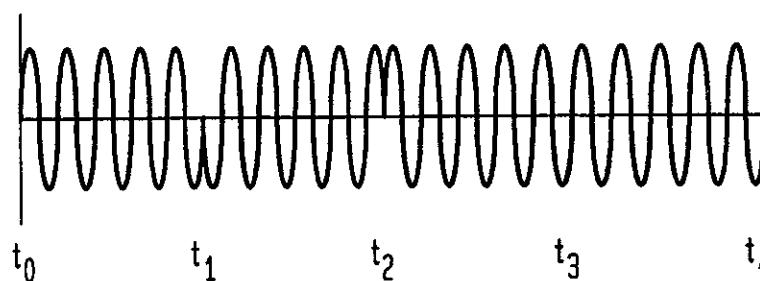
CARRIER SIGNAL
410

FIG. 10B



PHASE MODULATED
CARRIER SIGNAL
1016

FIG. 10C



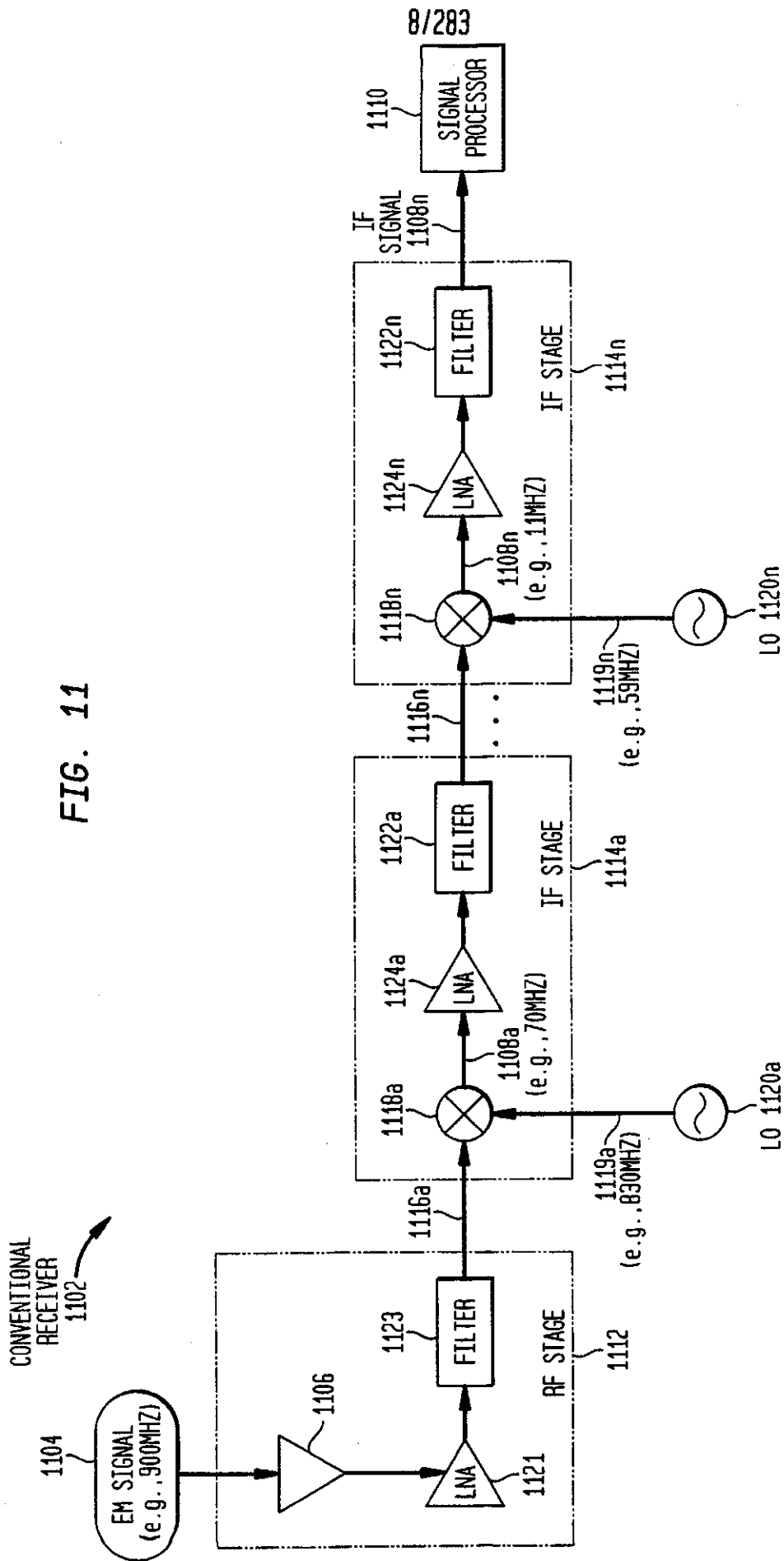
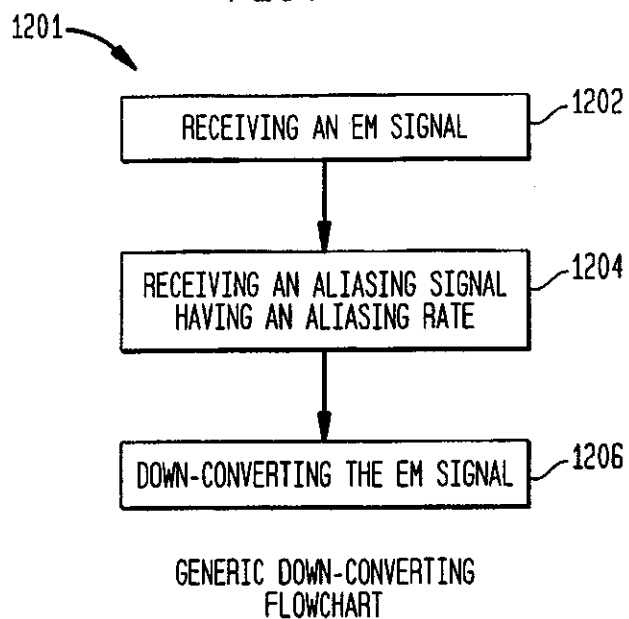
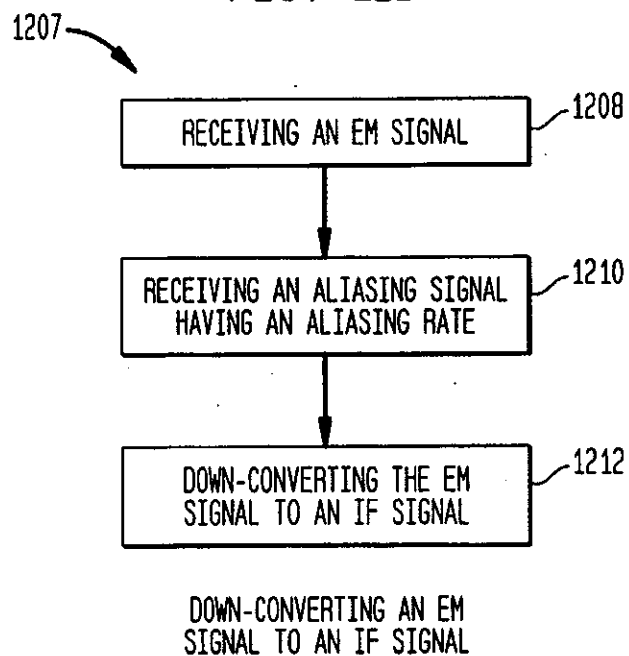
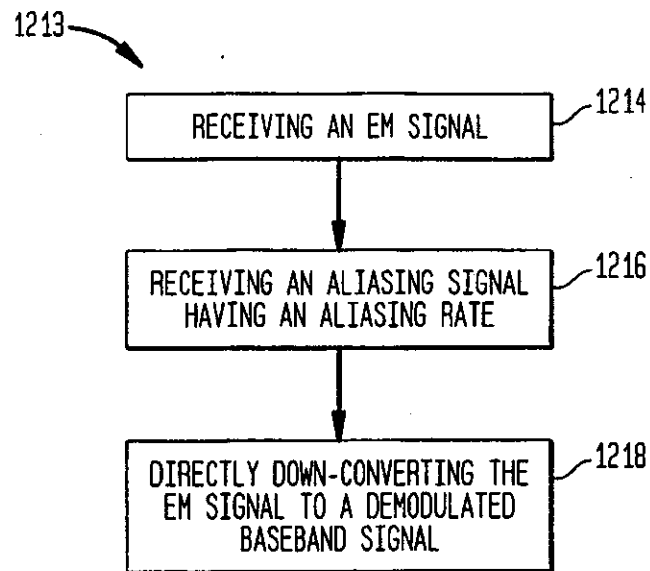


FIG. 12A**FIG. 12B**

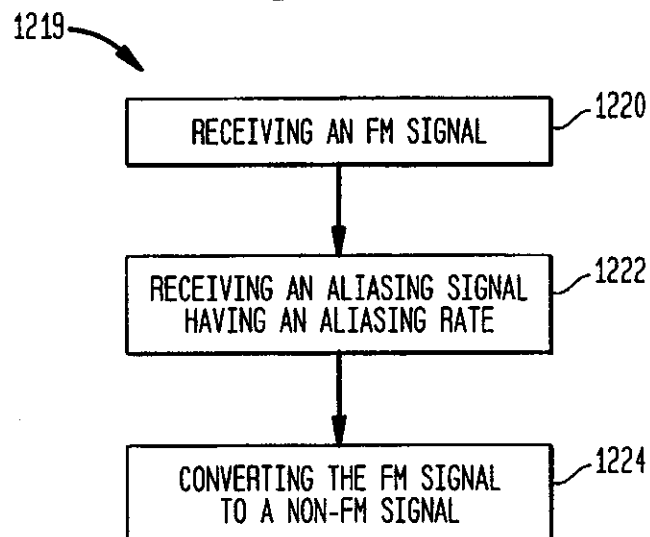
10/283

FIG. 12C



DIRECTLY DOWN-CONVERTING AN EM
SIGNAL TO A DEMODULATED BASEBAND SIGNAL

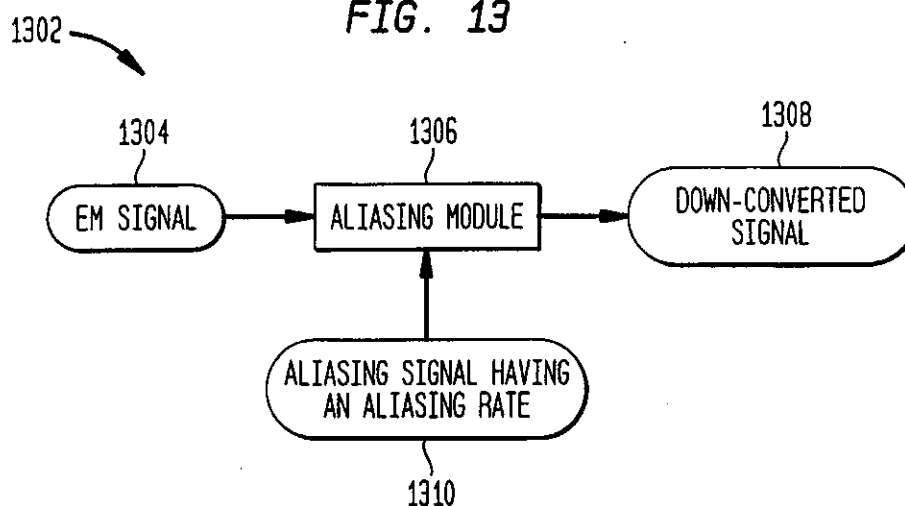
FIG. 12D



MODULATION CONVERSION

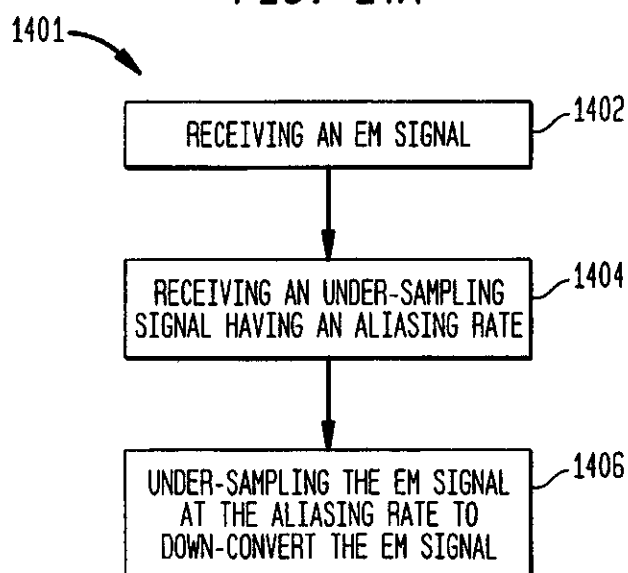
11/283

FIG. 13

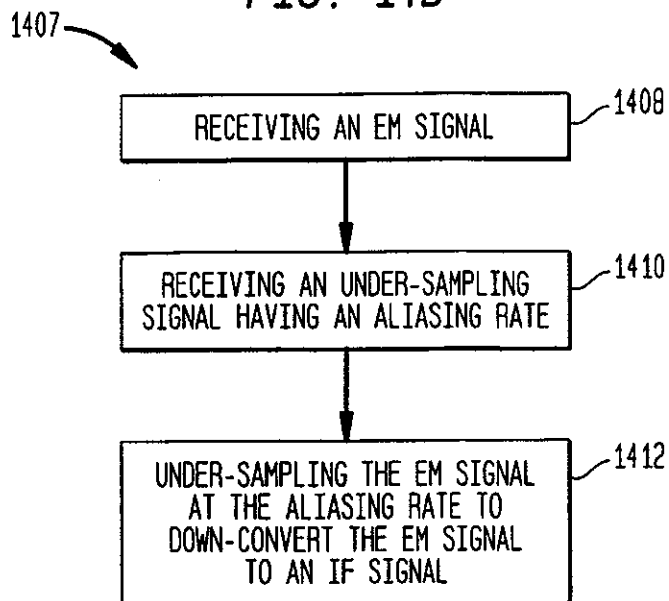
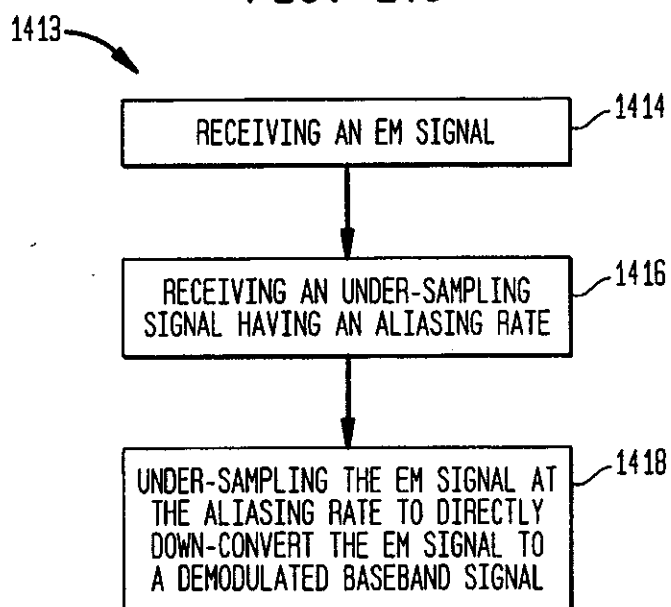


GENERIC DOWN-CONVERTING SYSTEM

FIG. 14A

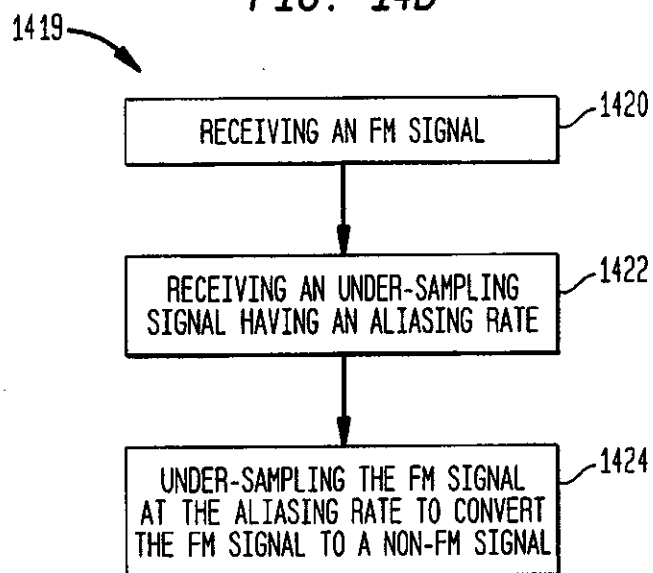


12/283

FIG. 14B**FIG. 14C**

13/283

FIG. 14D



14/283

FIG. 15E

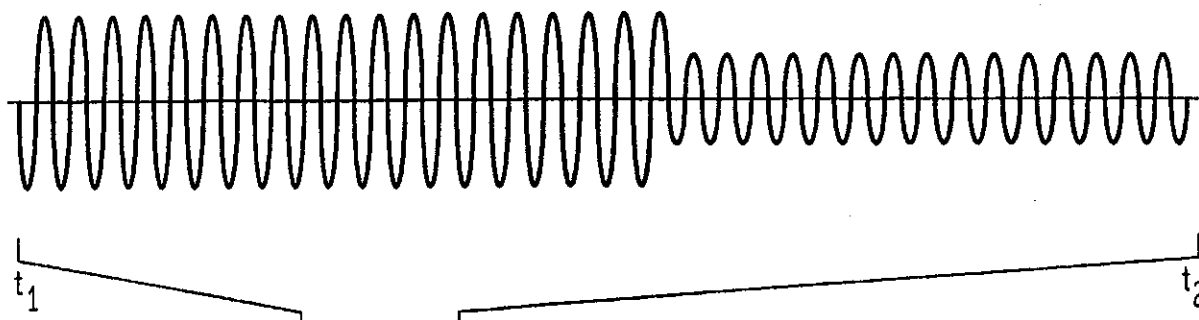


FIG. 15A

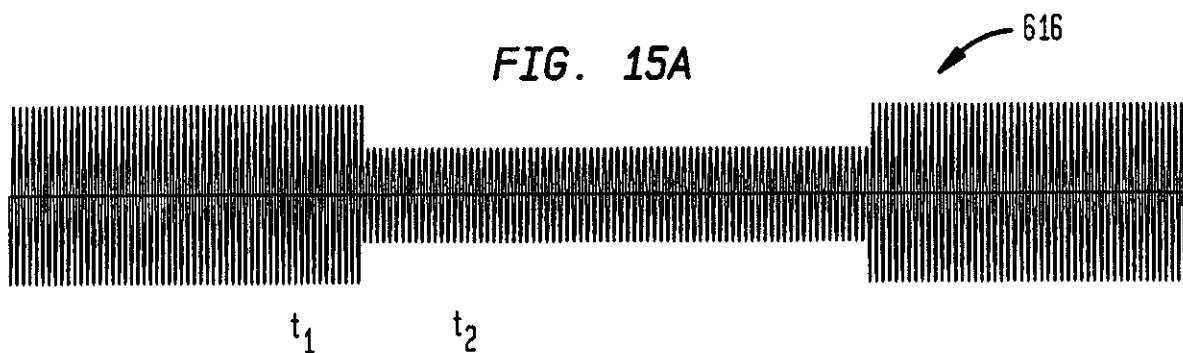


FIG. 15B

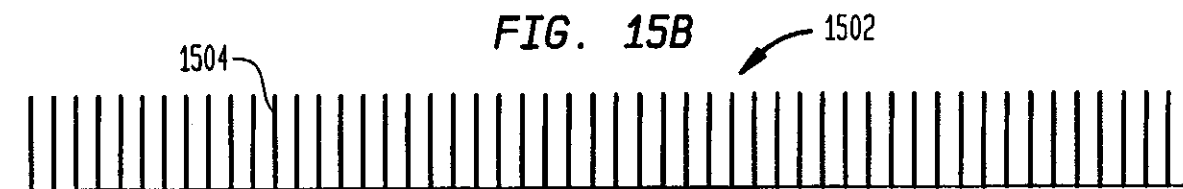


FIG. 15C

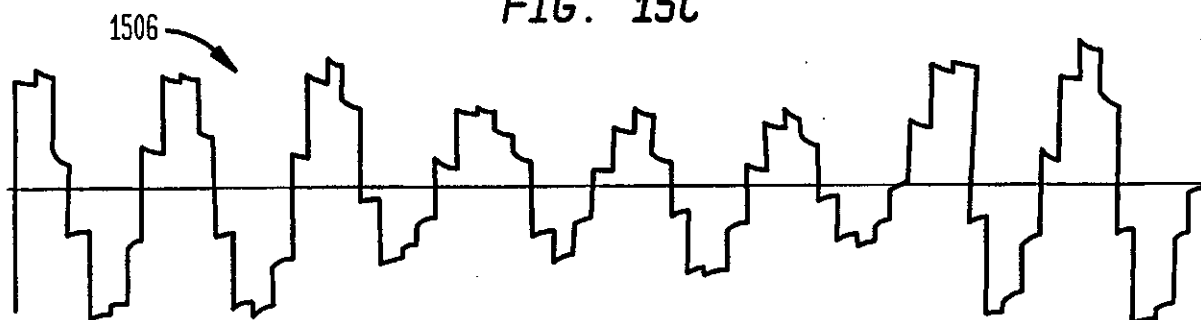
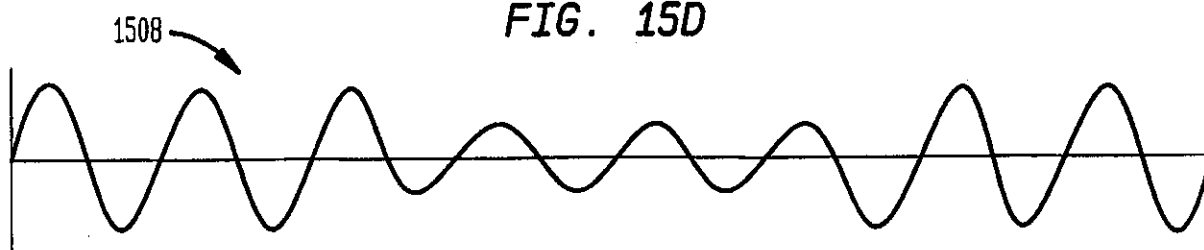


FIG. 15D



15/283

FIG. 16

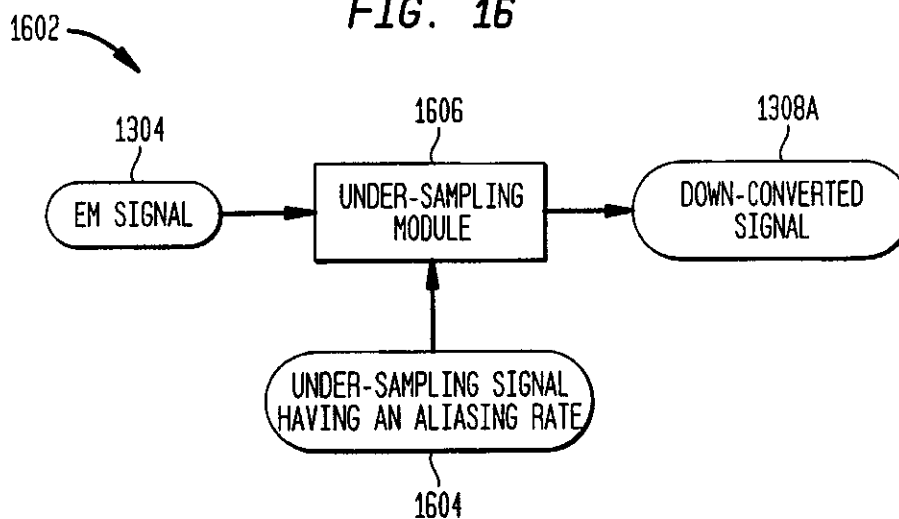
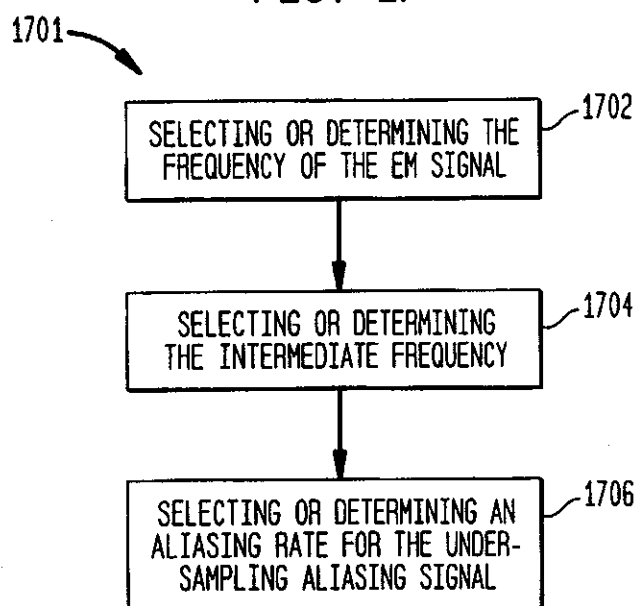


FIG. 17



16/283

FIG. 18A

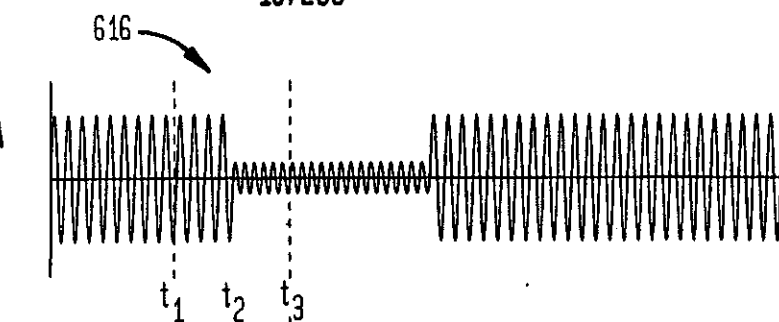


FIG. 18B

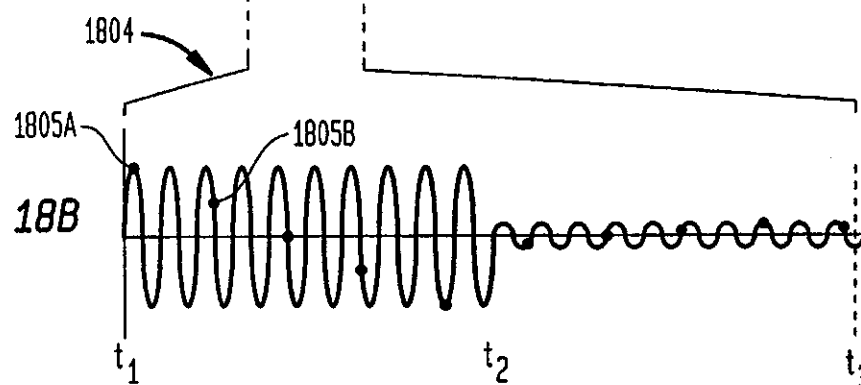


FIG. 18C

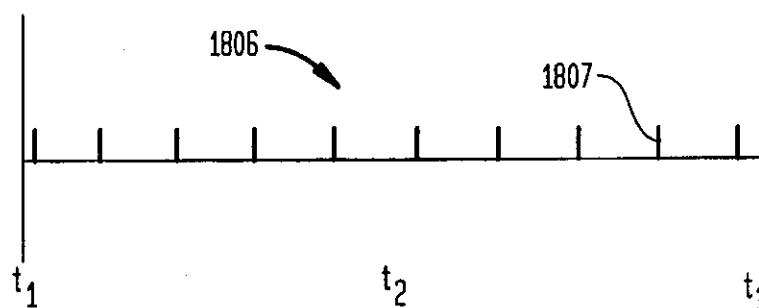


FIG. 18D

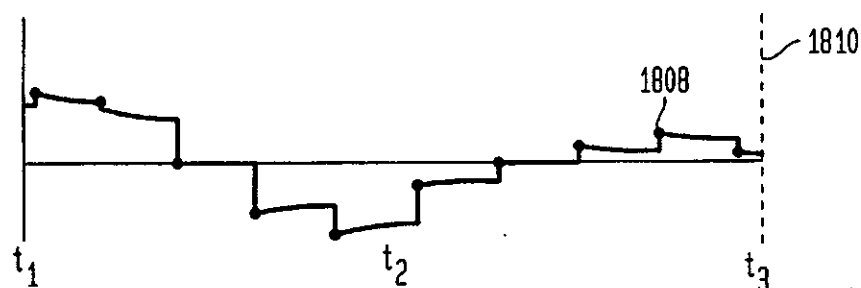
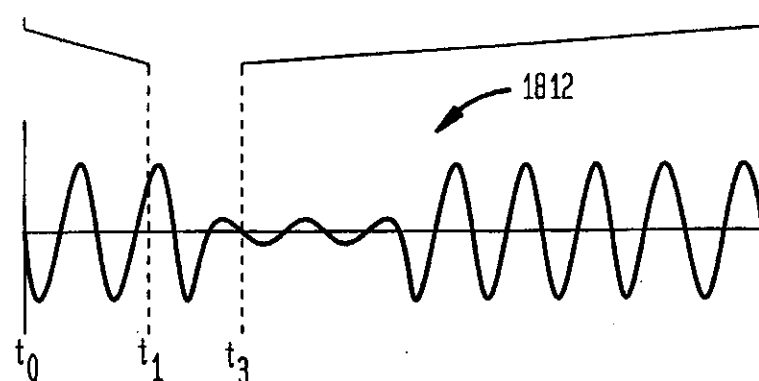


FIG. 18E



17/283

FIG. 19A

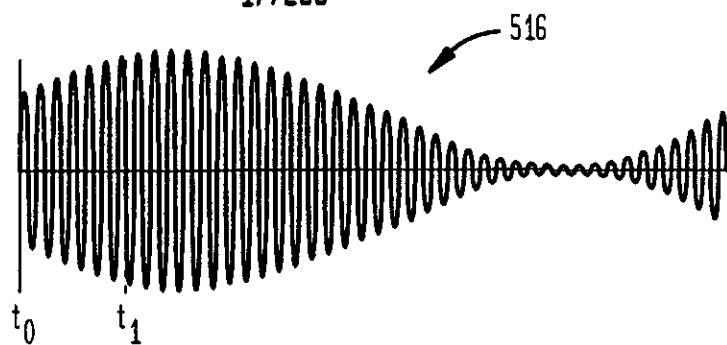


FIG. 19B

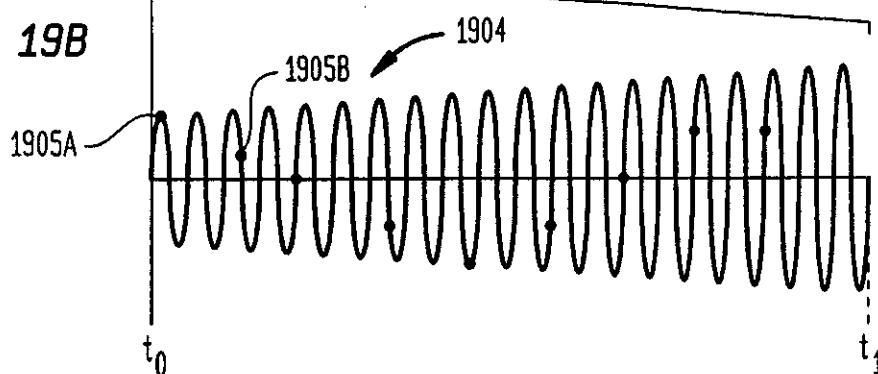


FIG. 19C

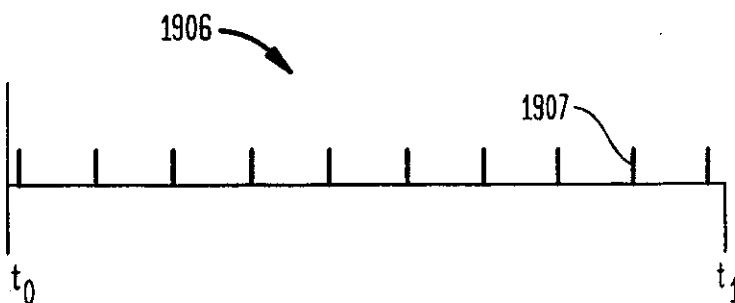


FIG. 19D

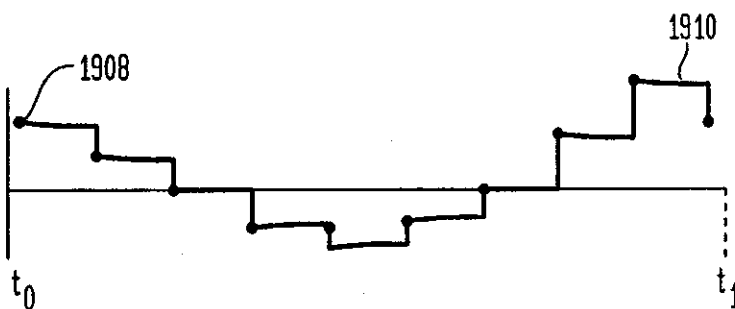
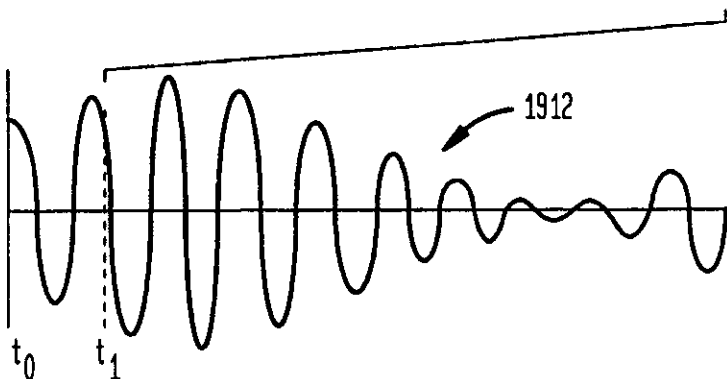


FIG. 19E



18/283

716

FIG. 20A

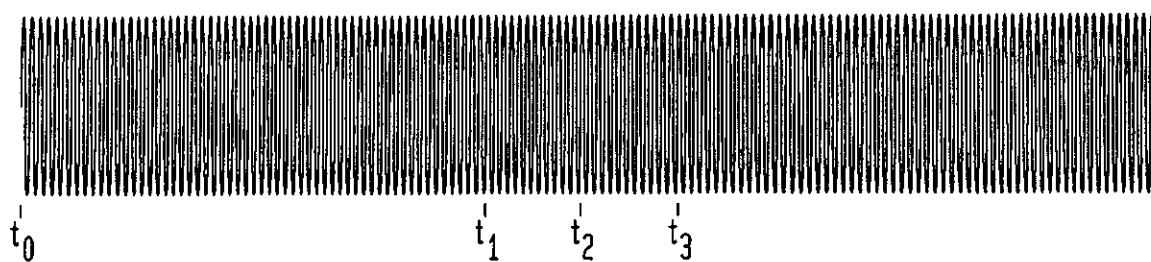


FIG. 20B

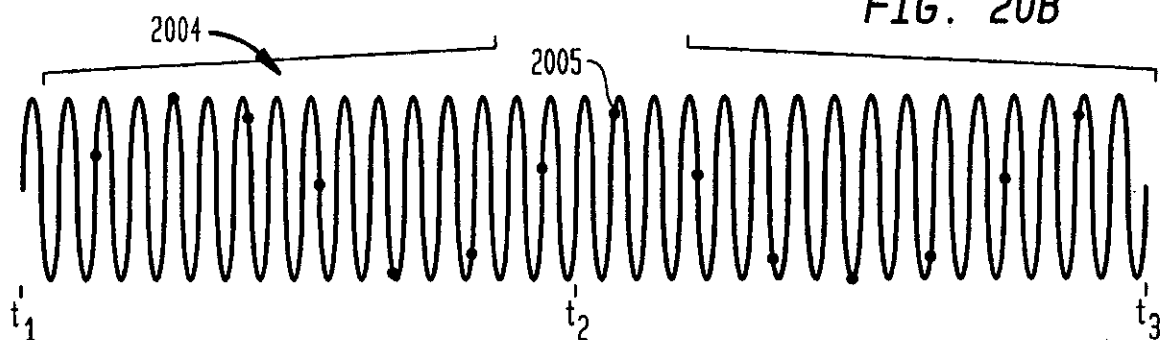


FIG. 20C

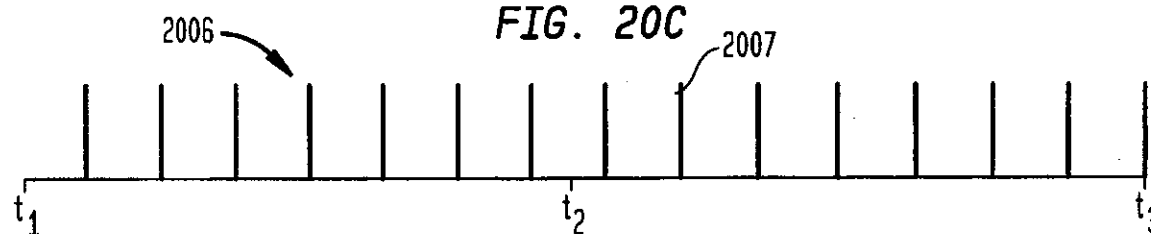


FIG. 20D

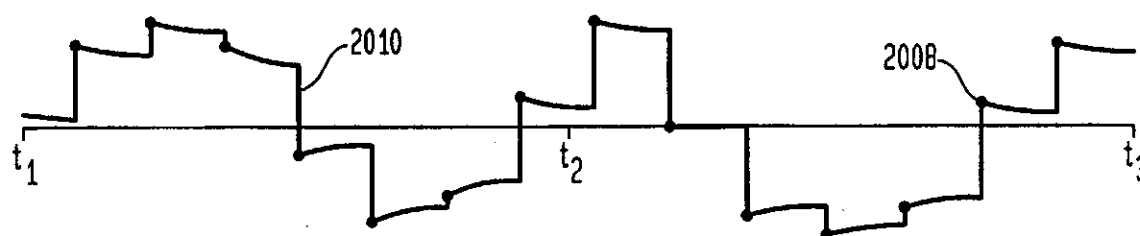
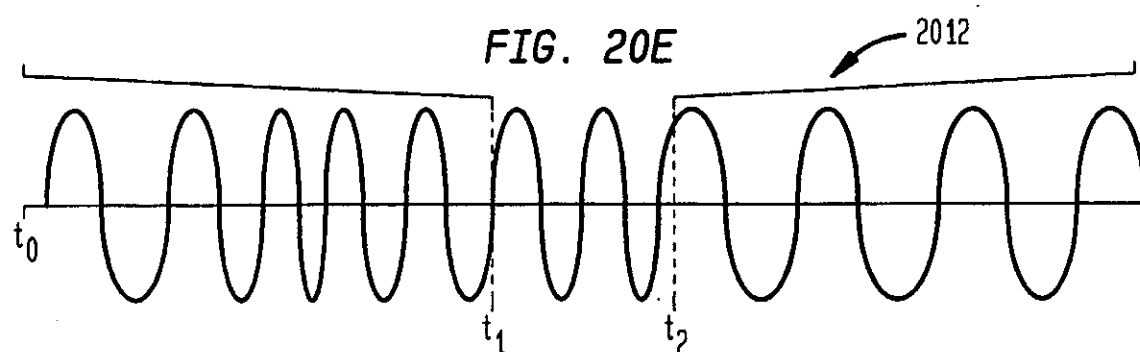


FIG. 20E



19/283

FIG. 21A

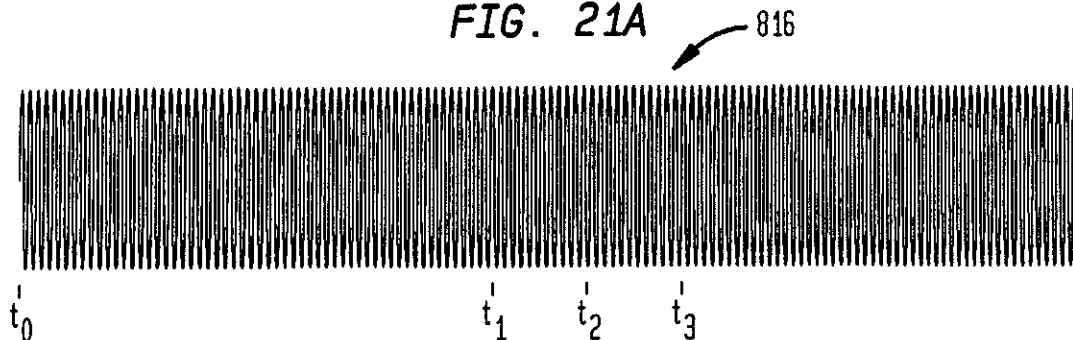


FIG. 21B

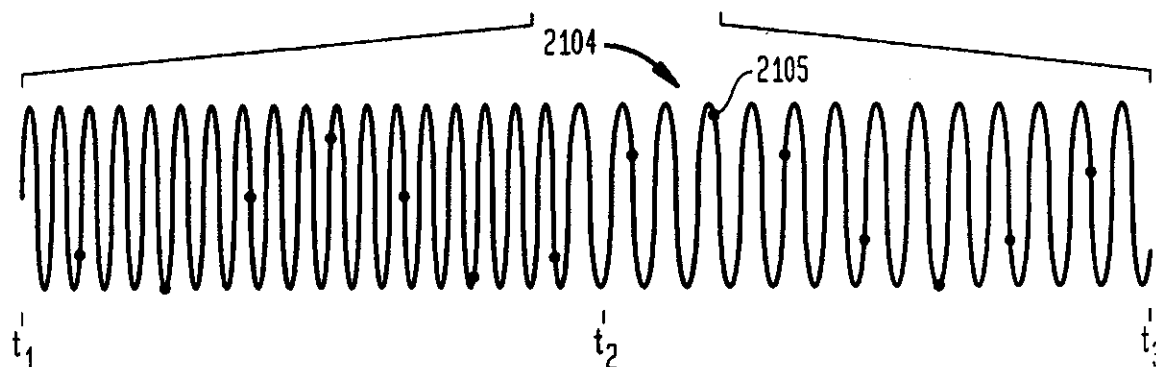


FIG. 21C

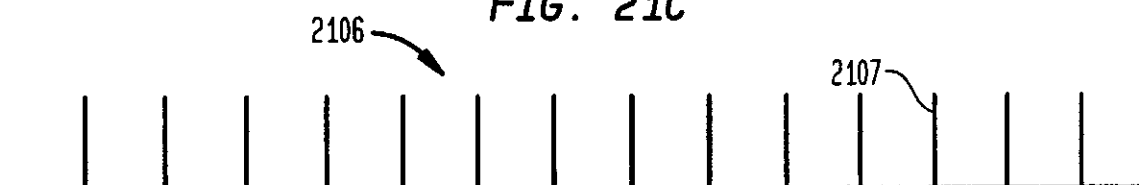


FIG. 21D

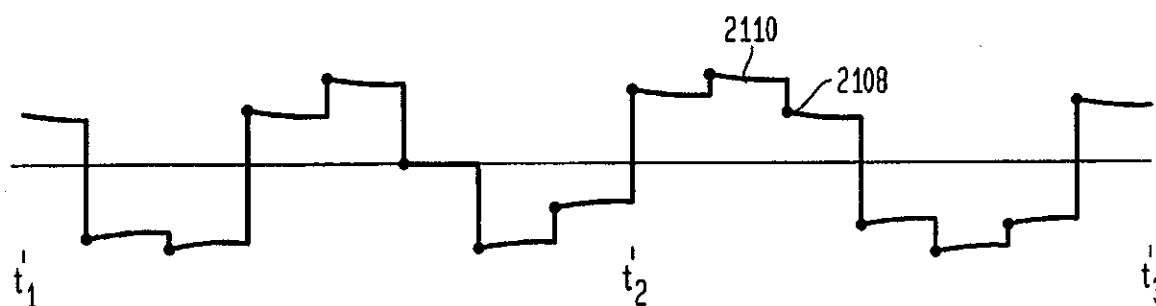
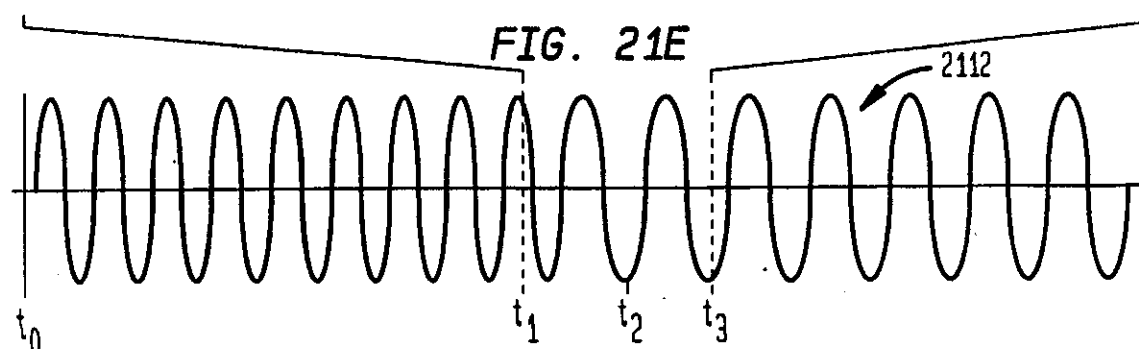


FIG. 21E



20/283

FIG. 22A

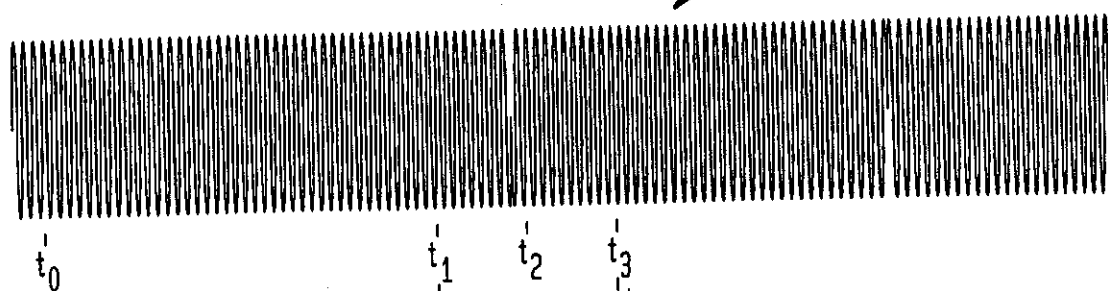


FIG. 22B

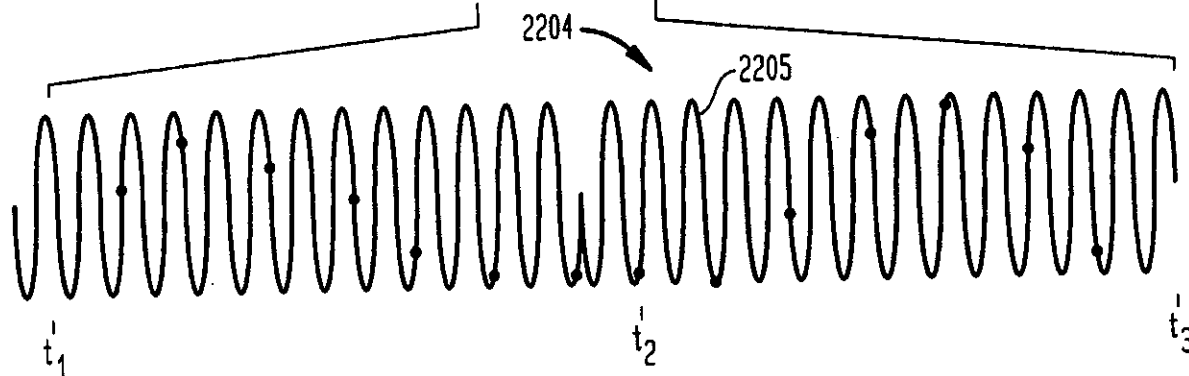


FIG. 22C

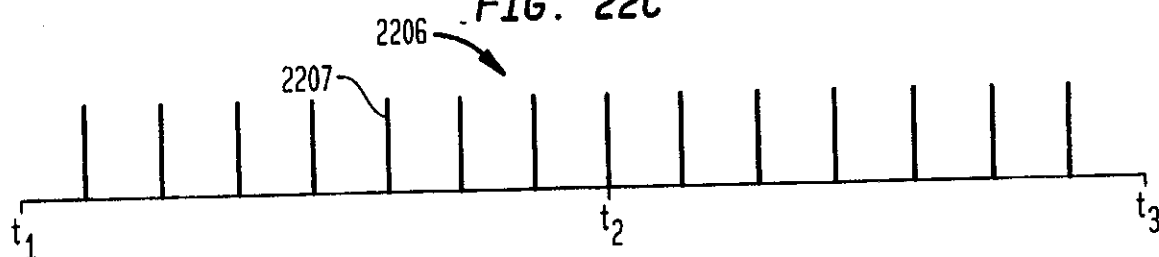


FIG. 22D

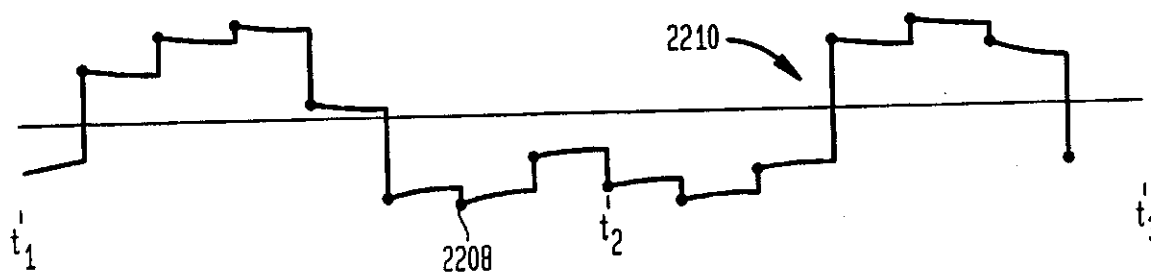
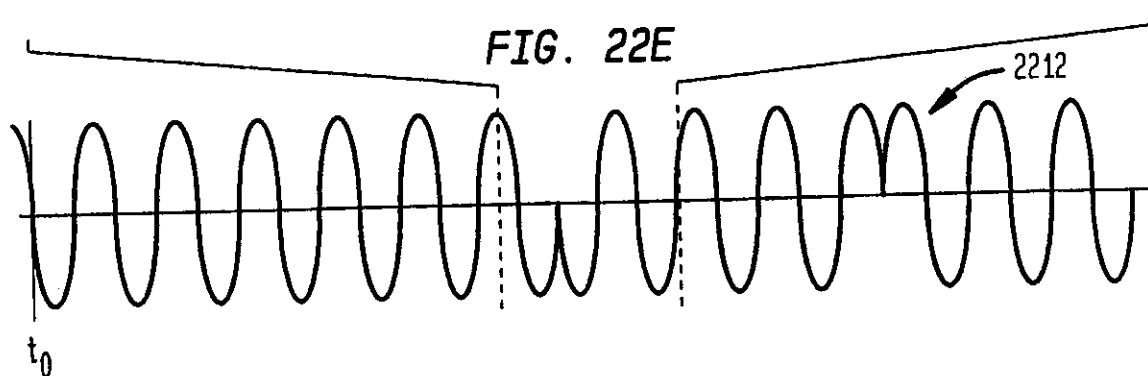


FIG. 22E



21/283

FIG. 23A

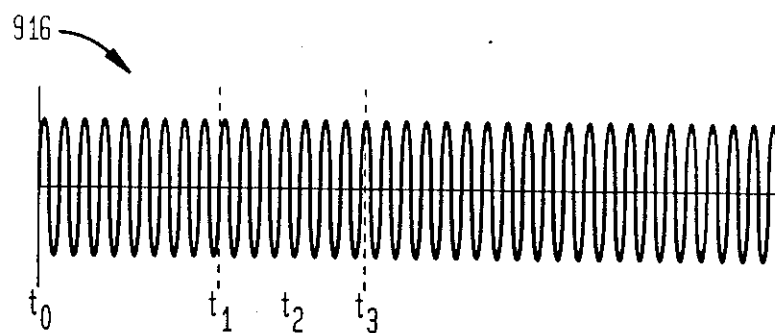


FIG. 23B

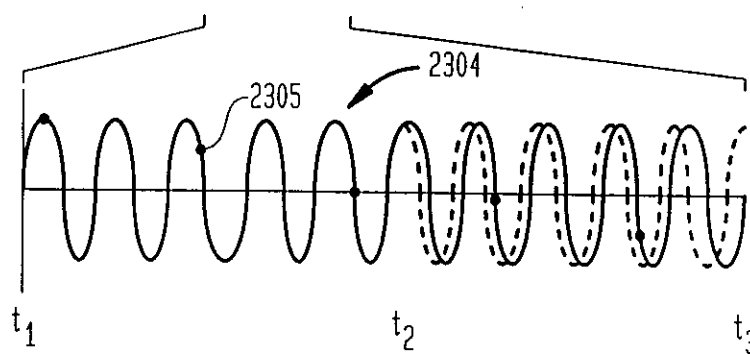


FIG. 23C



FIG. 23D

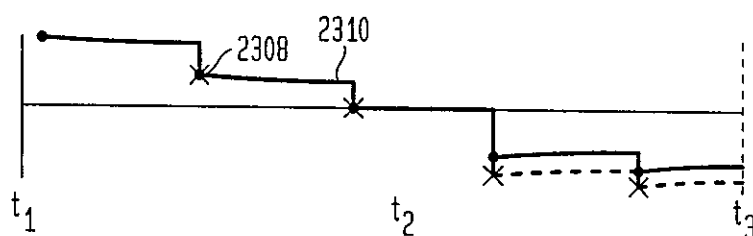


FIG. 23E

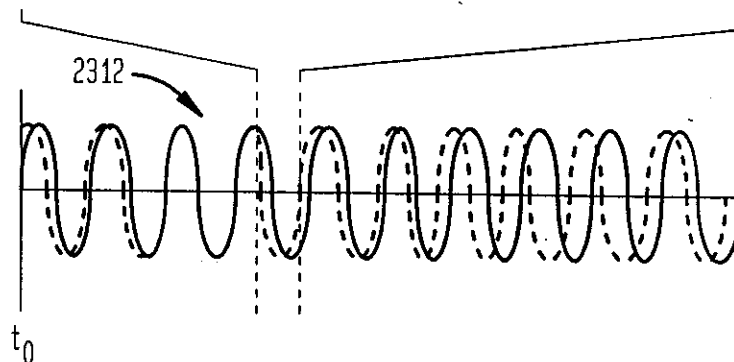
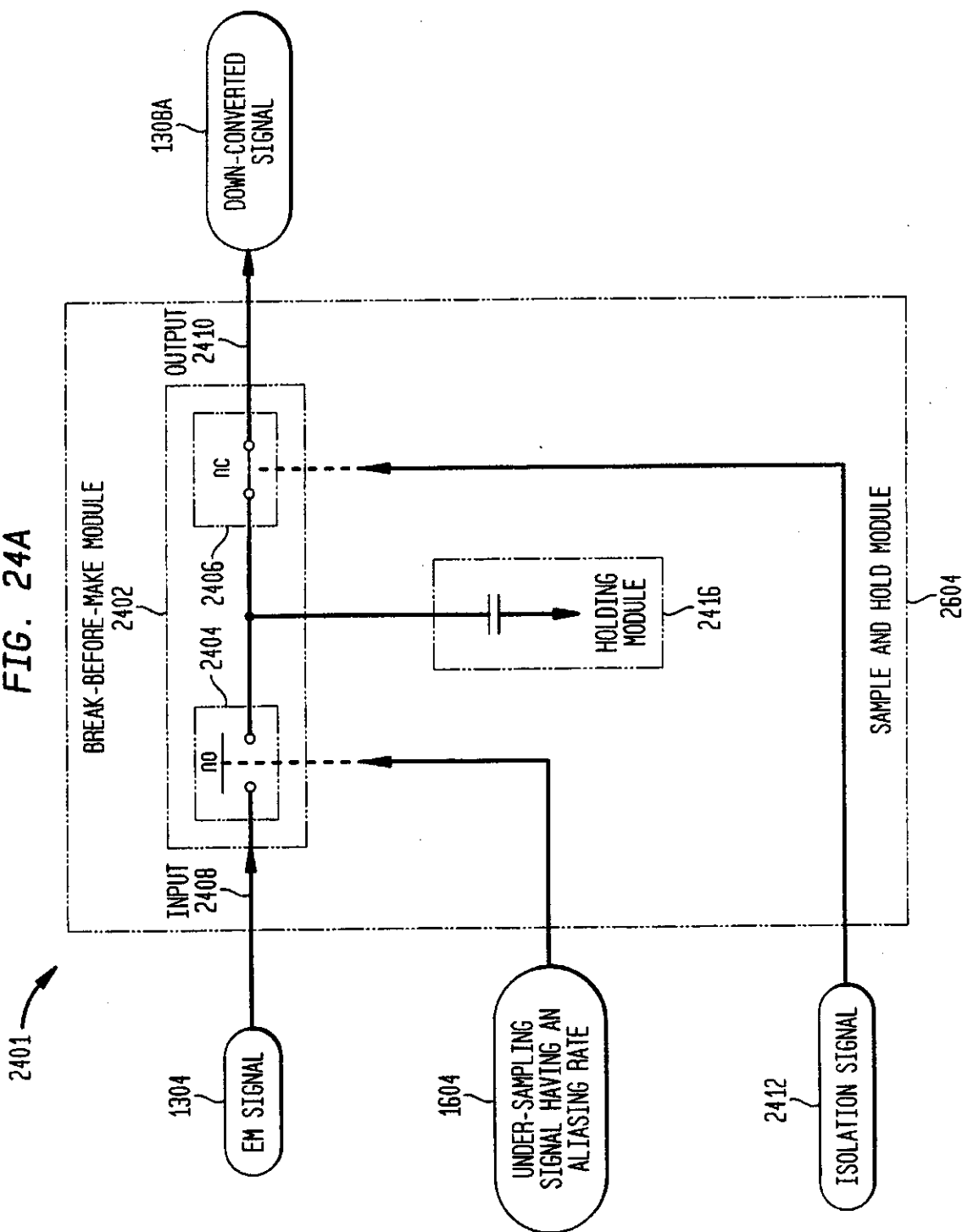


FIG. 24A



23/283

FIG. 24B

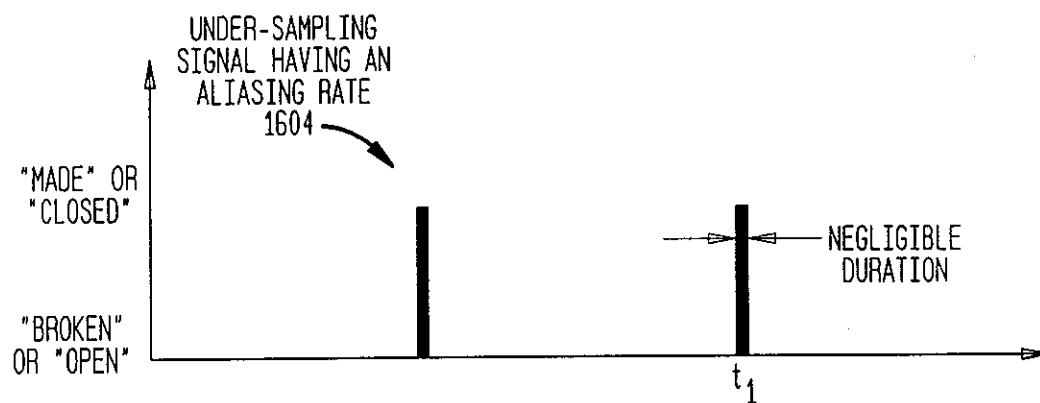
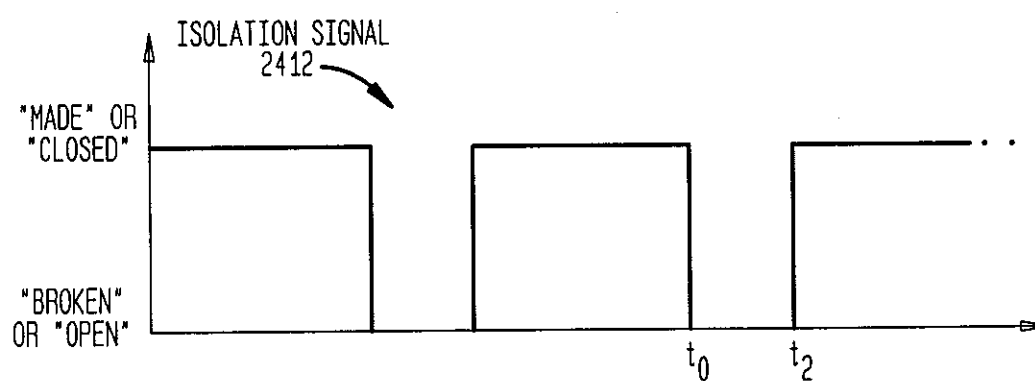
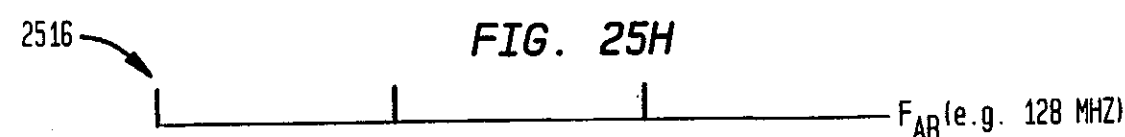
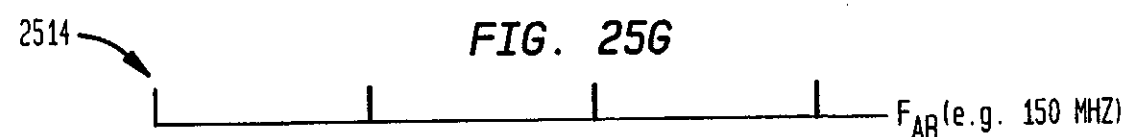
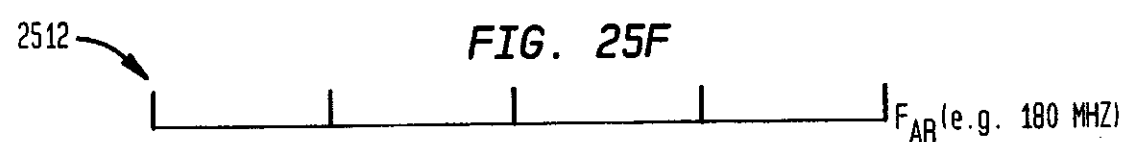
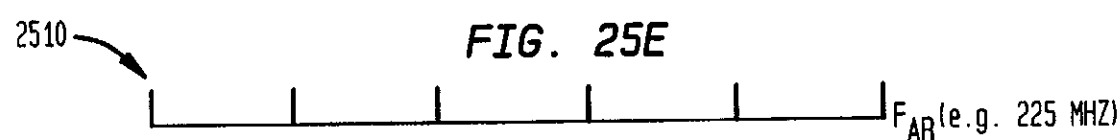
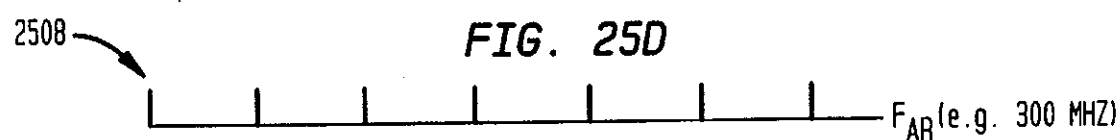
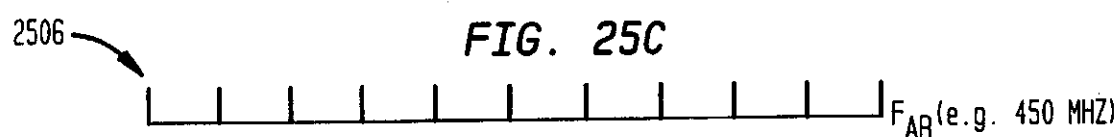
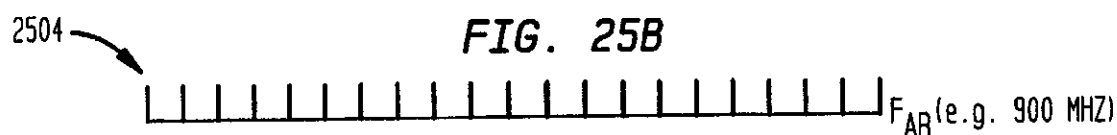
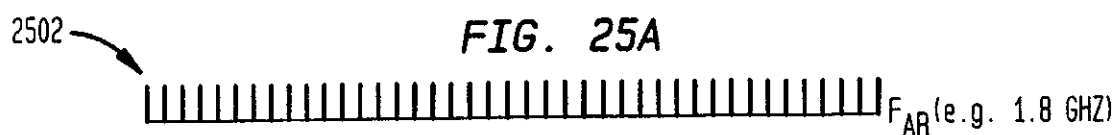


FIG. 24C





25/283

FIG. 26A

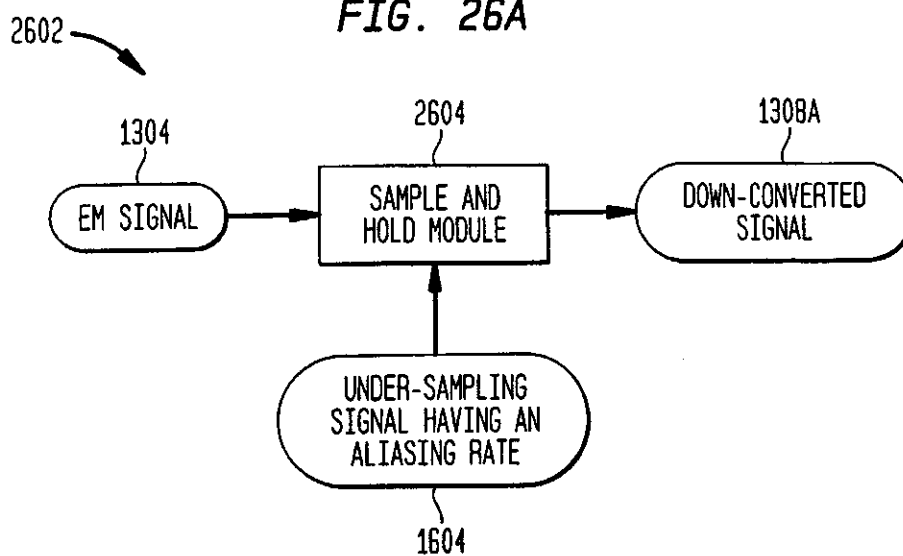
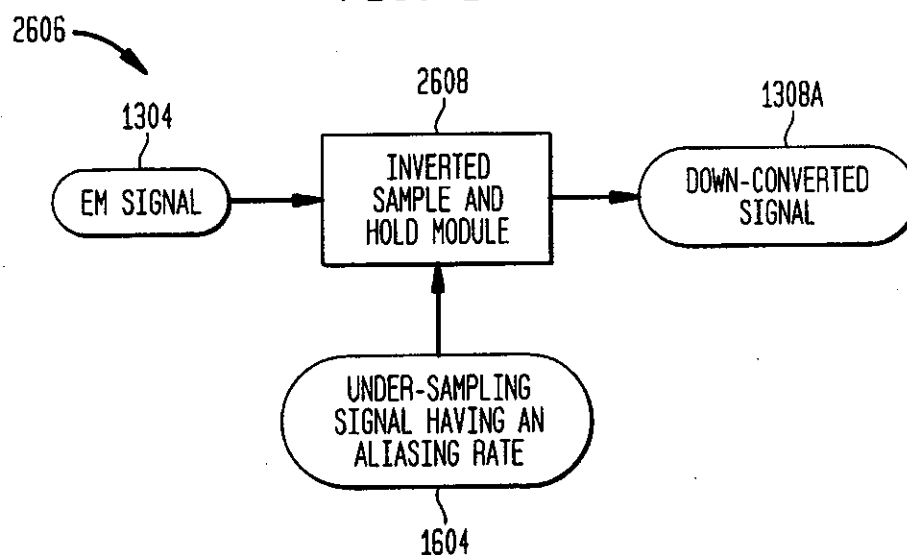
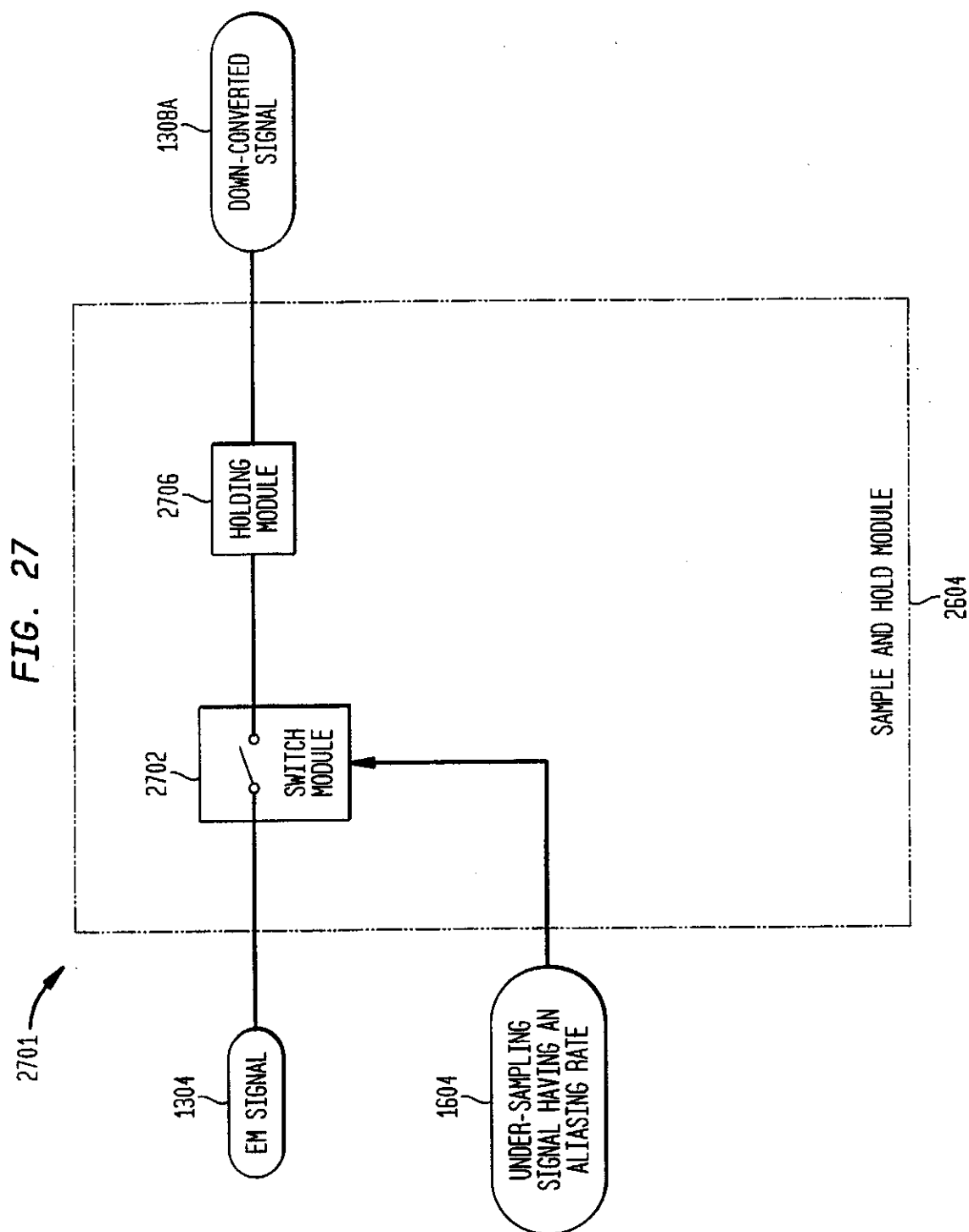


FIG. 26B





27/283

FIG. 28A

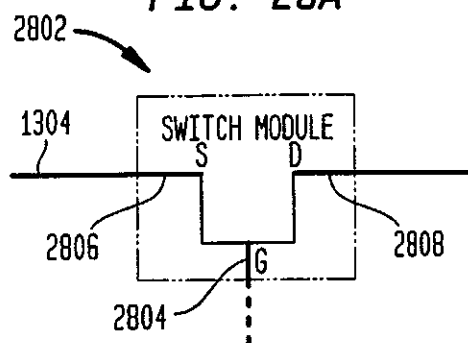


FIG. 28B

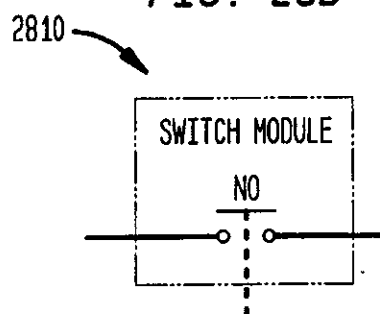


FIG. 28C

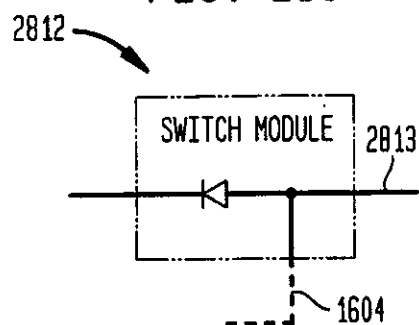
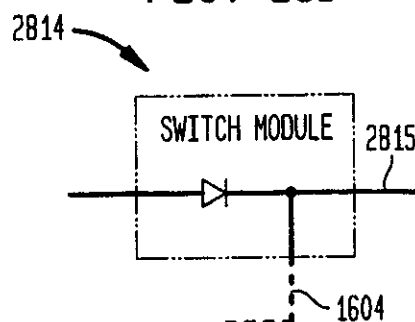


FIG. 28D



28/283

FIG. 29A

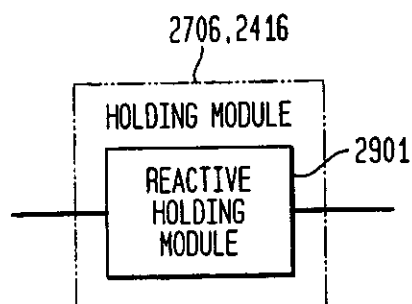


FIG. 29B

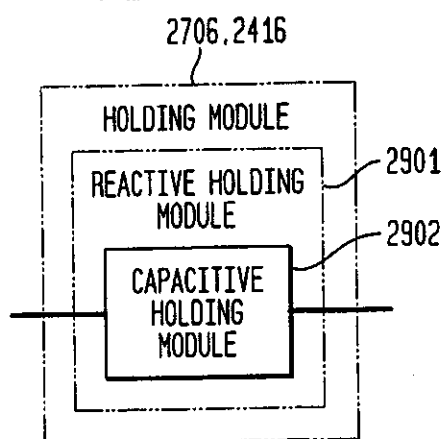
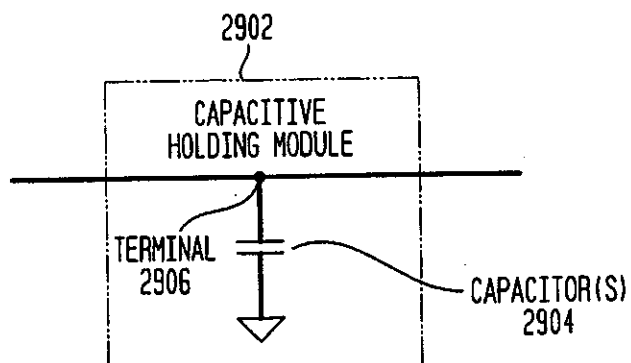


FIG. 29C



29/283

FIG. 29D

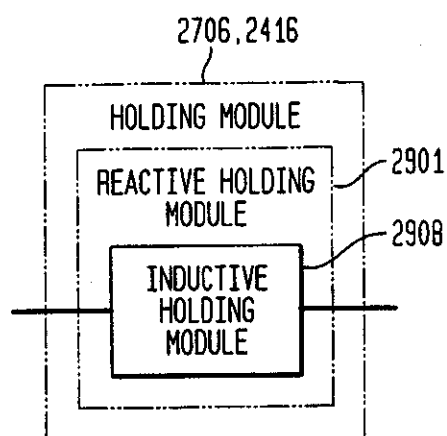


FIG. 29E

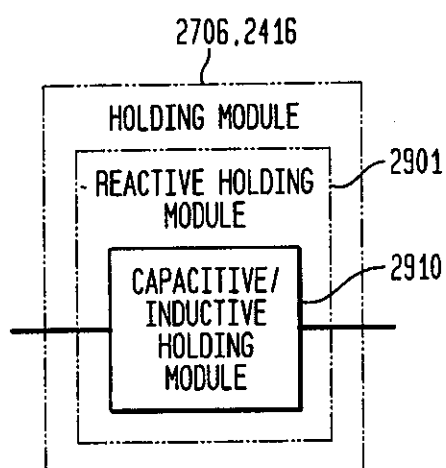
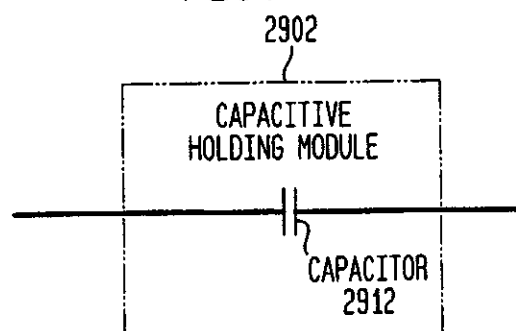
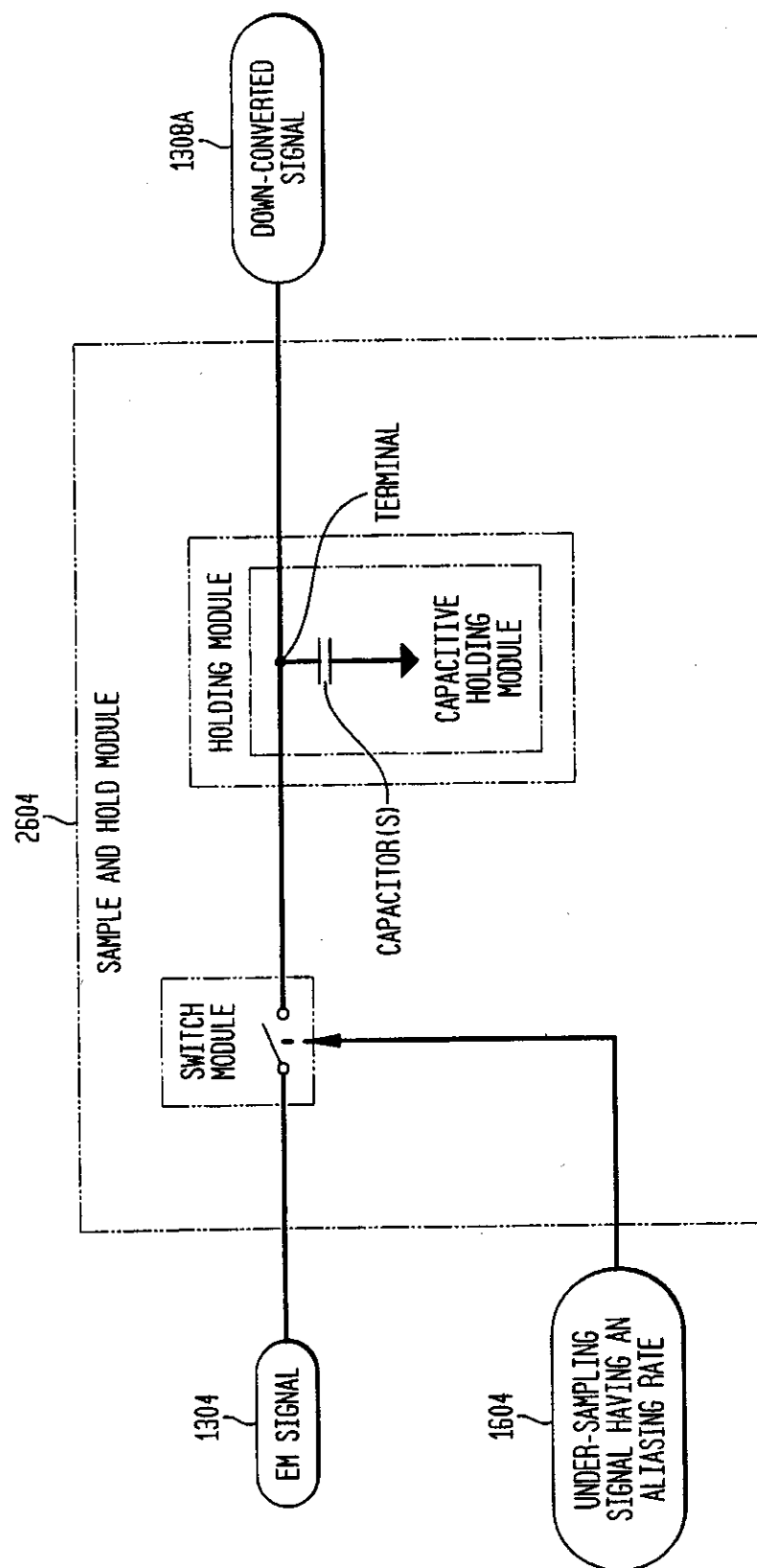


FIG. 29F



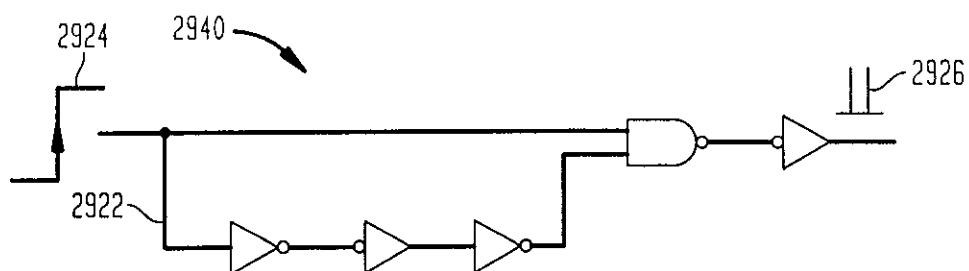
30/283

FIG. 296



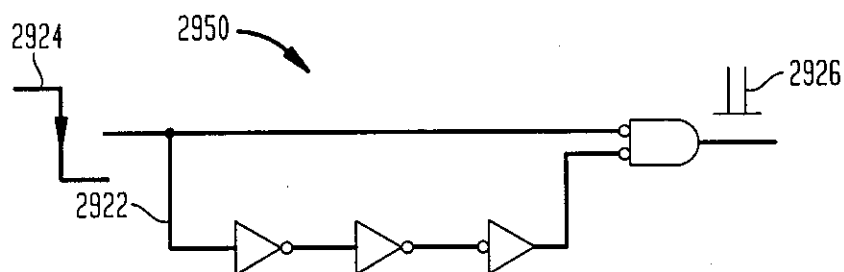
31/283

FIG. 29H



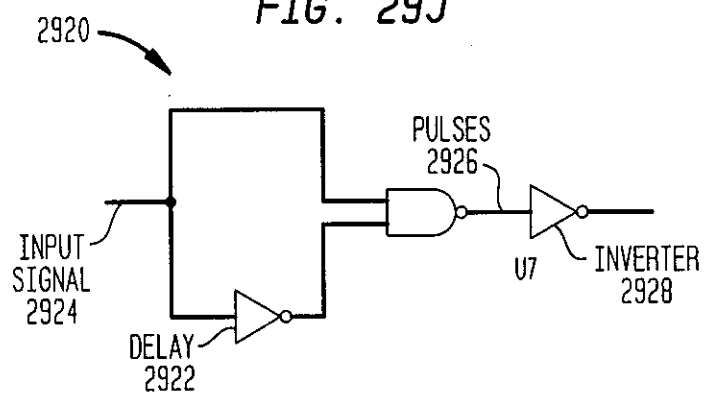
A. RISING EDGE PULSE GENERATOR

FIG. 29I



B. FALLING-EDGE PULSE GENERATOR

FIG. 29J



32/283

FIG. 29K

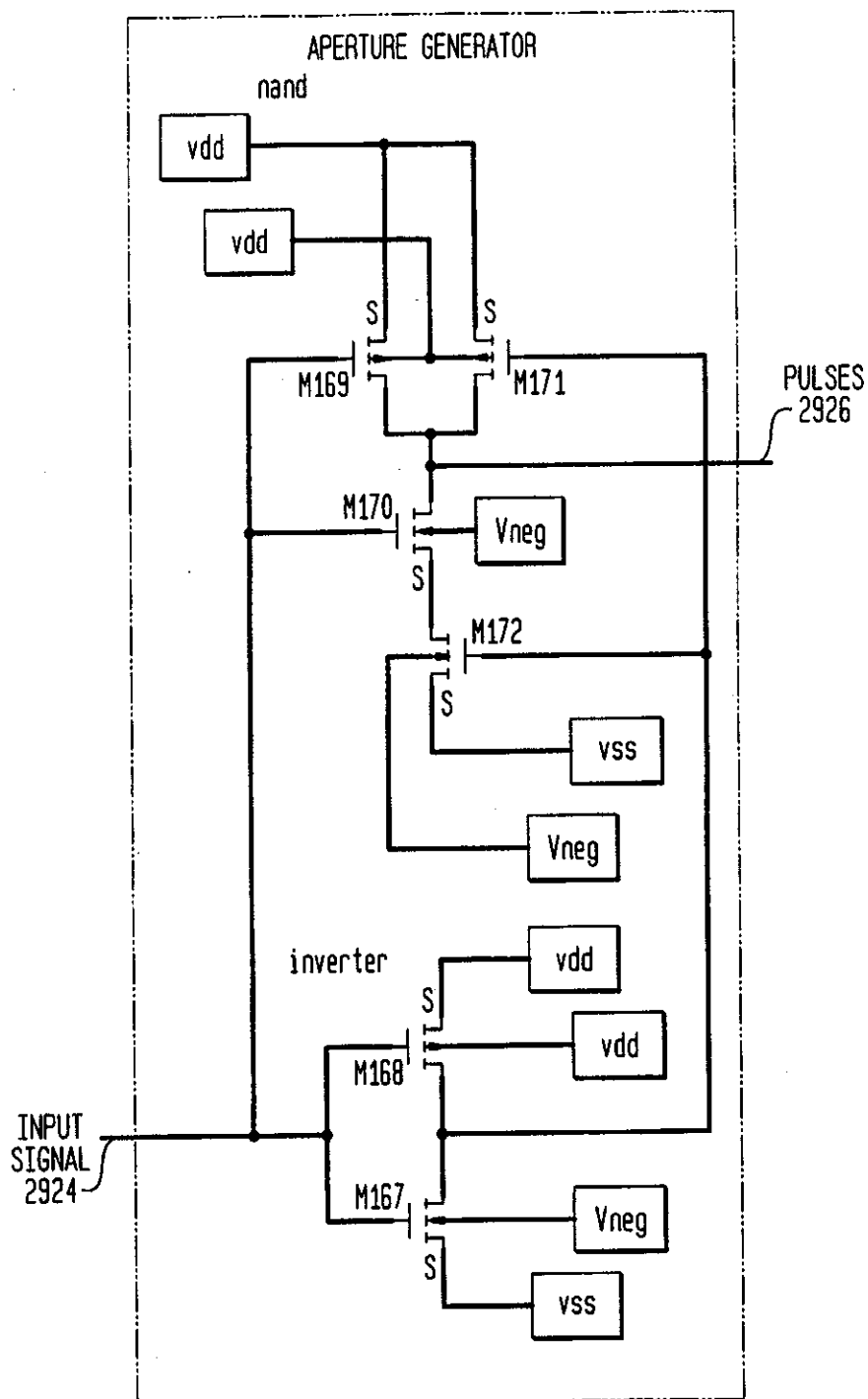


FIG. 29L

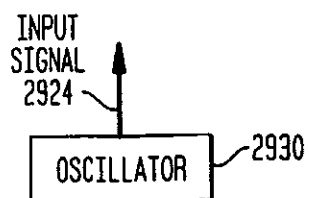


FIG. 30

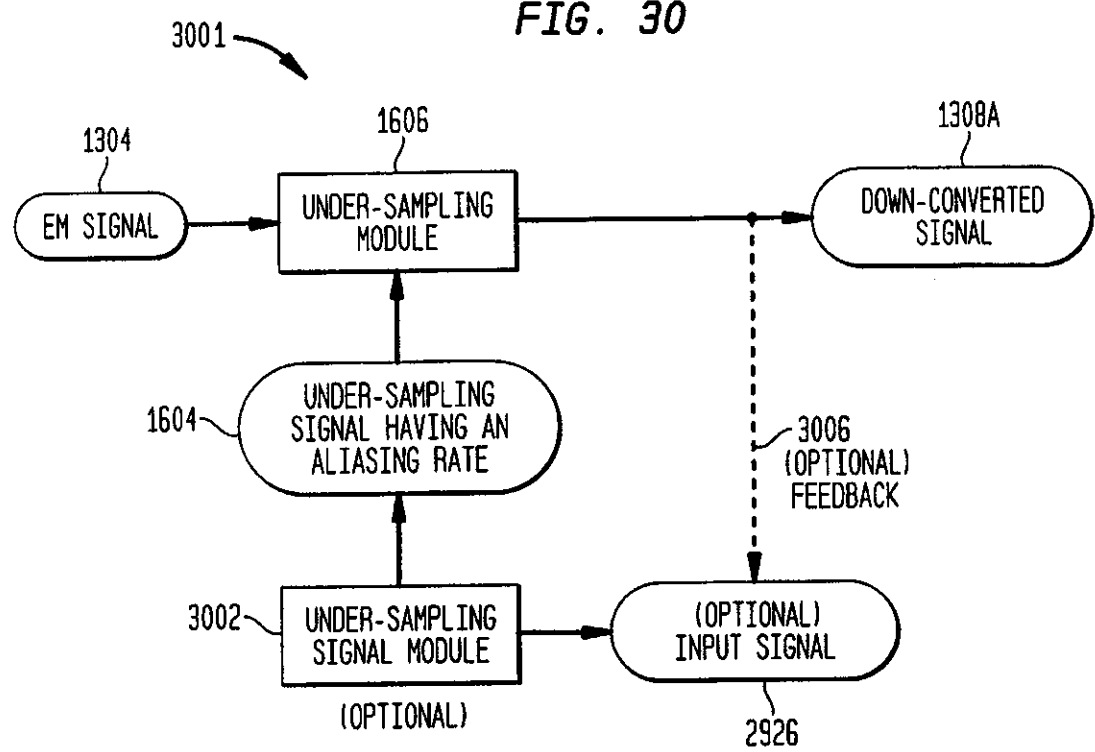


FIG. 31A

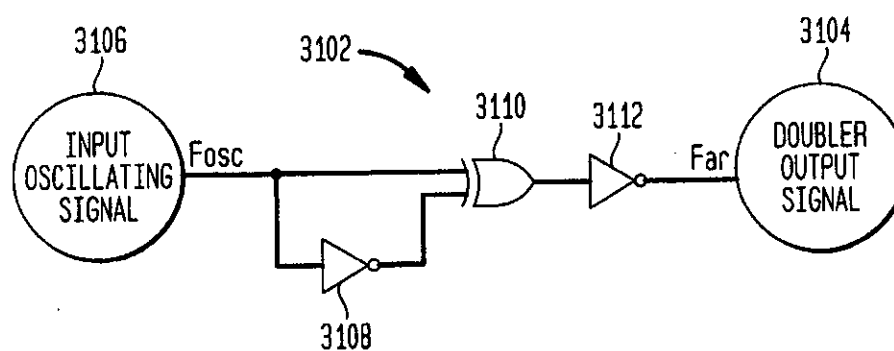


FIG. 31B

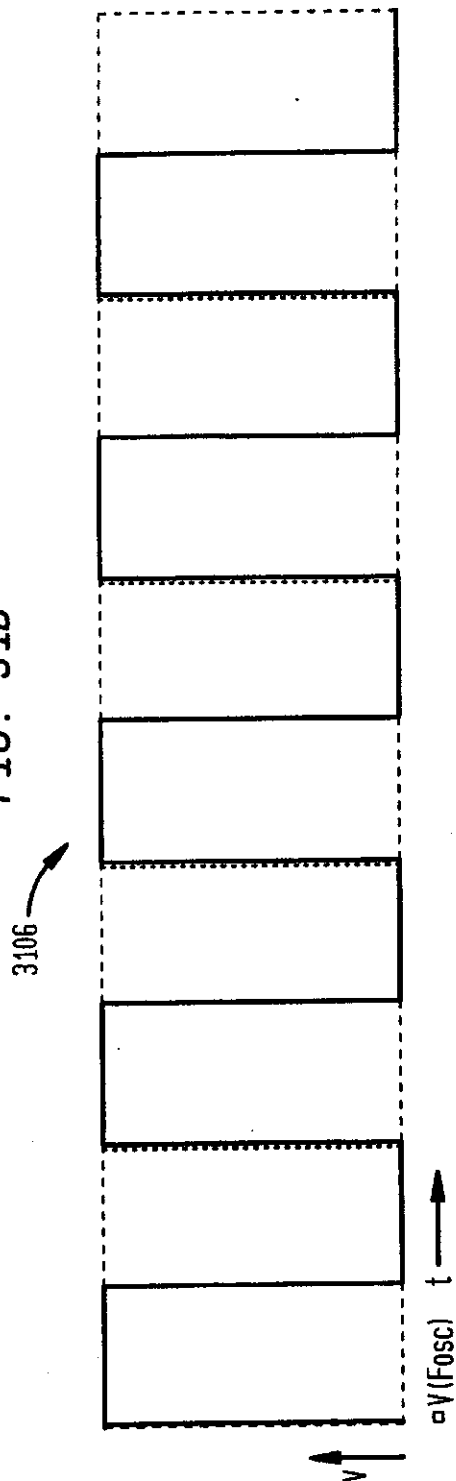


FIG. 31C

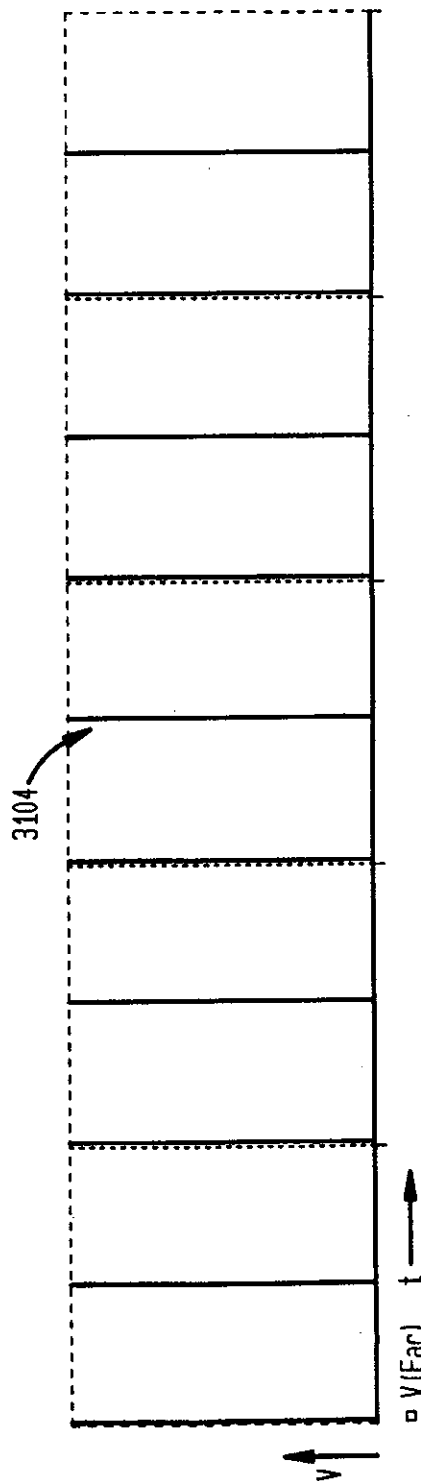
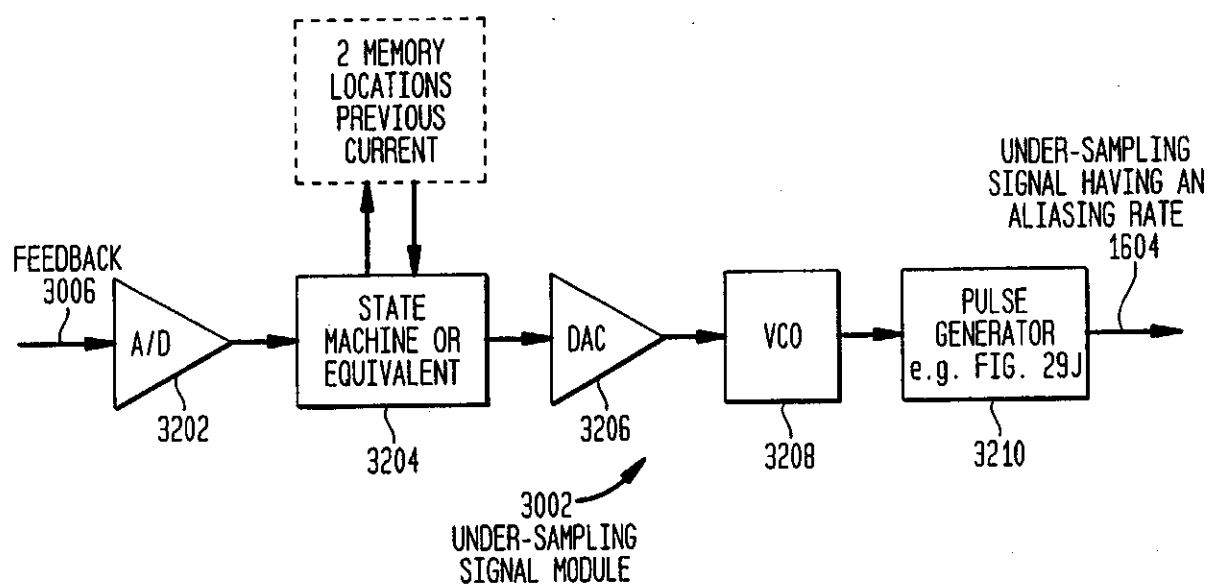
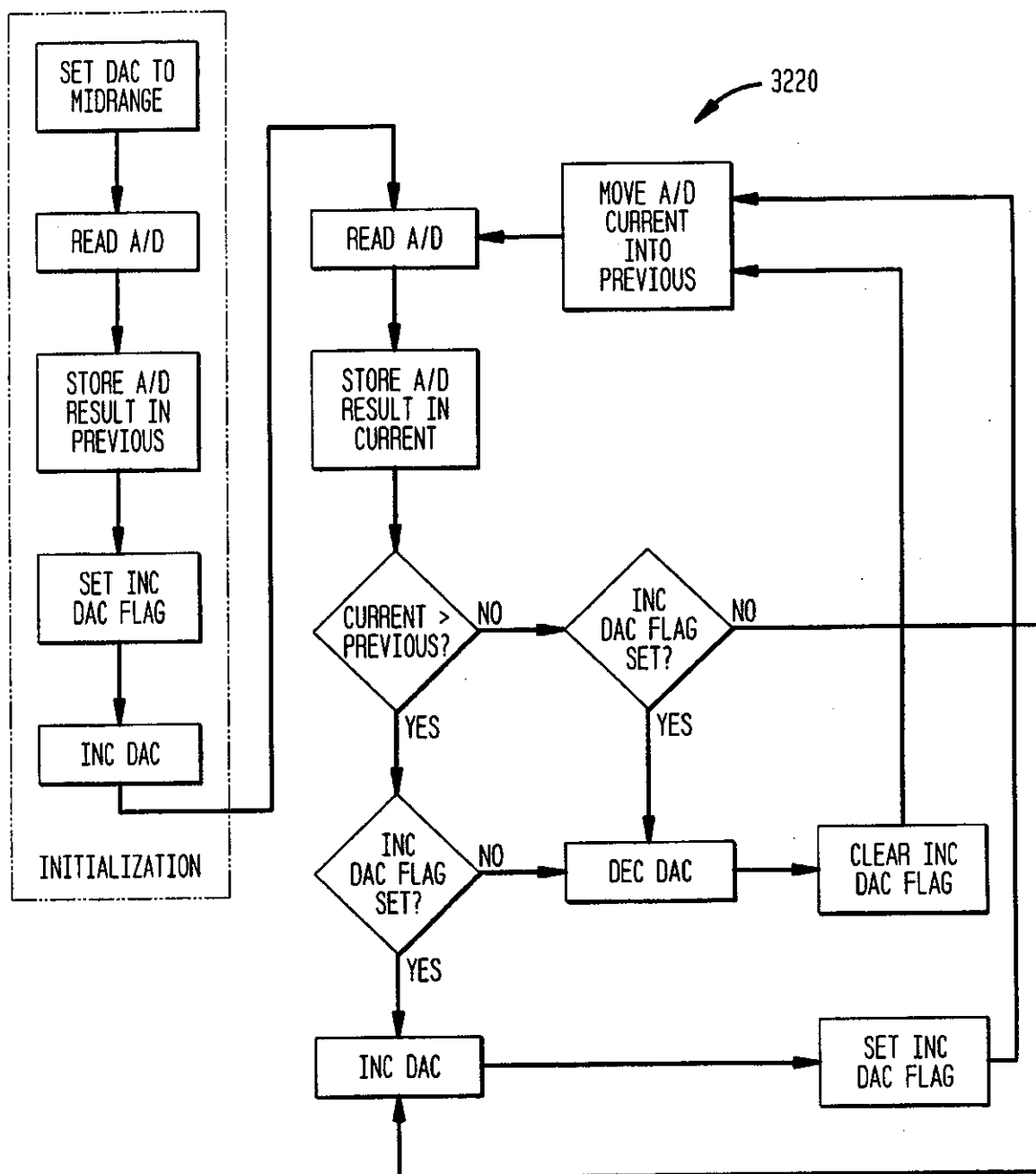


FIG. 32A



37/283

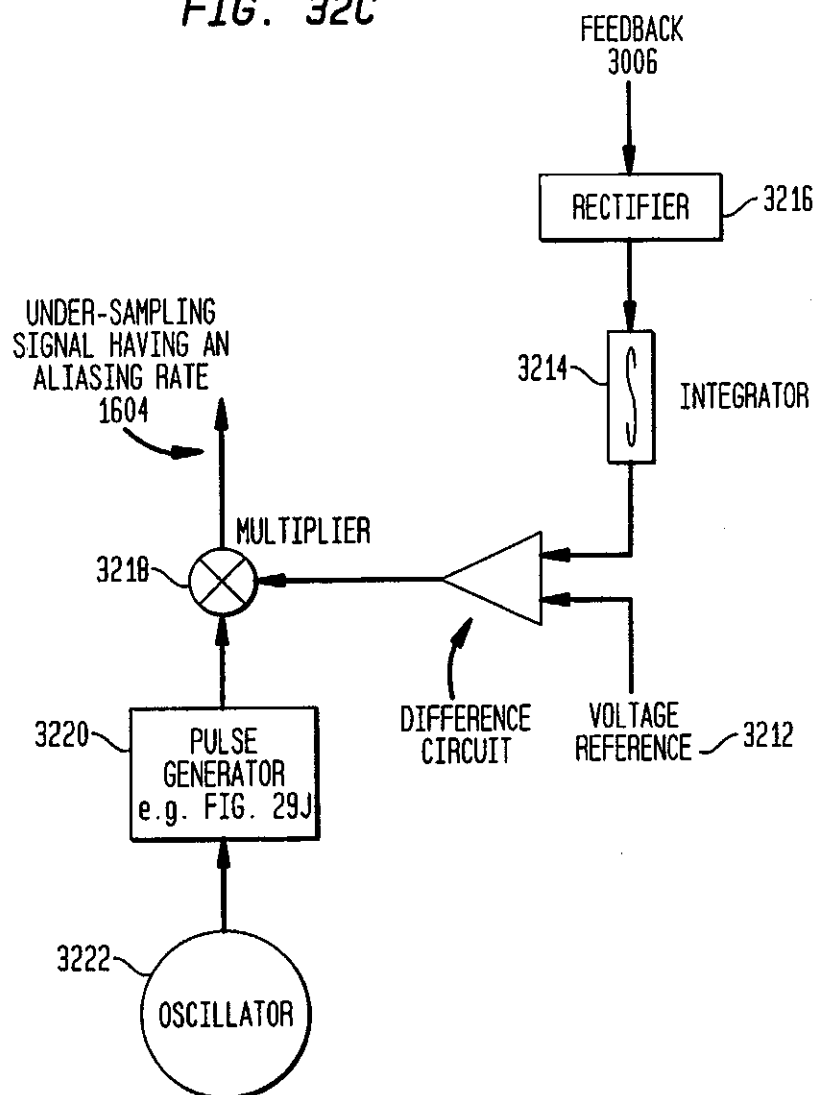
FIG. 32B



STATE MACHINE FLOWCHART

38/283

FIG. 32C



ENERGY TRANSFER SIGNAL MODULE 3002

39/283

FIG. 33A

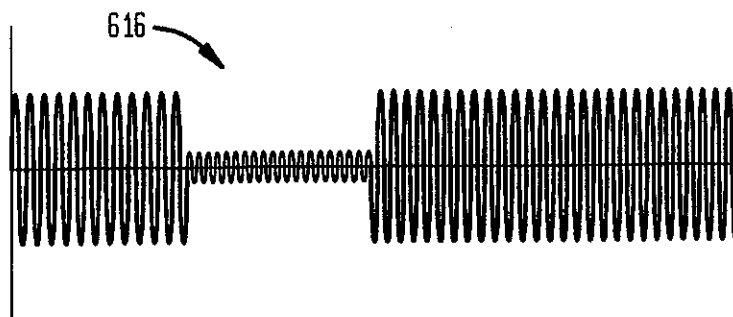


FIG. 33B

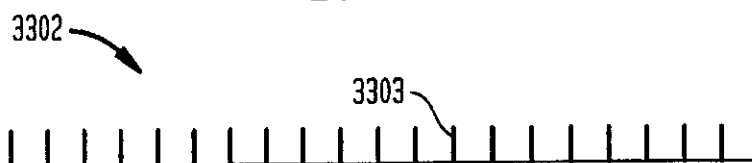


FIG. 33C

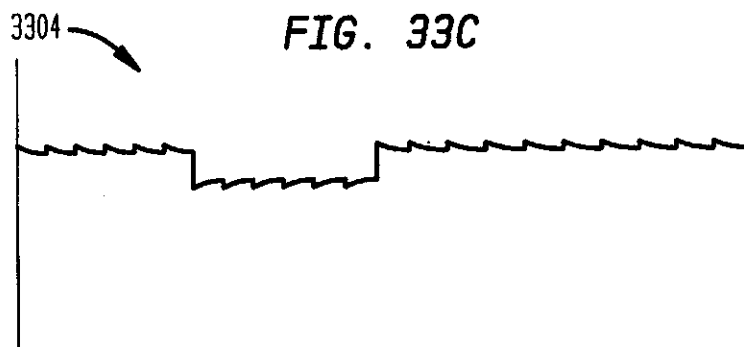


FIG. 33D

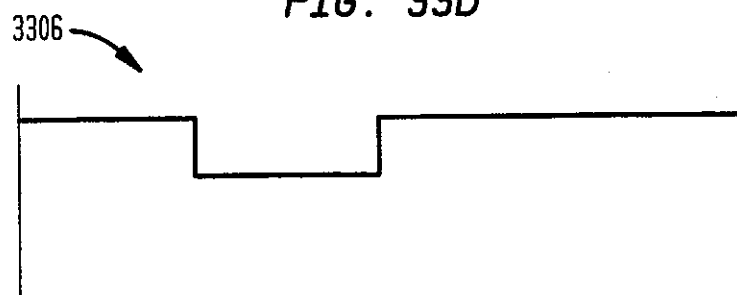


FIG. 34A

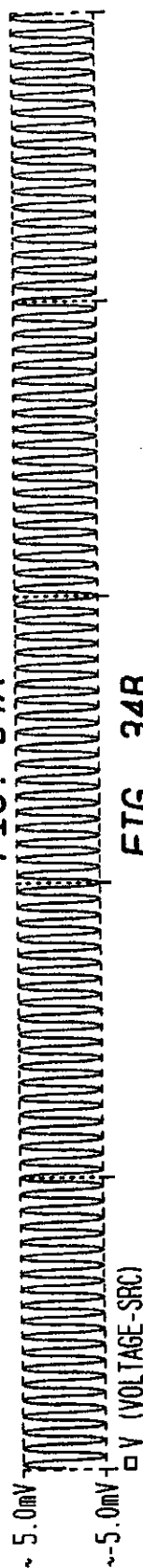


FIG. 34B

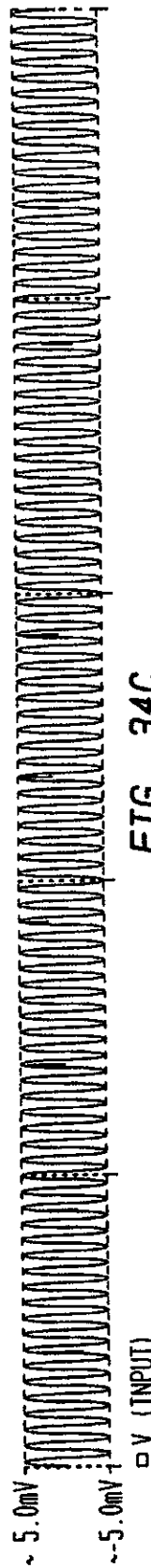


FIG. 34C

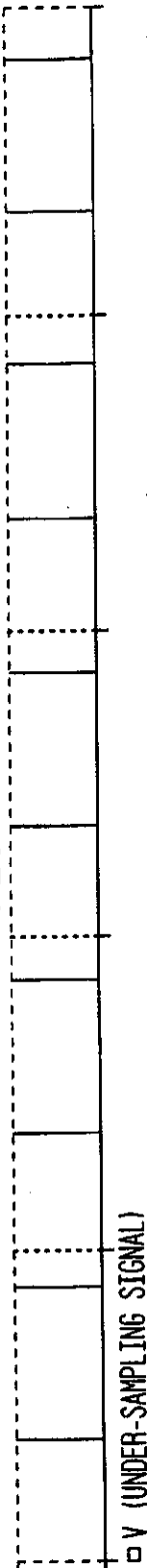


FIG. 34D

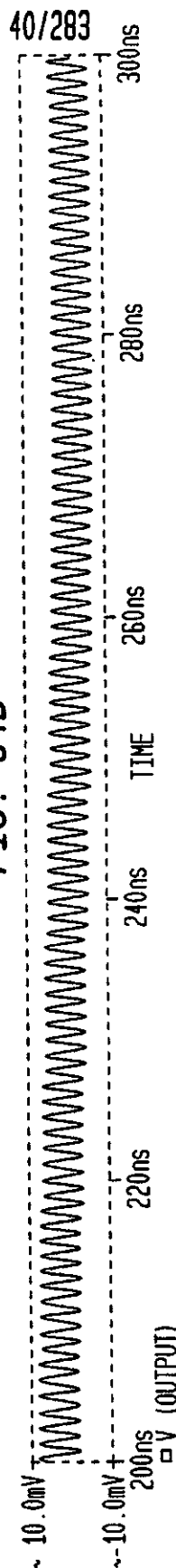


FIG. 34E

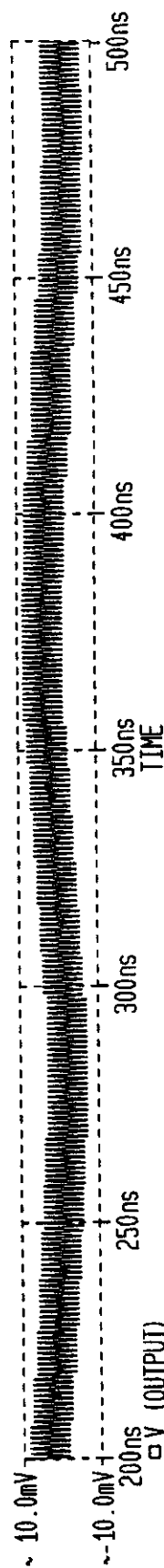
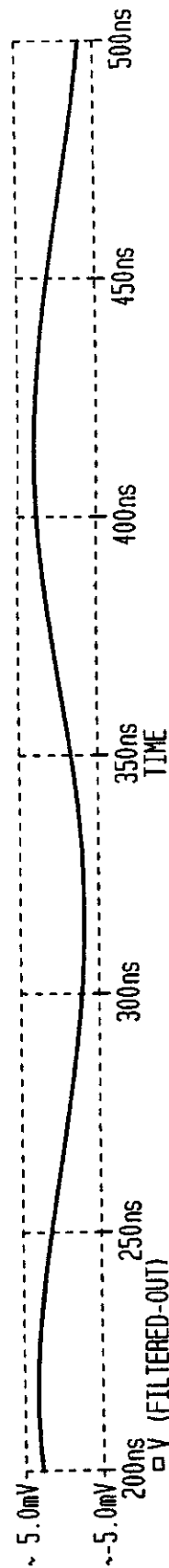


FIG. 34F



41/283

FIG. 35A

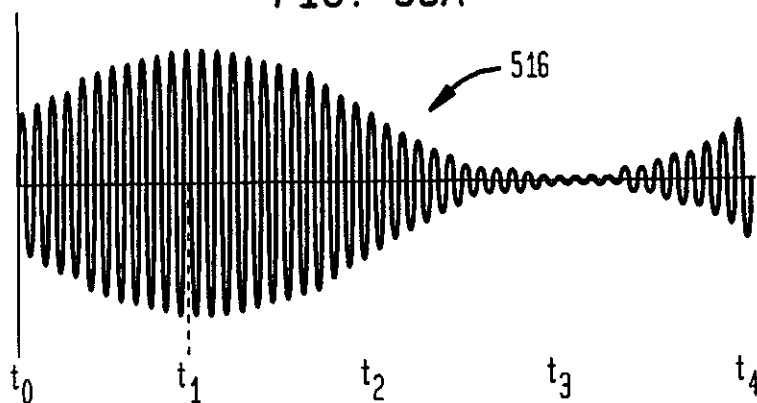


FIG. 35B

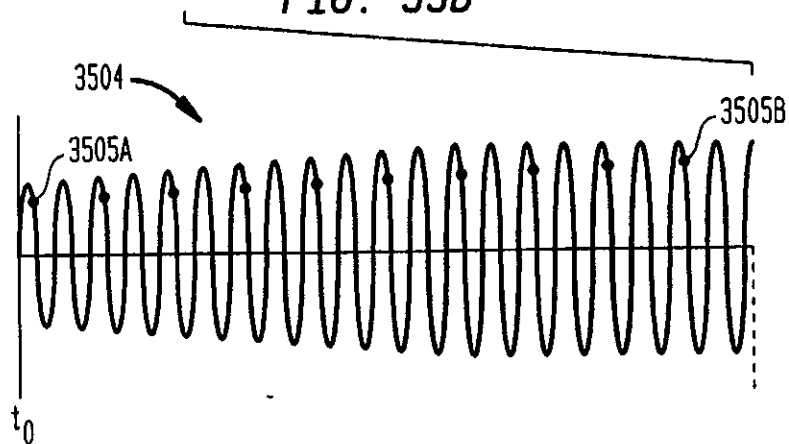


FIG. 35C



FIG. 35D

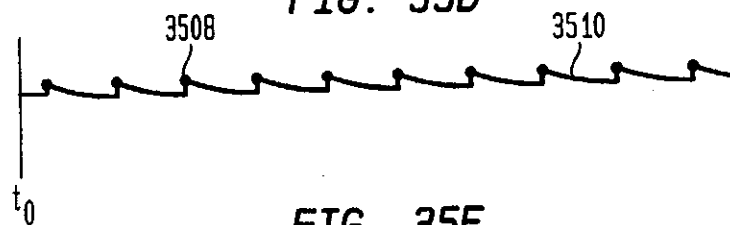
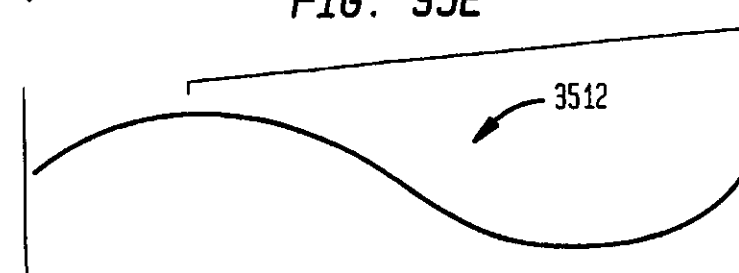


FIG. 35E



42/283

FIG. 36A

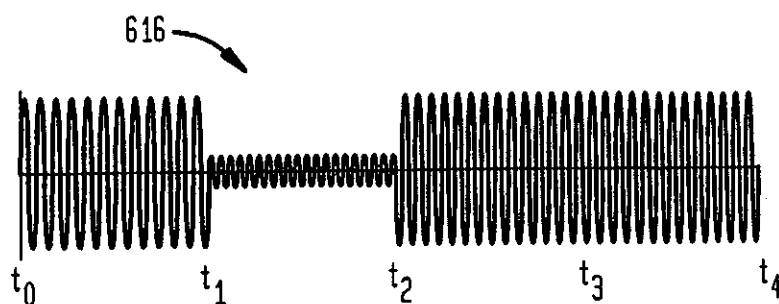


FIG. 36B

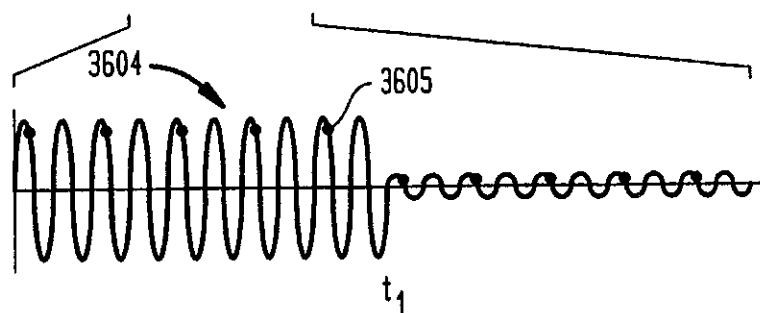


FIG. 36C

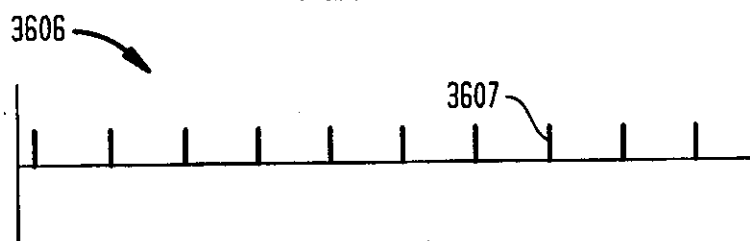


FIG. 36D

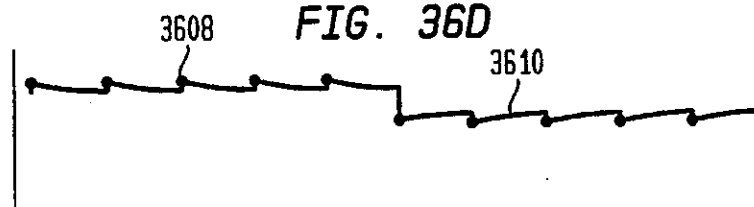
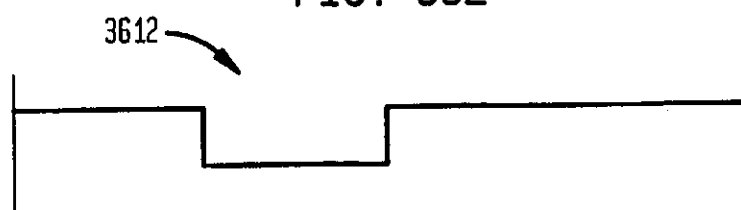


FIG. 36E



43/283

FIG. 37A

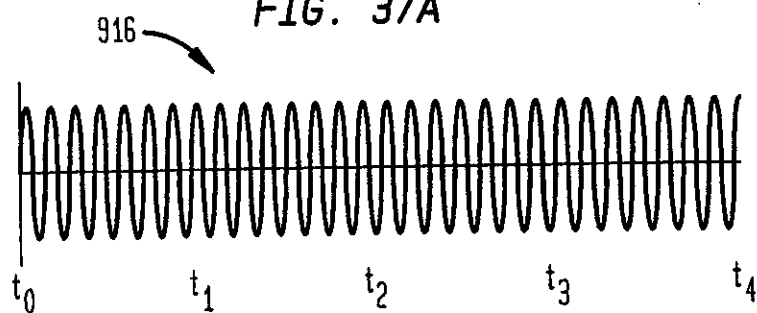


FIG. 37B

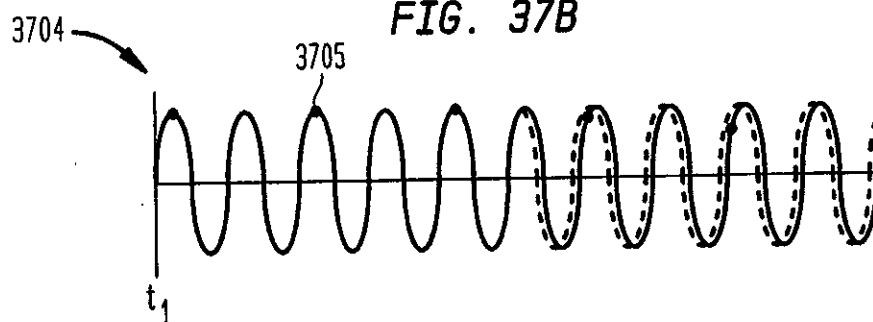


FIG. 37C

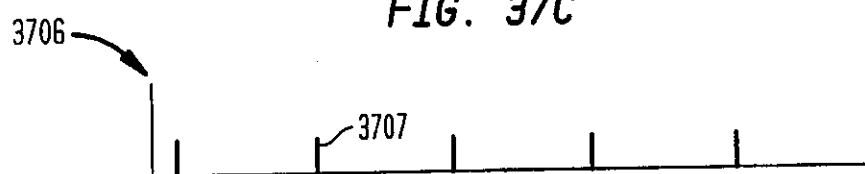


FIG. 37D

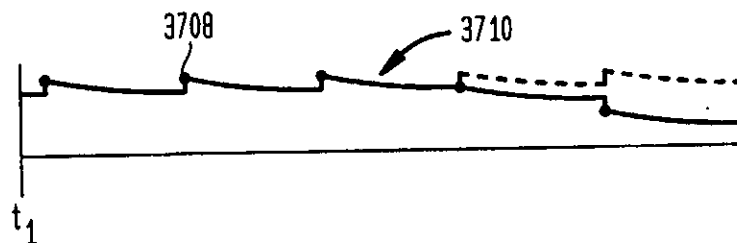
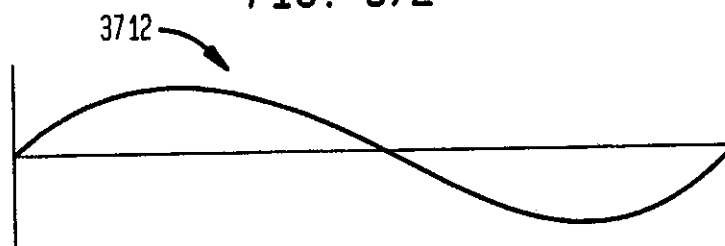
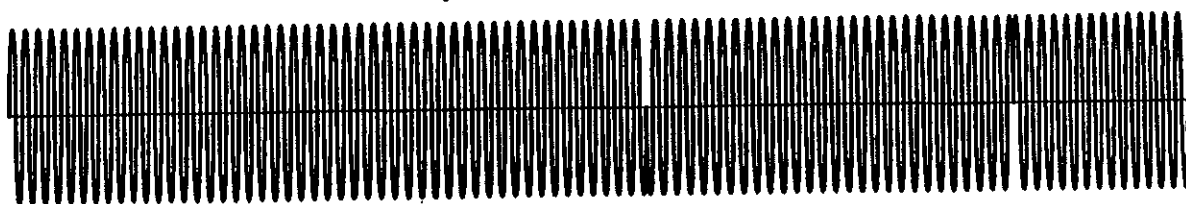
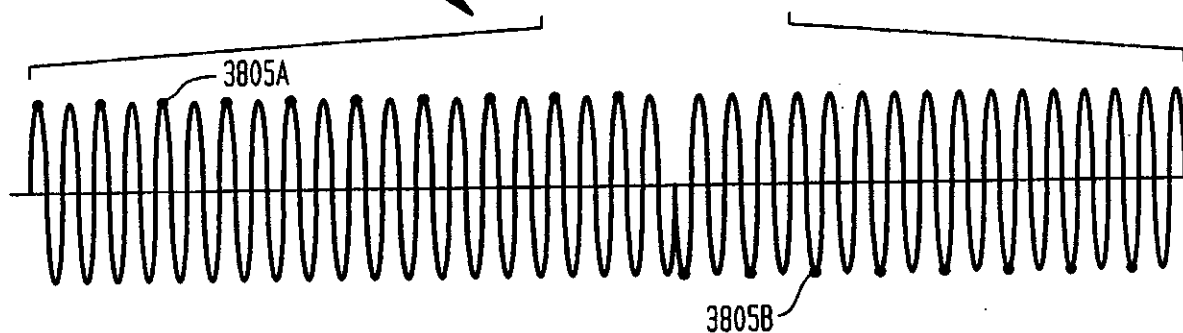
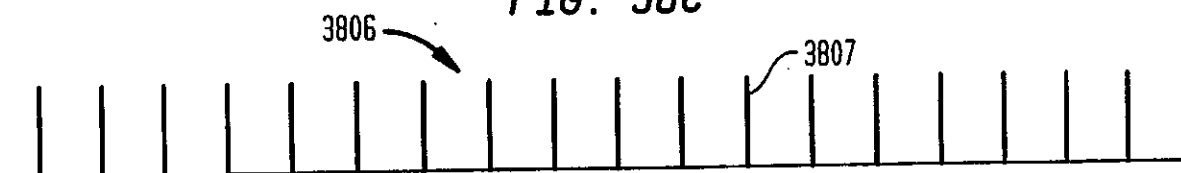
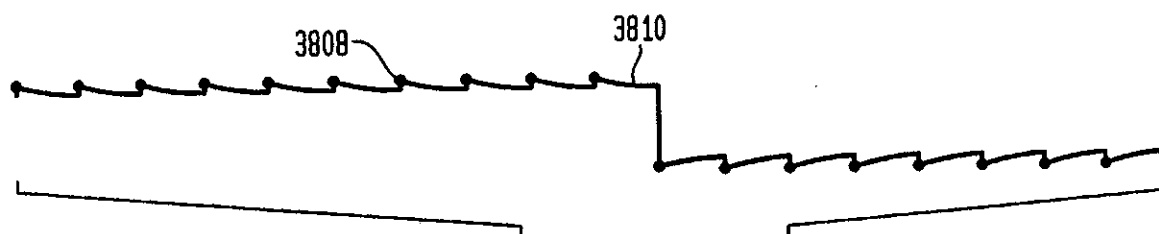


FIG. 37E



44/283

1016 *FIG. 38A*3804 *FIG. 38B**FIG. 38C**FIG. 38D**FIG. 38E*

3812



45/283

FIG. 39A

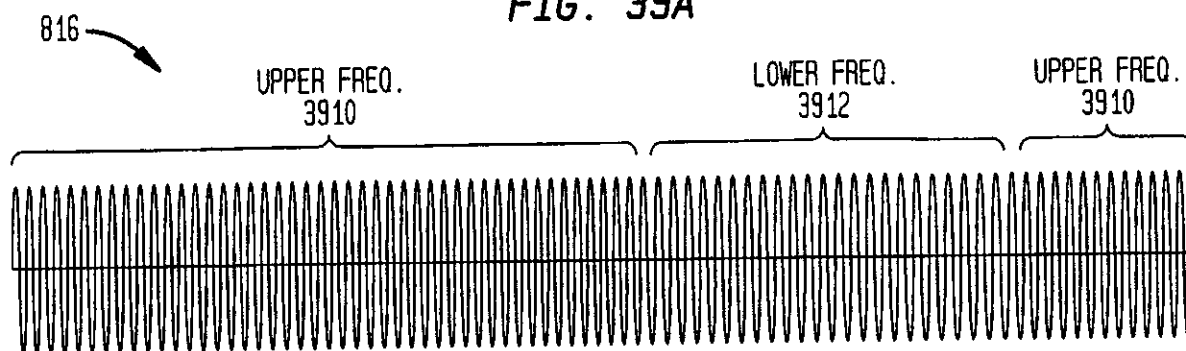


FIG. 39B

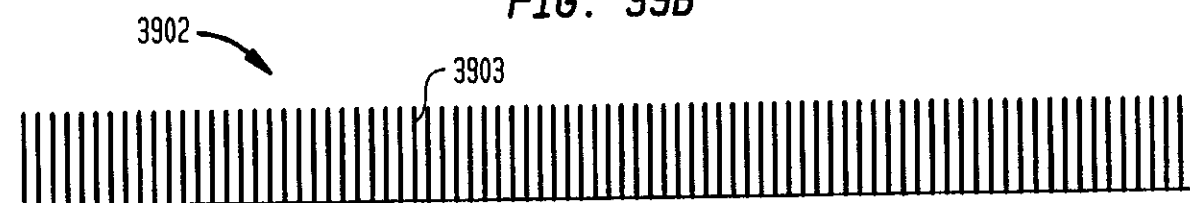
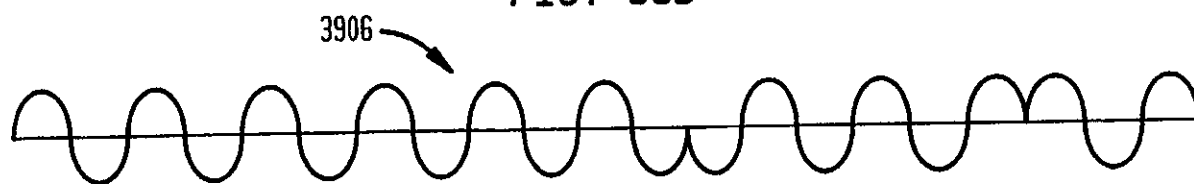


FIG. 39C



FIG. 39D



46/283

FIG. 40A

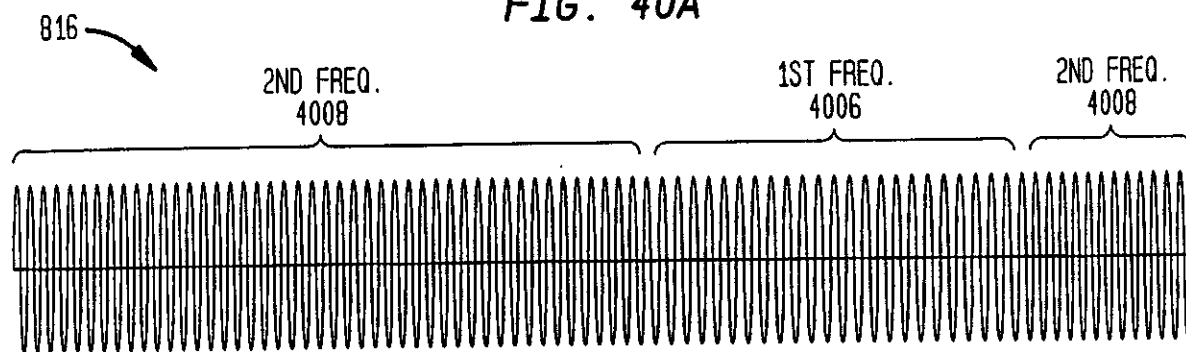


FIG. 40B

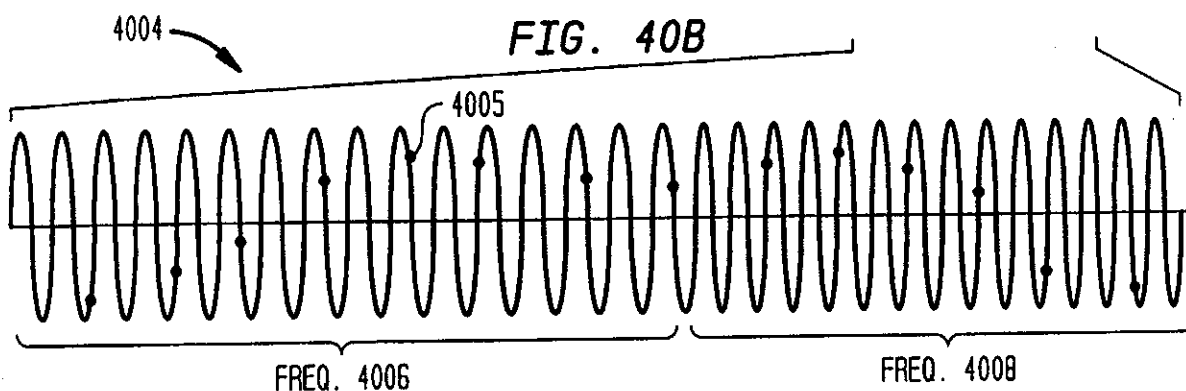


FIG. 40C

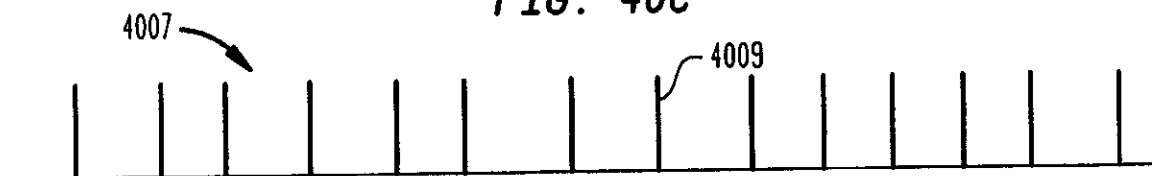


FIG. 40D

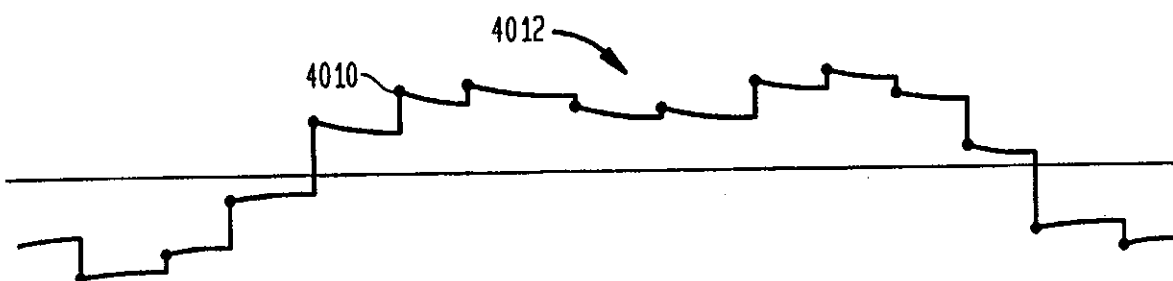
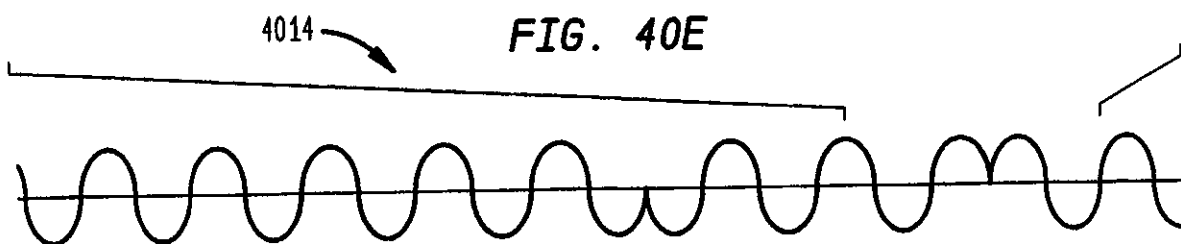
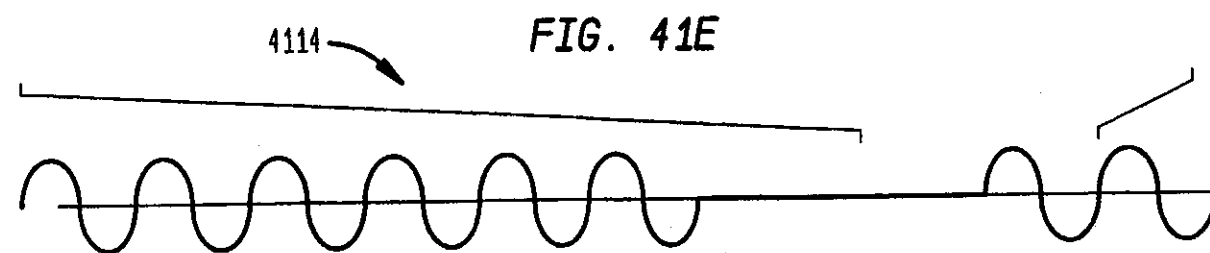
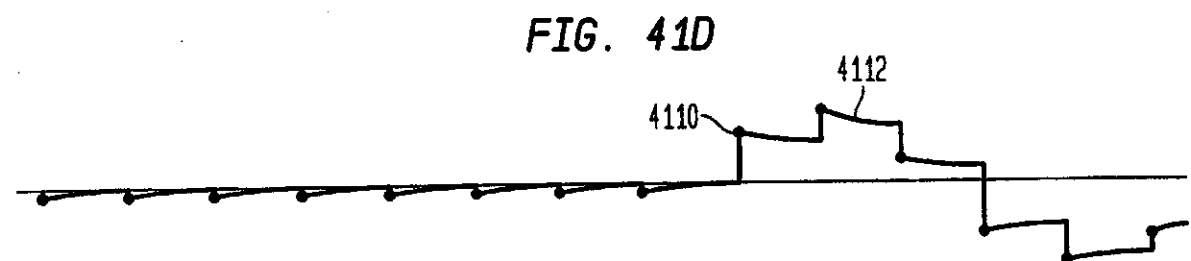
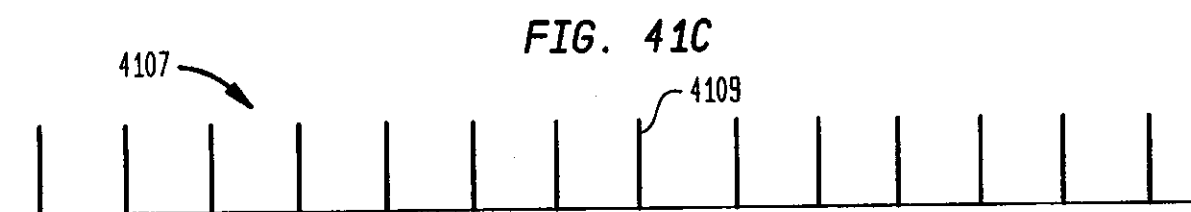
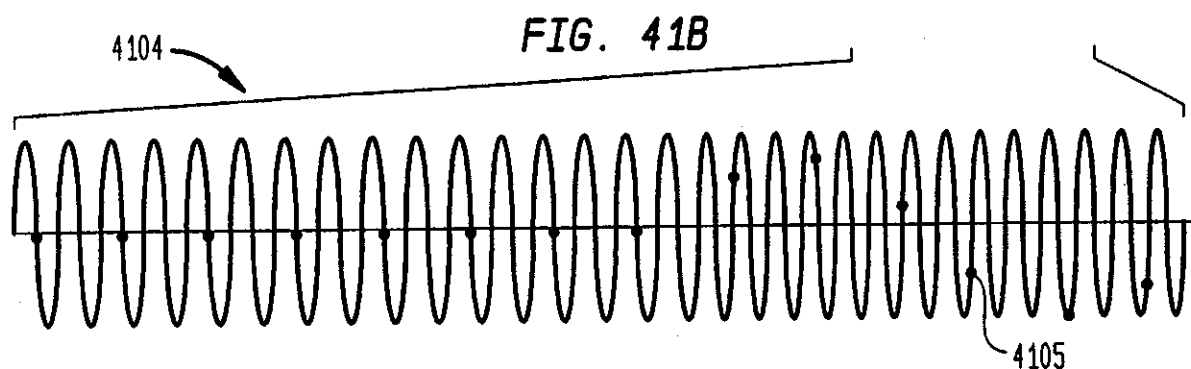
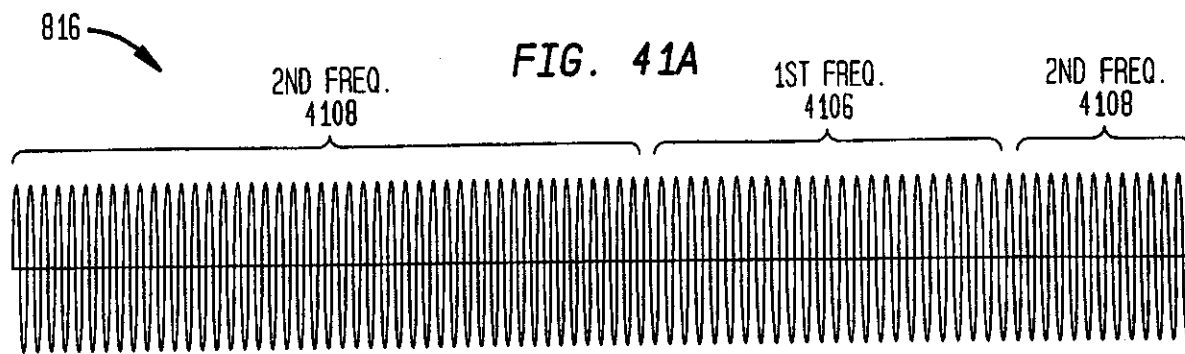


FIG. 40E



47/283



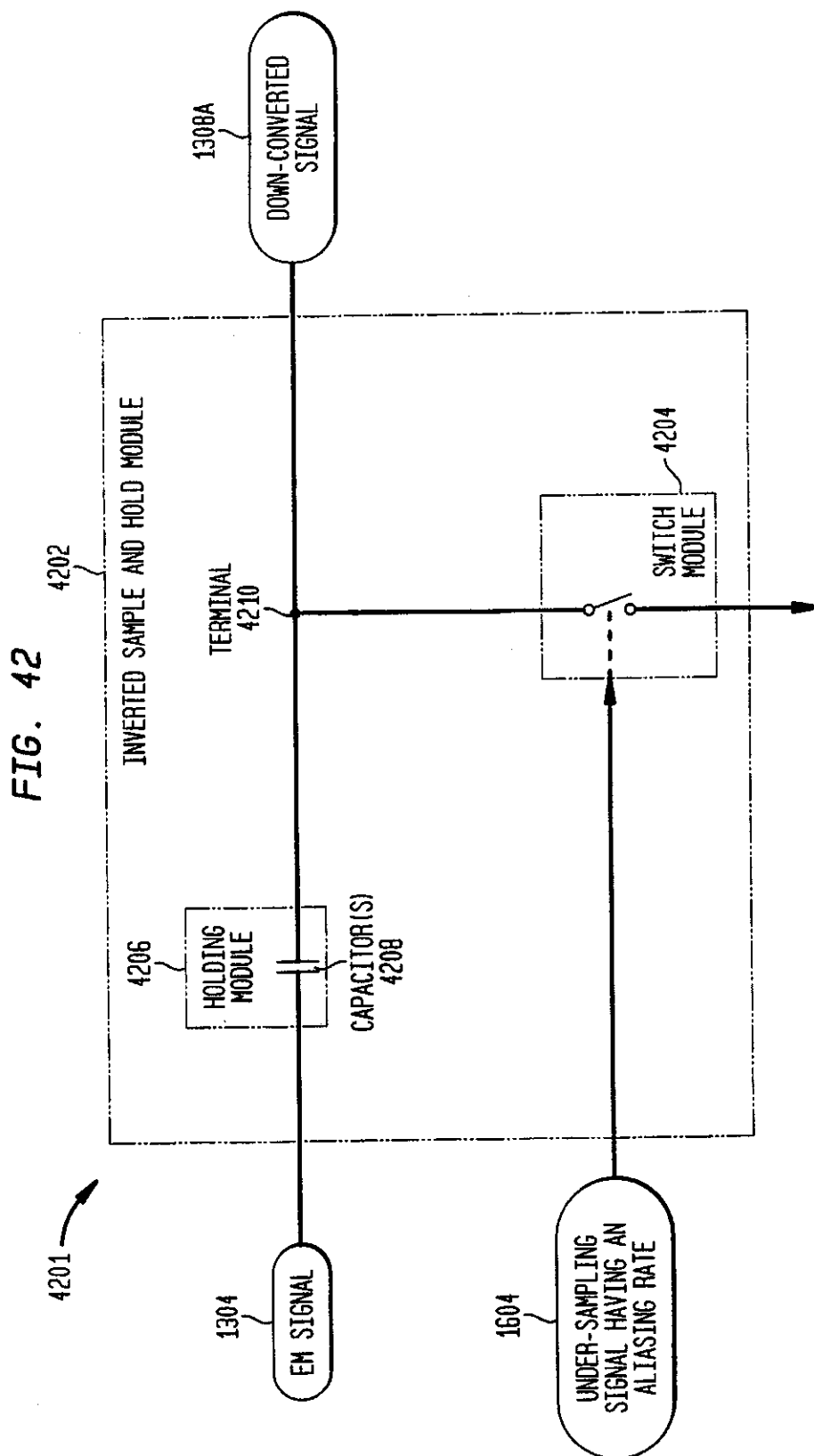
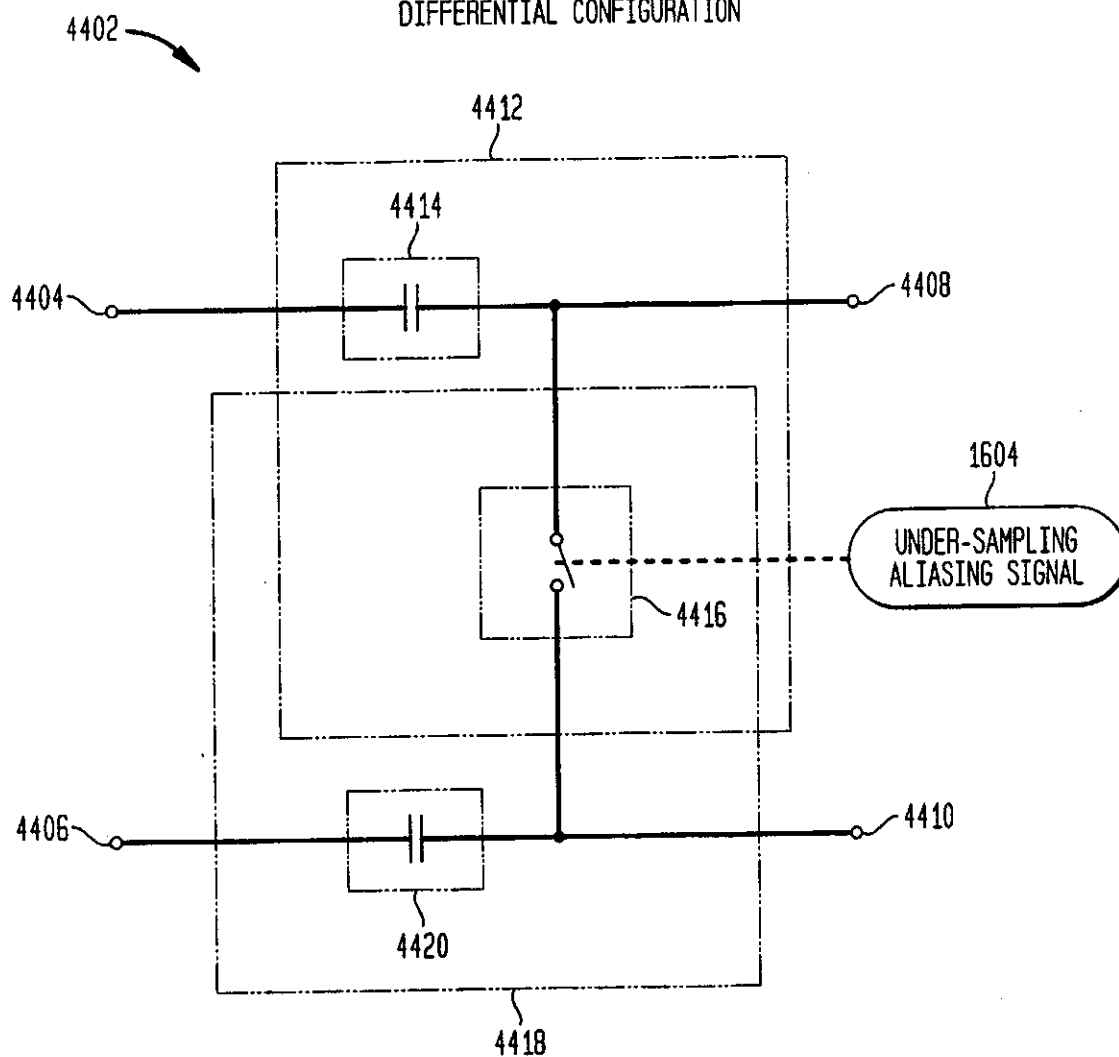


FIG. 43

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin(1/2 \cdot T) \cdot \cos(t - 1/2 \cdot T)$$

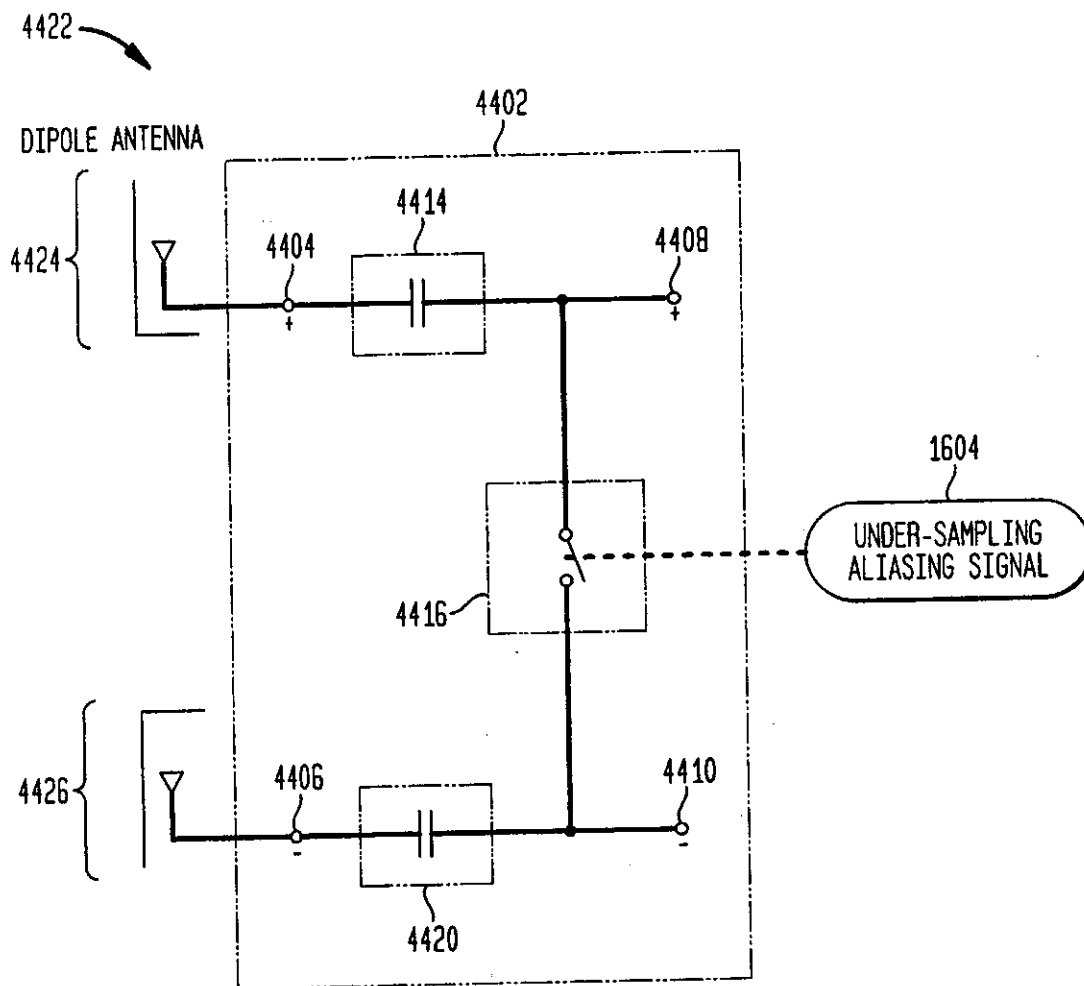
49/283

FIG. 44A
DIFFERENTIAL CONFIGURATION



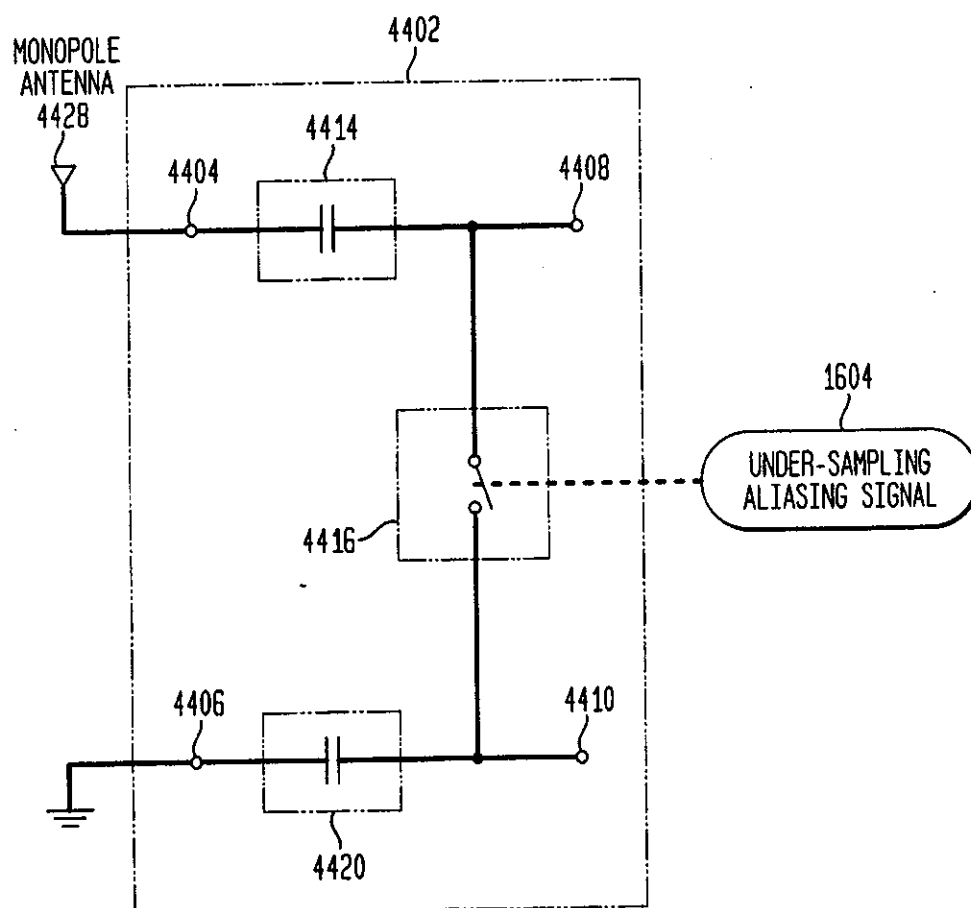
50/283

FIG. 44B
DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT



51/283

FIG. 44C
SINGLE INPUT TO DIFFERENTIAL OUTPUT



52/283

FIG. 44D
DIFFERENTIAL INPUT TO SINGLE OUTPUT

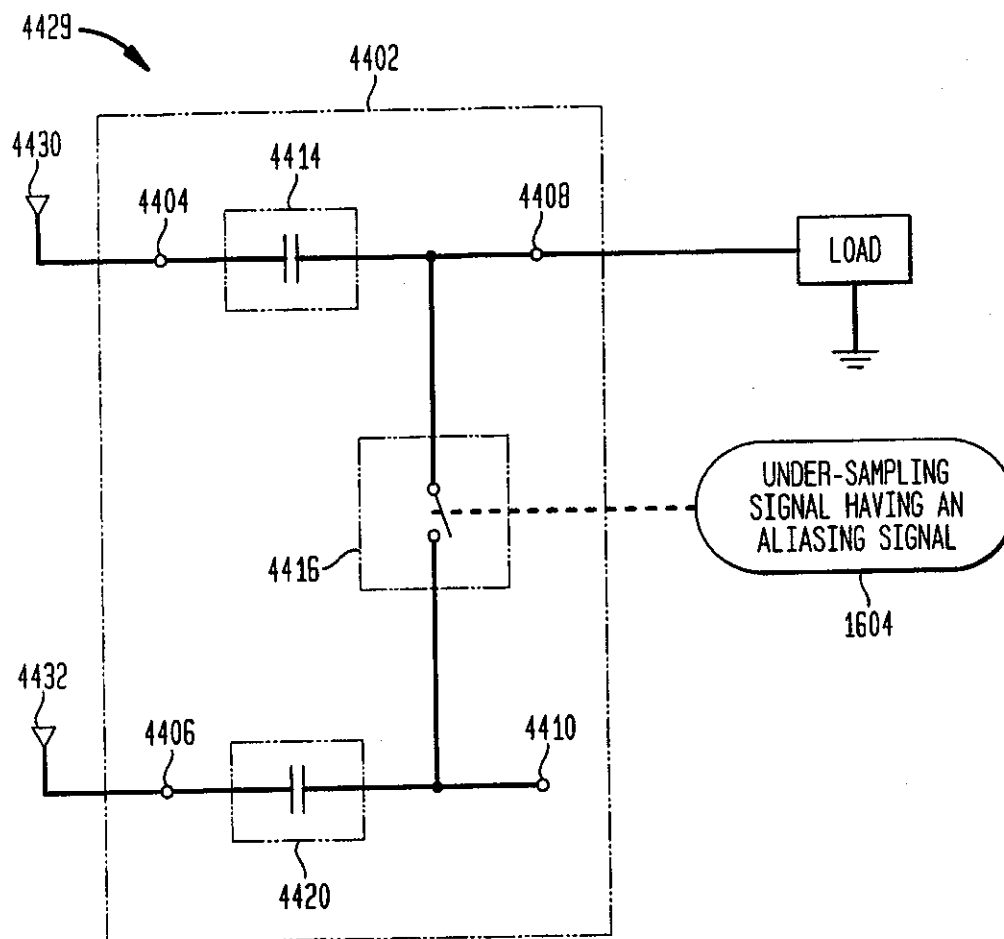
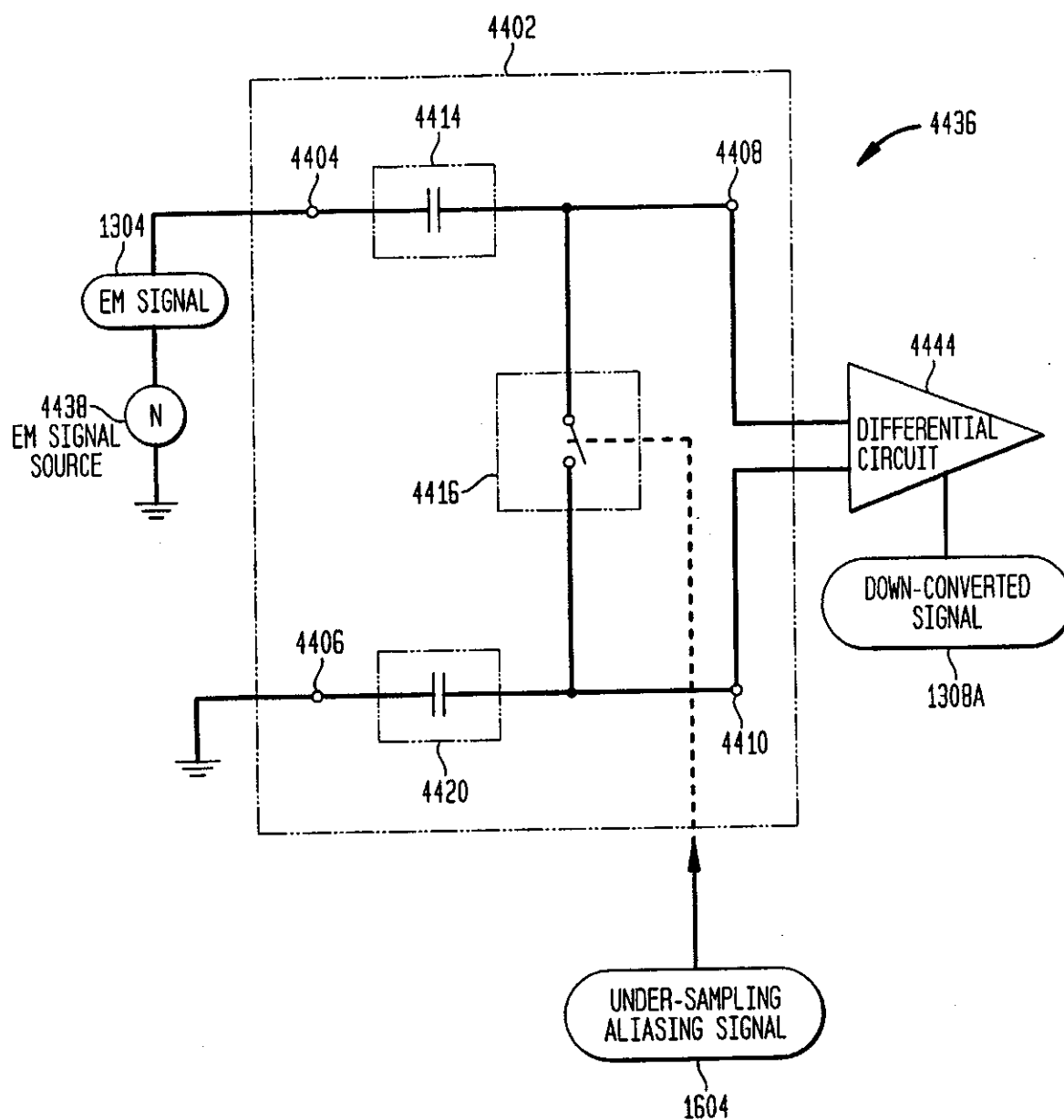
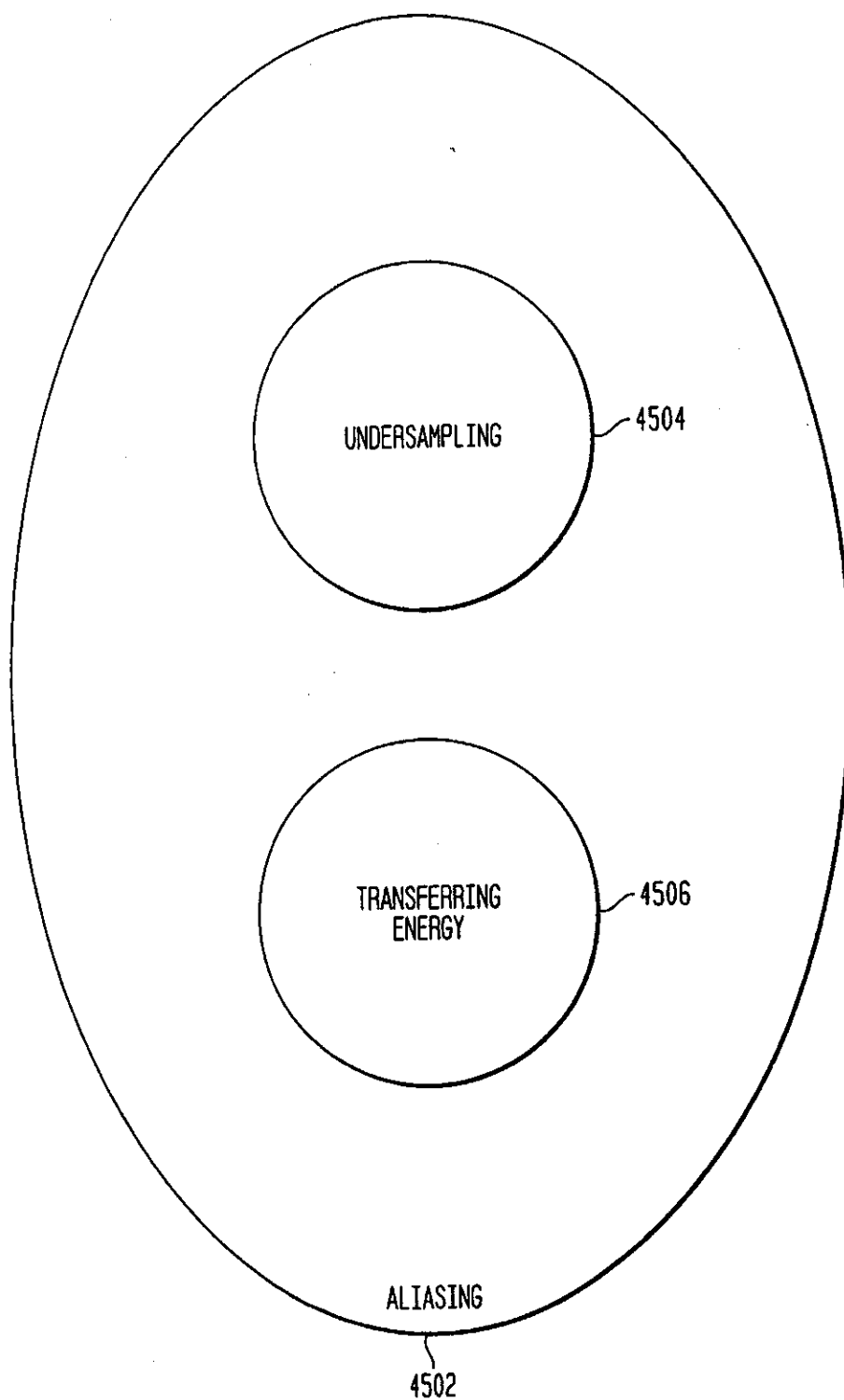


FIG. 44E
EXAMPLE INPUT/OUTPUT CIRCUITRY



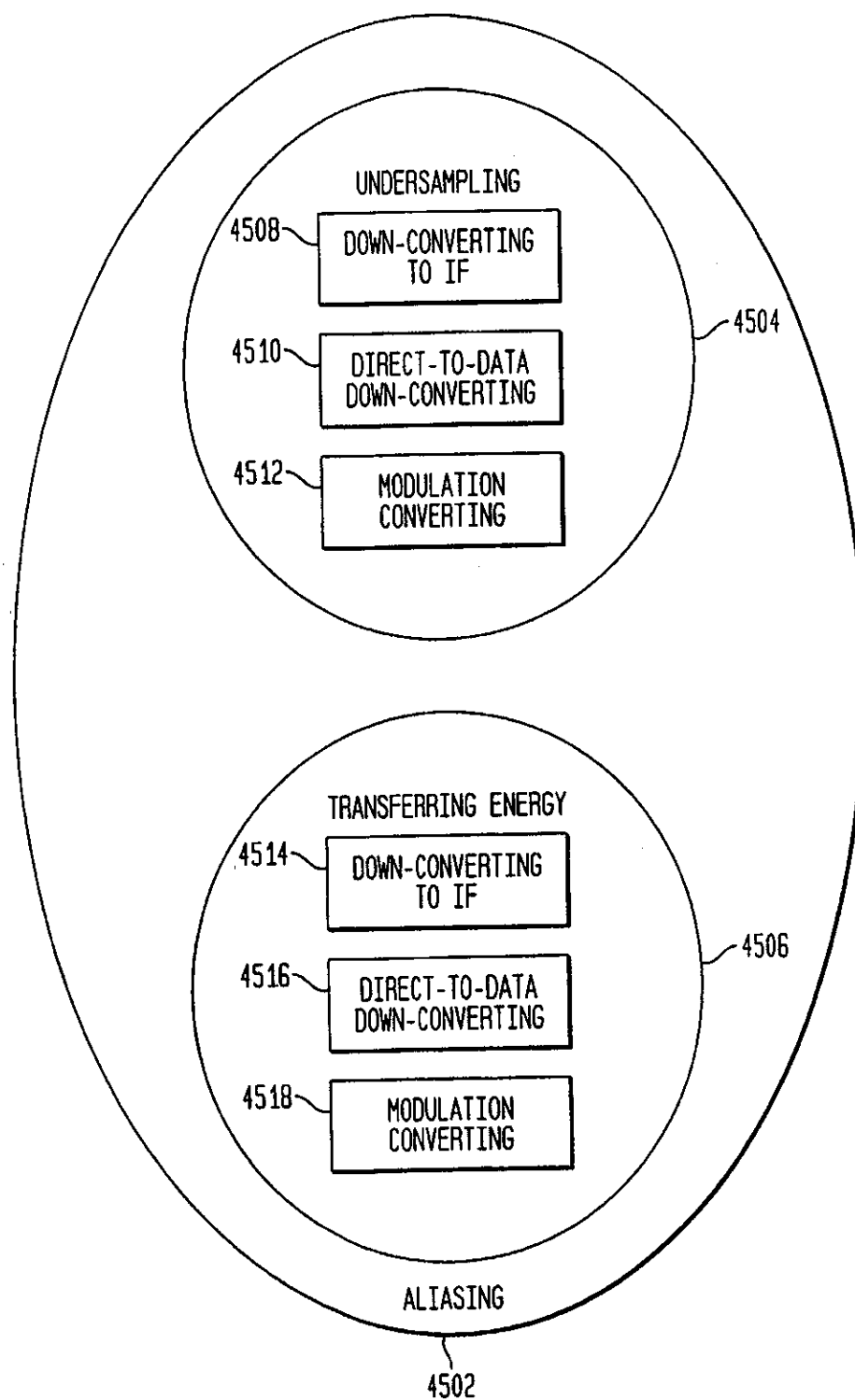
54/283

FIG. 45A



55/283

FIG. 45B



56/283

FIG. 46A

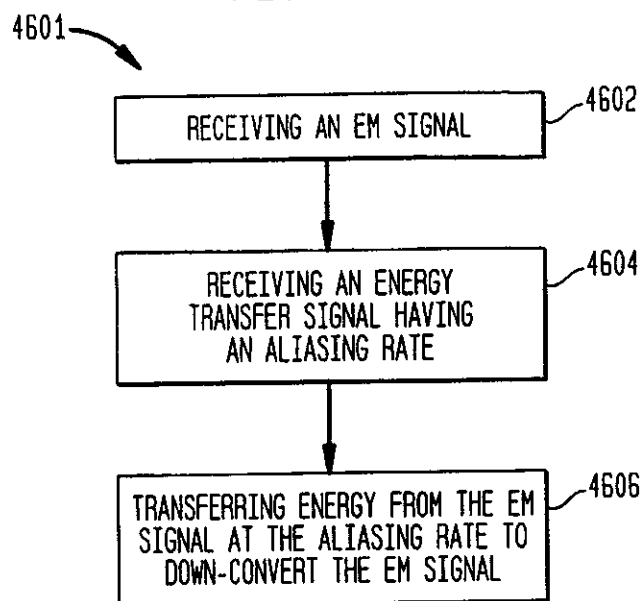
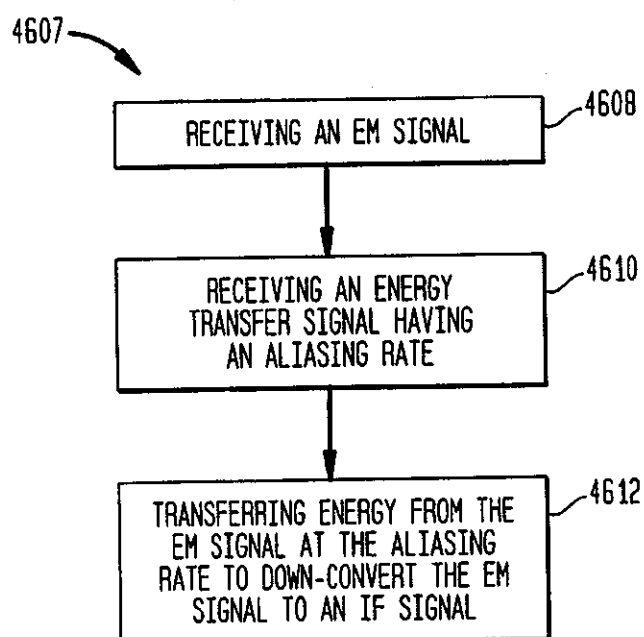


FIG. 46B



57/283

FIG. 46C

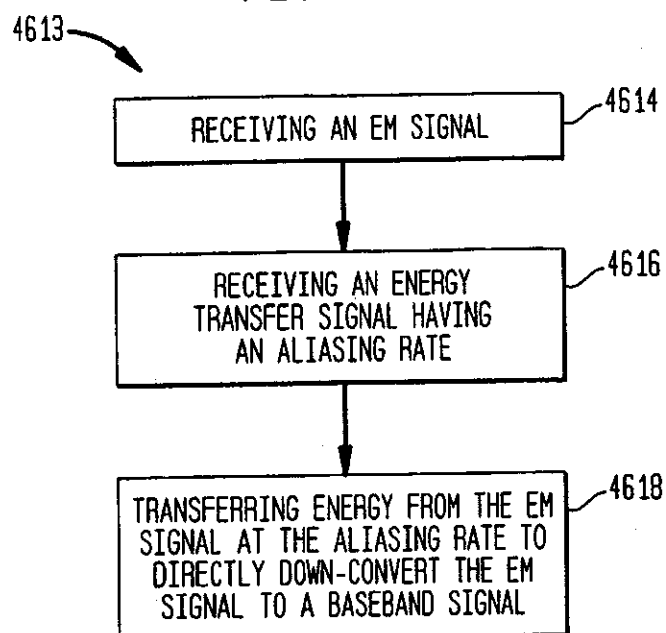
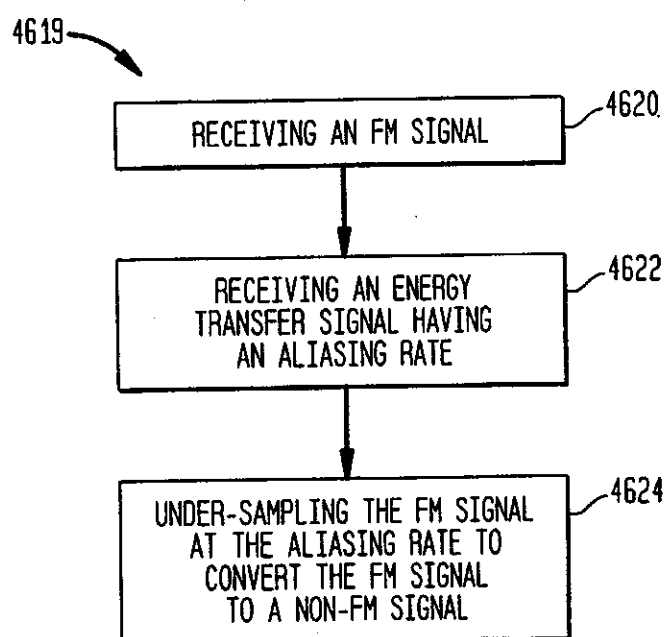
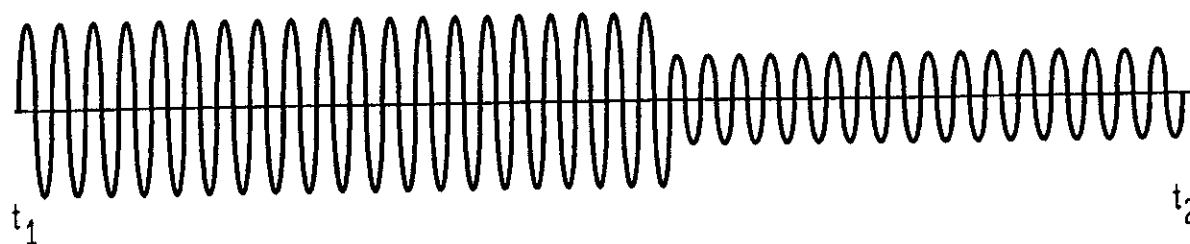


FIG. 46D



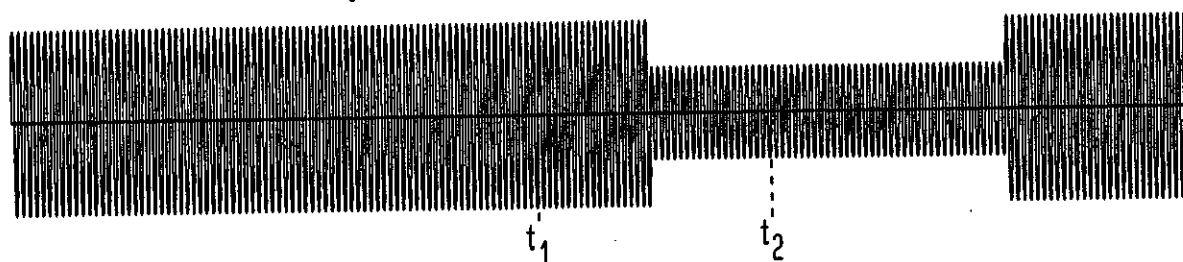
58/283

FIG. 47E



616

FIG. 47A



4702

FIG. 47B

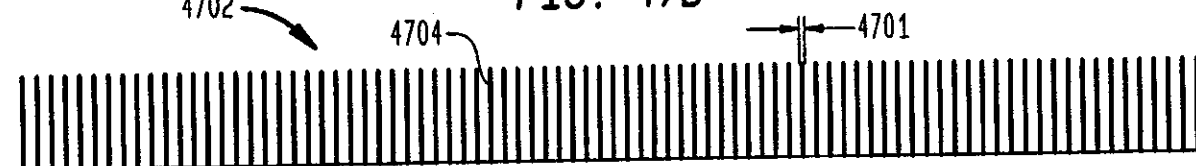


FIG. 47C

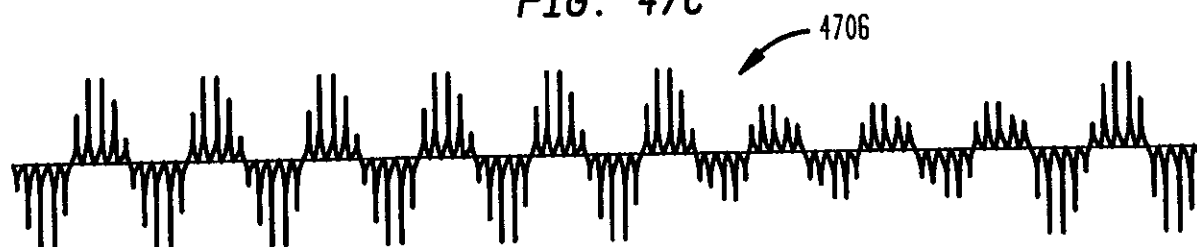
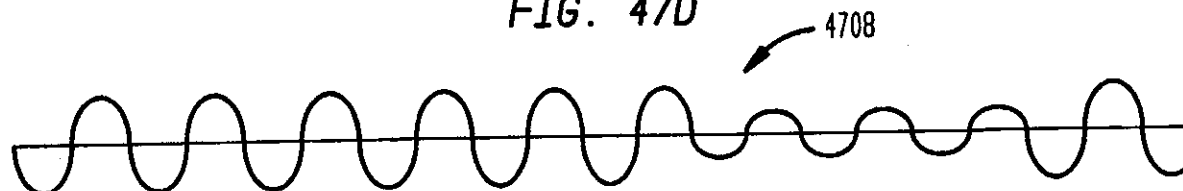
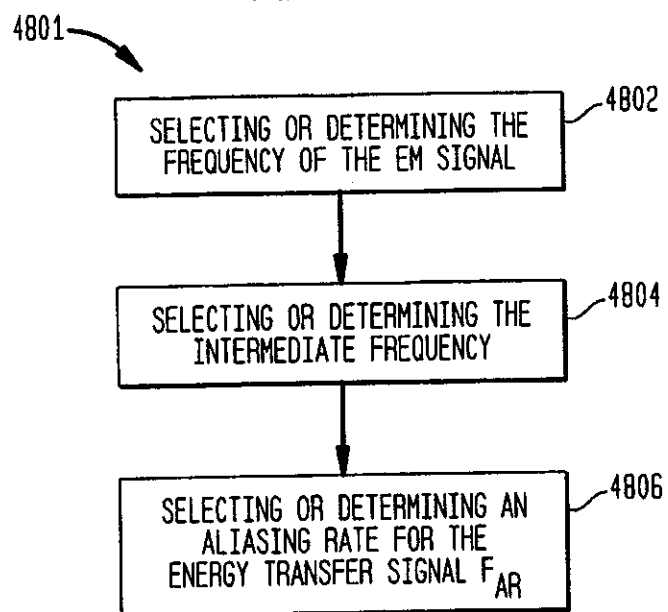


FIG. 47D

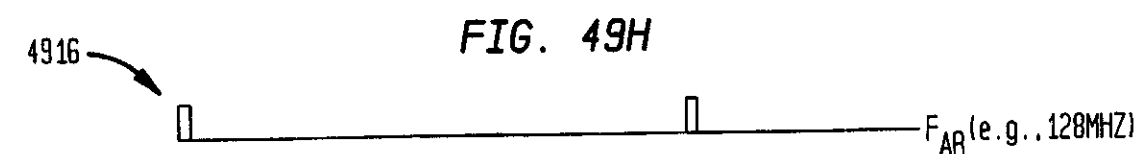
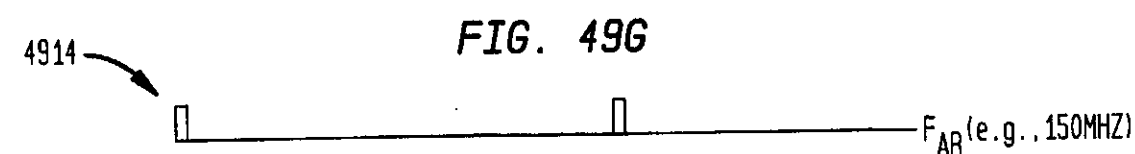
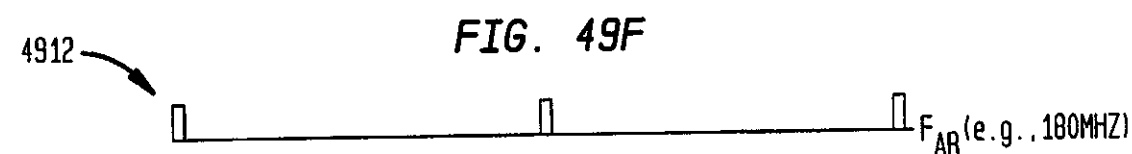
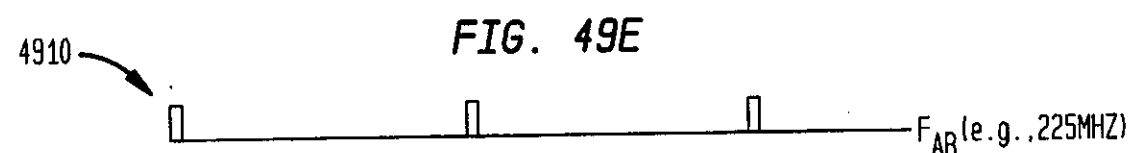
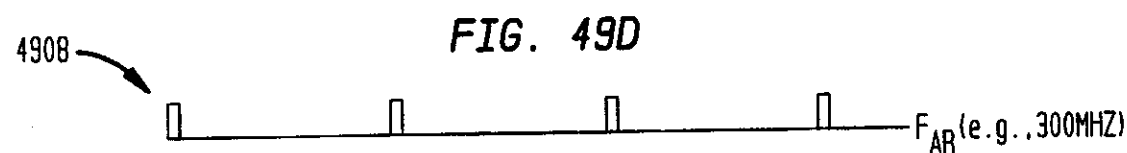
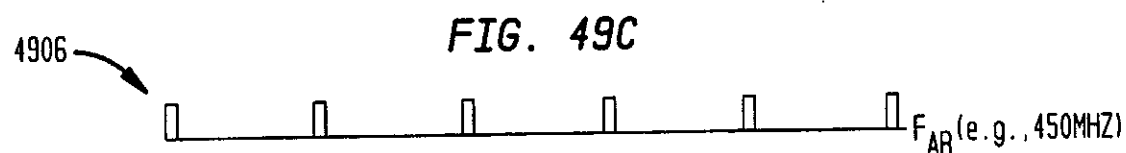
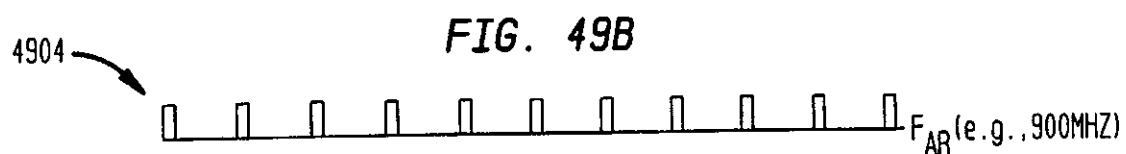
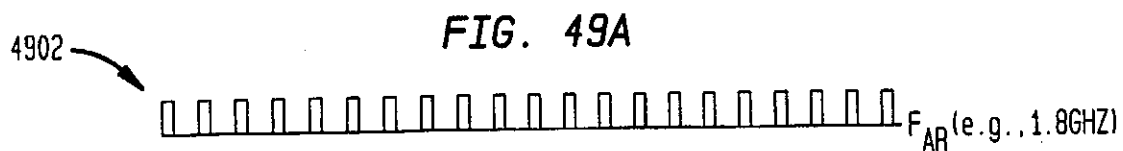


59/283

FIG. 48



60/283



61/283

FIG. 50A

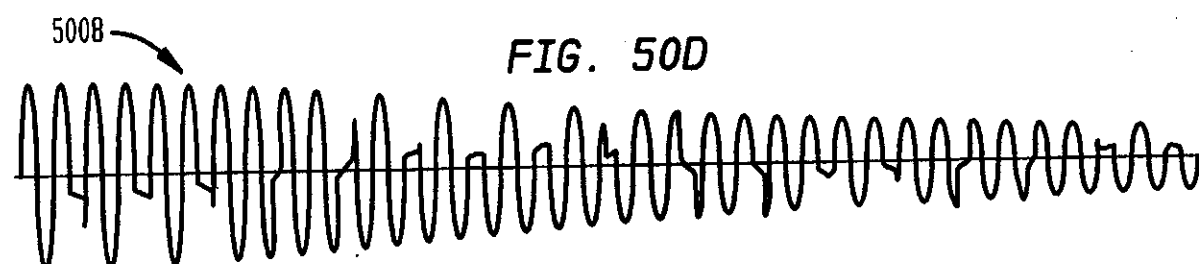
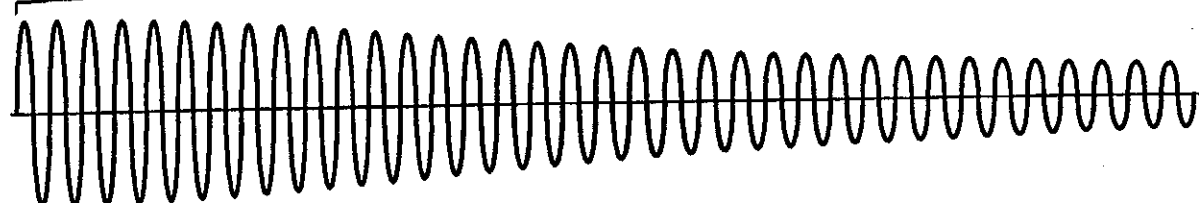
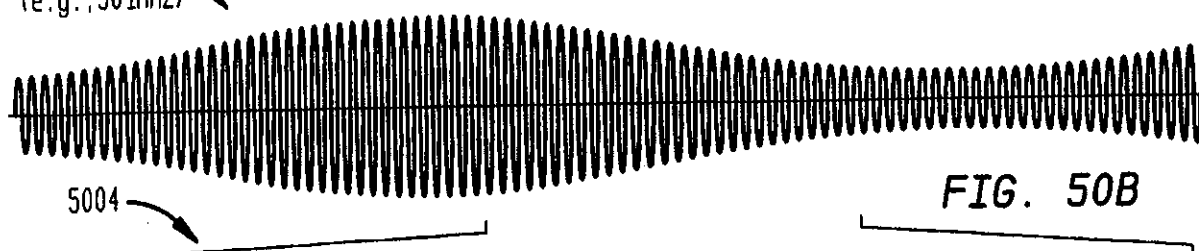
516
(e.g., 901MHz)

FIG. 50D

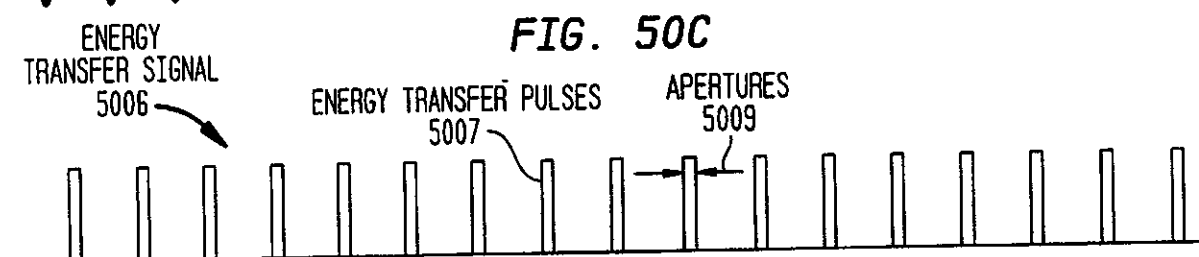


FIG. 50C

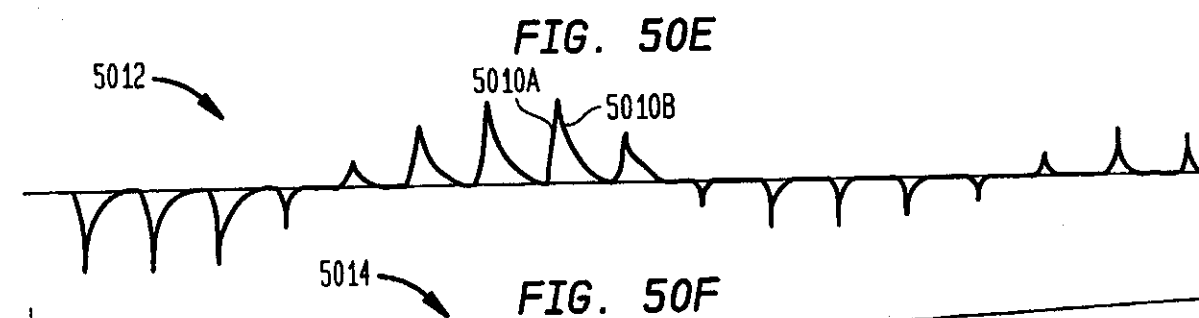


FIG. 50E

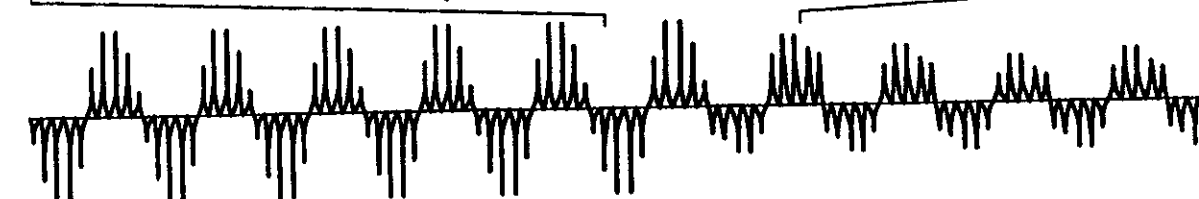
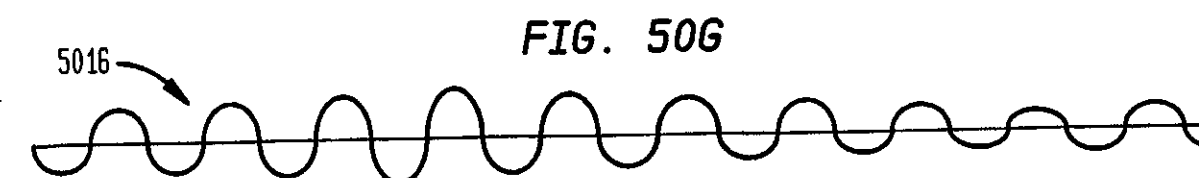


FIG. 50F



62/283

FIG. 51A

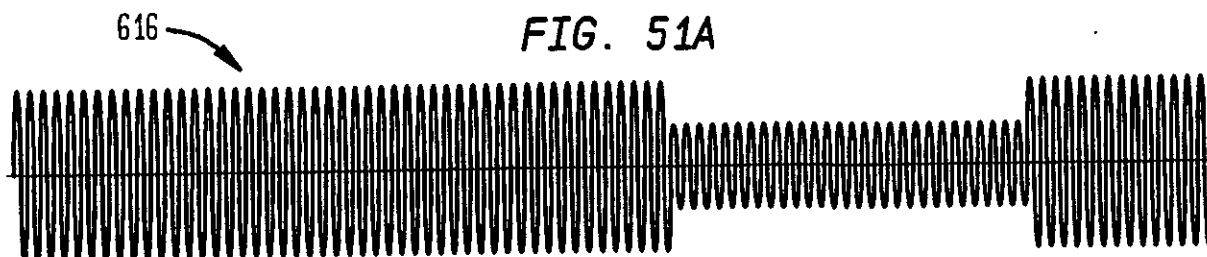


FIG. 51B

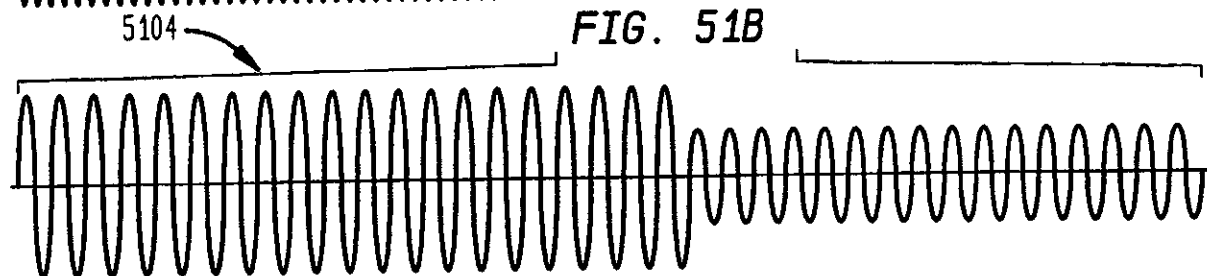


FIG. 51D

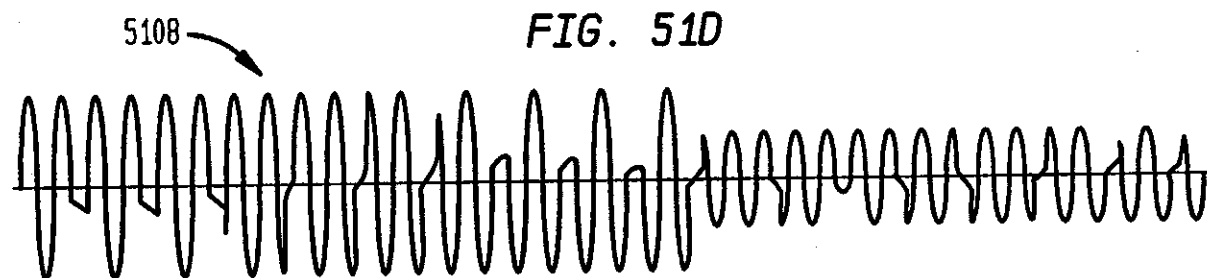


FIG. 51C

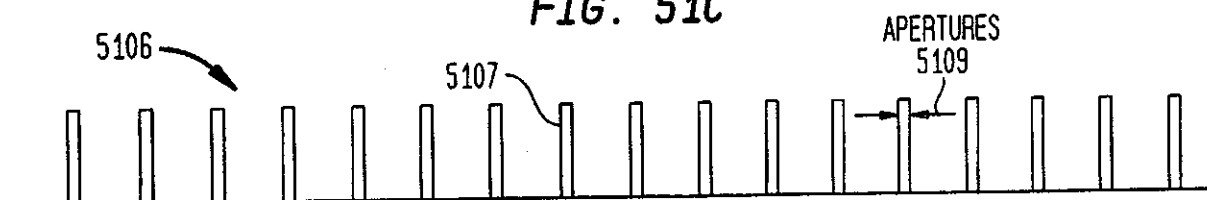


FIG. 51E

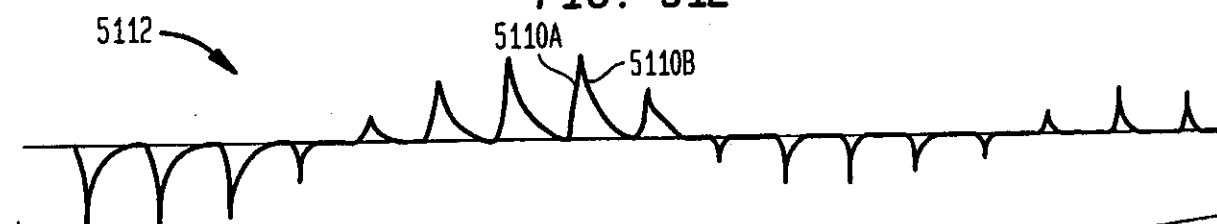


FIG. 51F

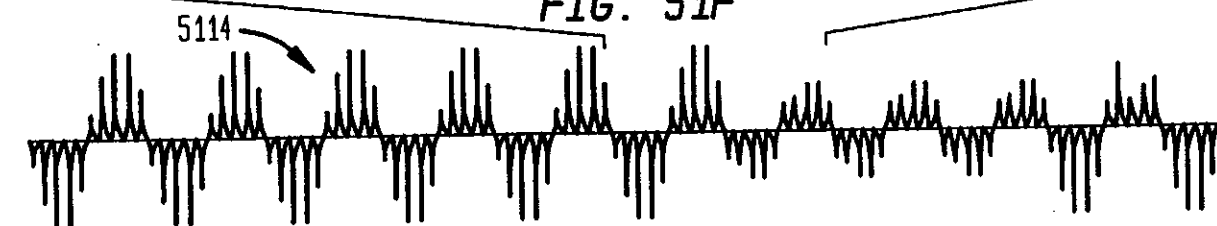
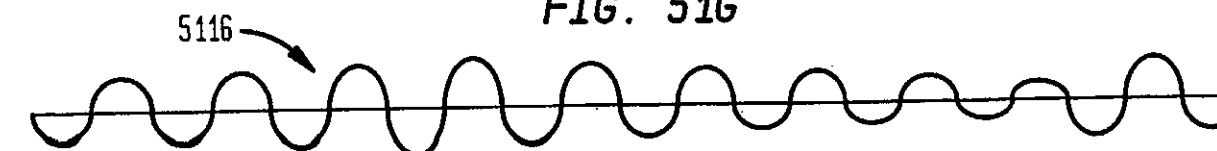
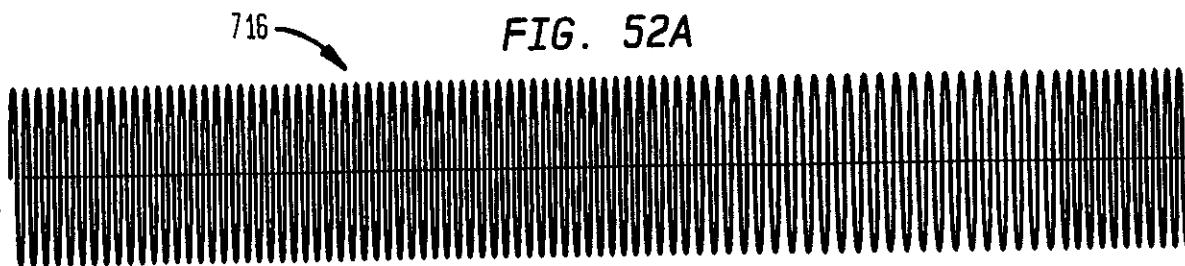


FIG. 51G



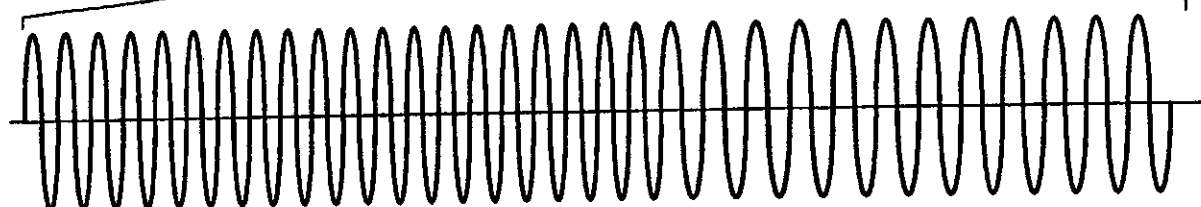
63/283

FIG. 52A



5204

FIG. 52B



5208

FIG. 52D

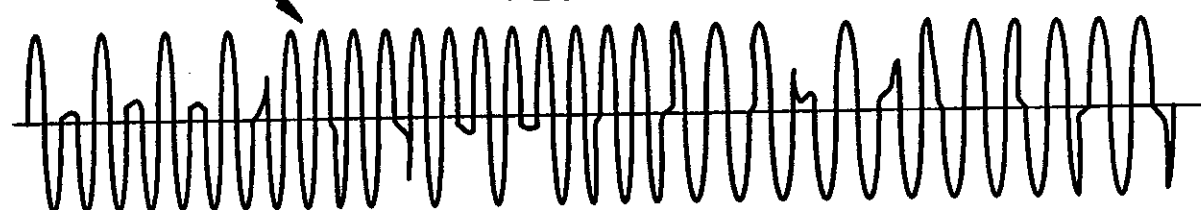


FIG. 52C

5206

5207

APERTURES
5209

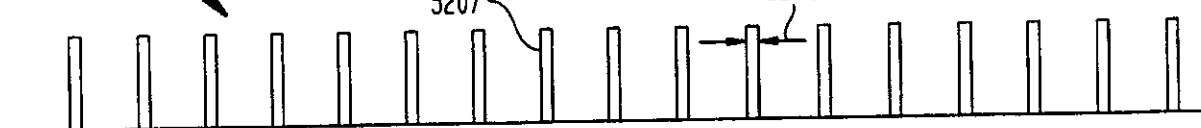


FIG. 52E

5212

5210A

5210B

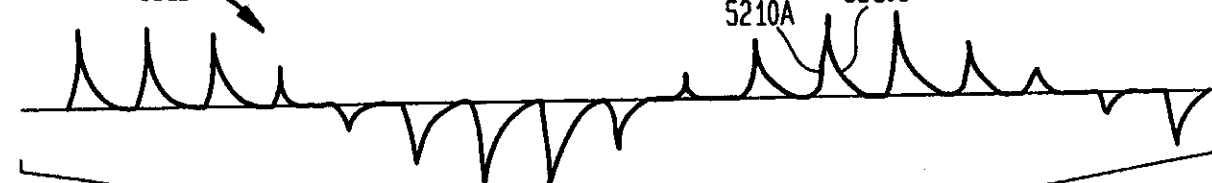


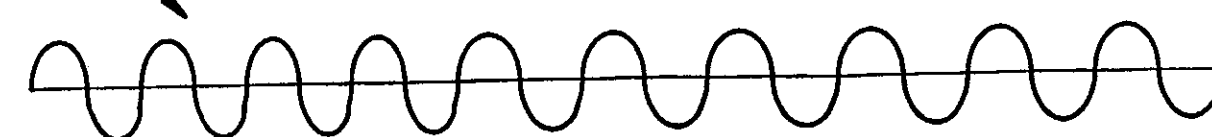
FIG. 52F

5214



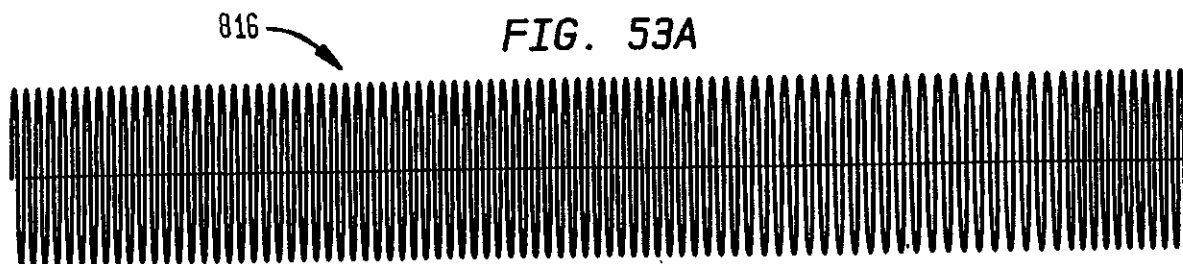
5216

FIG. 52G



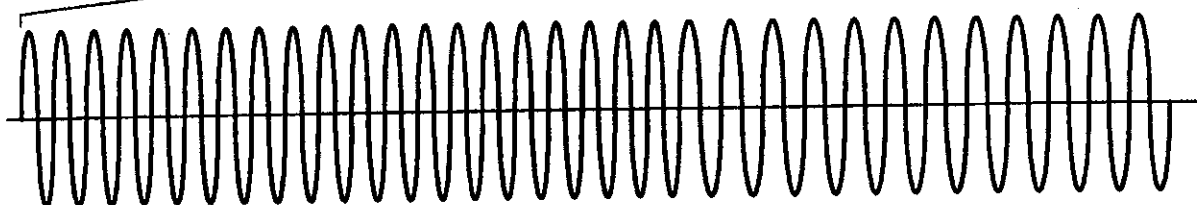
64/283

FIG. 53A



5304

FIG. 53B



5208

FIG. 53D

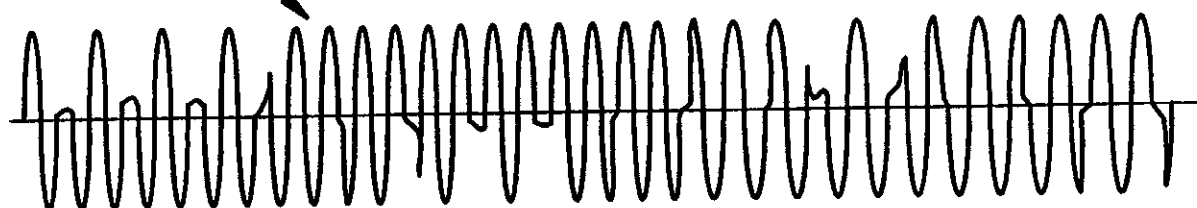


FIG. 53C

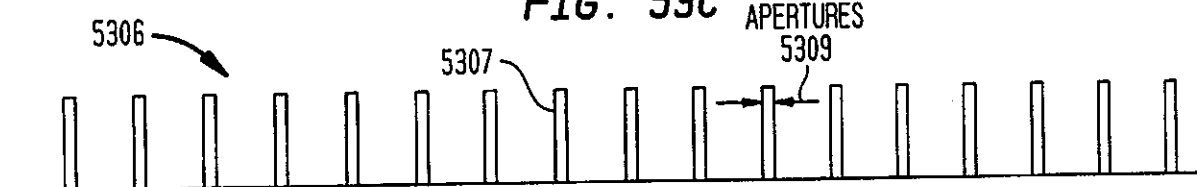


FIG. 53E

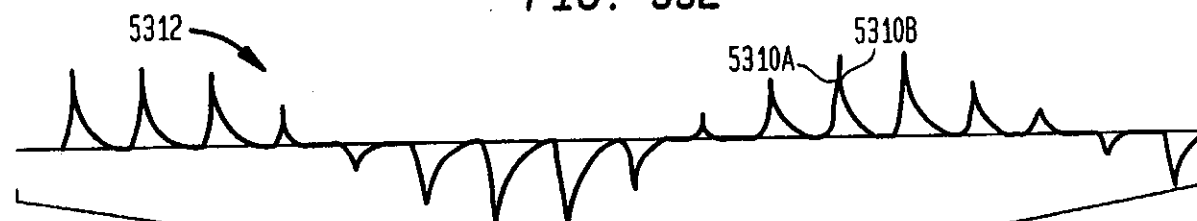


FIG. 53F

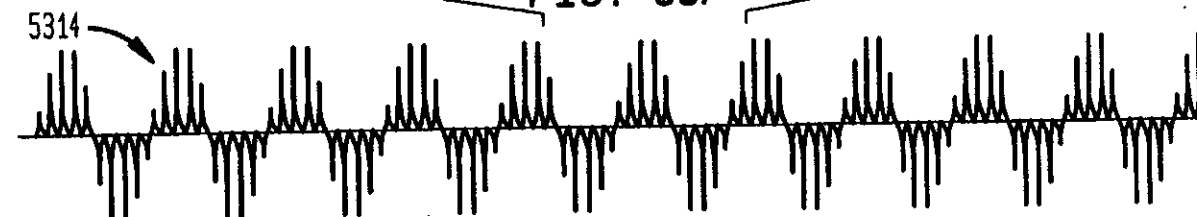
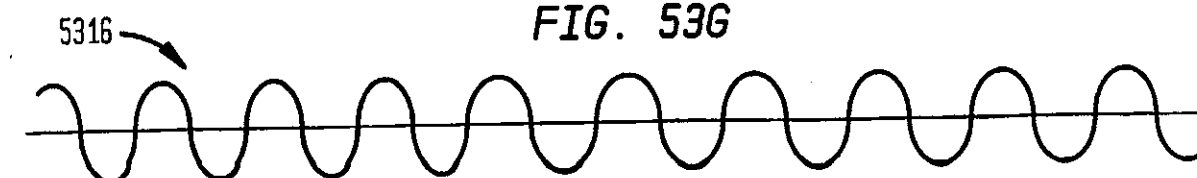


FIG. 53G



65/283

FIG. 54A

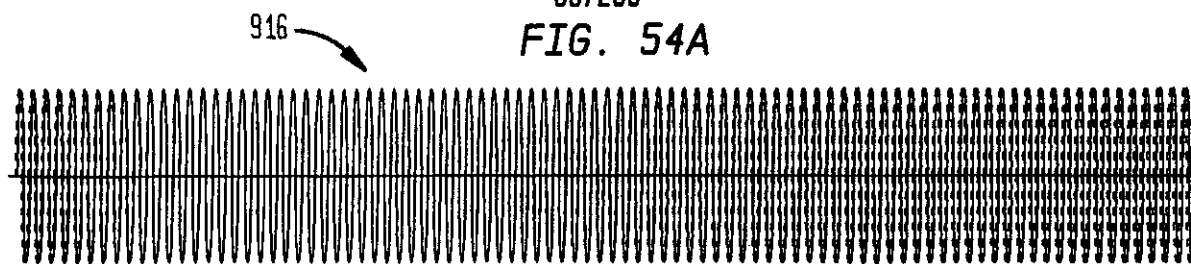


FIG. 54B

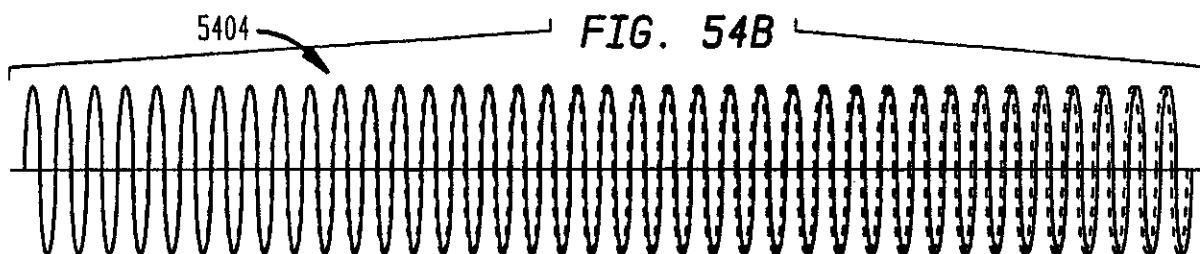


FIG. 54D

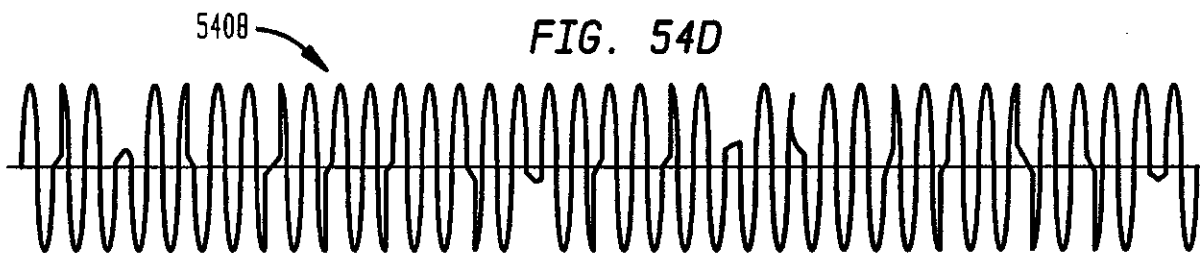


FIG. 54C

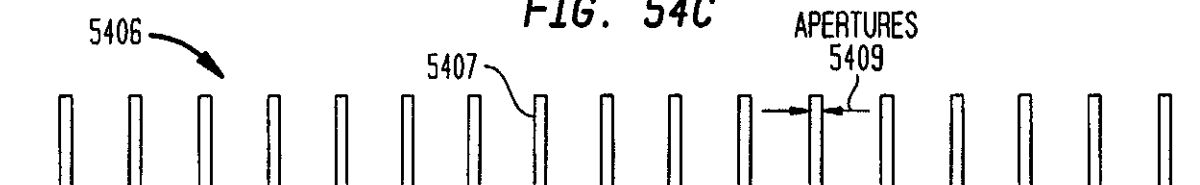


FIG. 54E

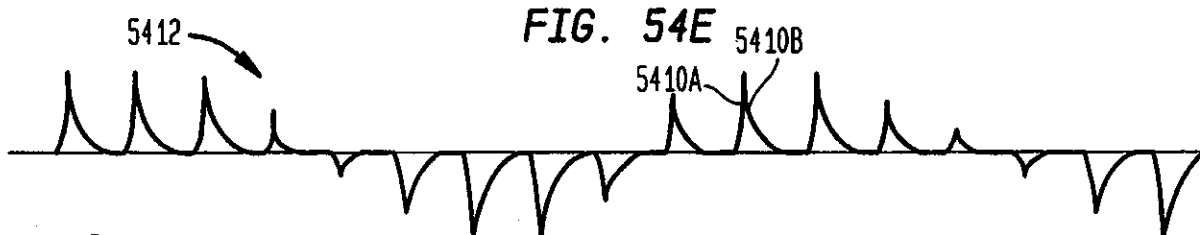


FIG. 54F

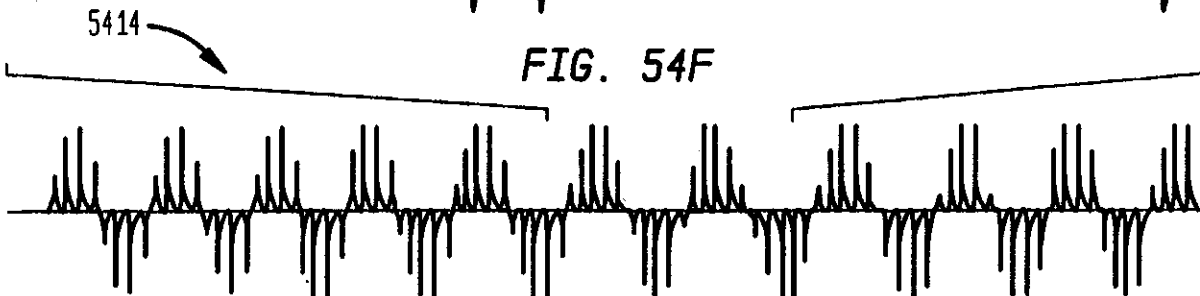
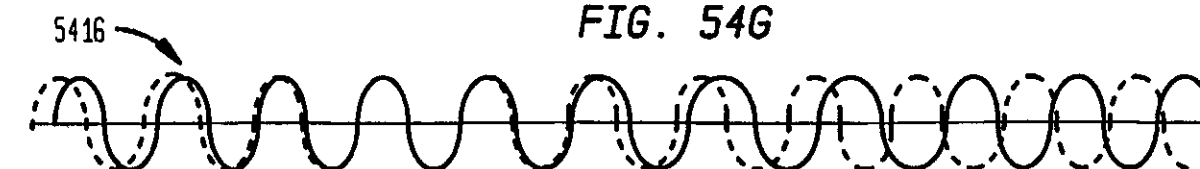


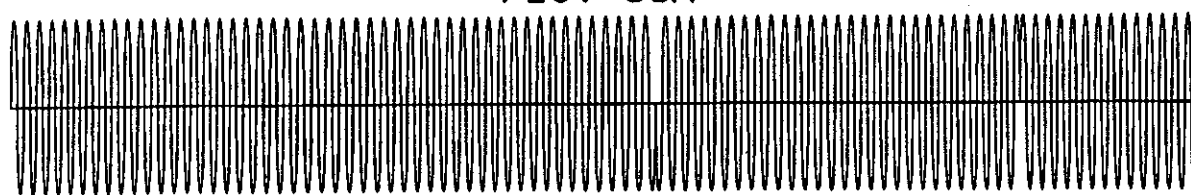
FIG. 54G



66/283

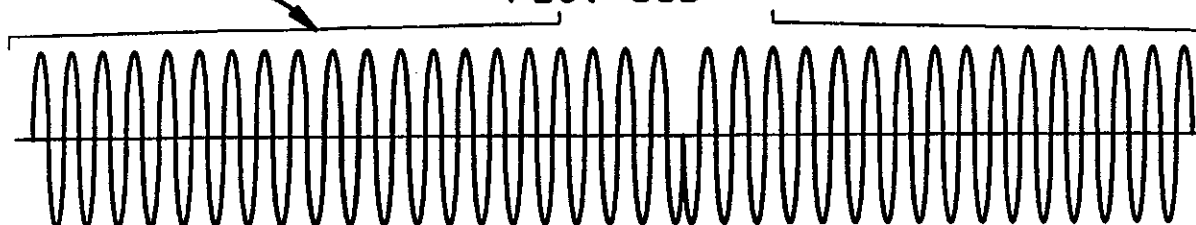
1016

FIG. 55A



5504

FIG. 55B



5508

FIG. 55D

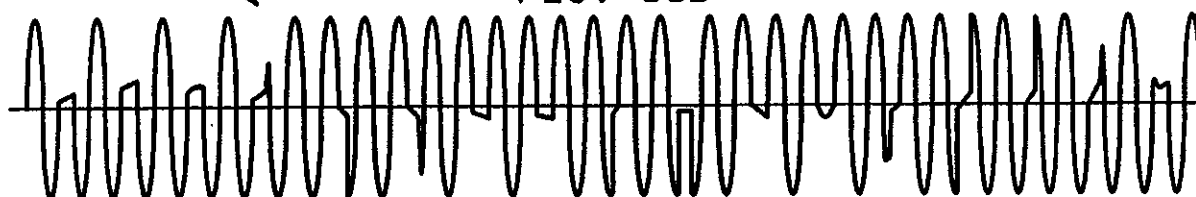


FIG. 55C

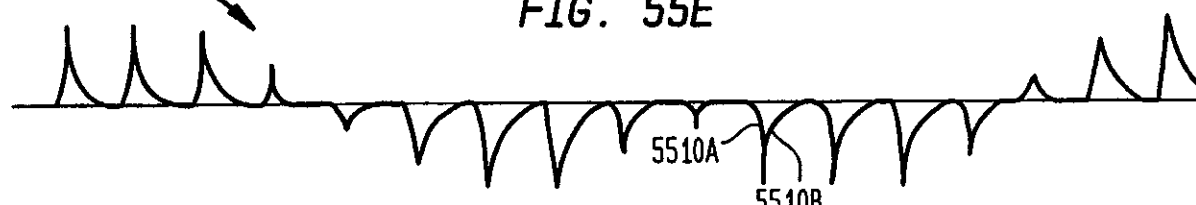
5506

5507

APERTURES
5509

5512

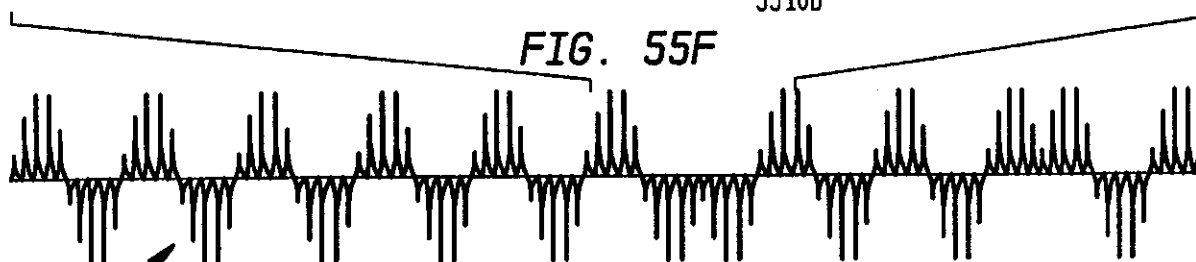
FIG. 55E



5510A

5510B

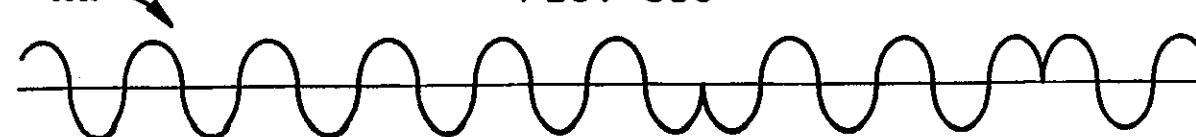
FIG. 55F



5514

5516

FIG. 55G



67/283

FIG. 56A

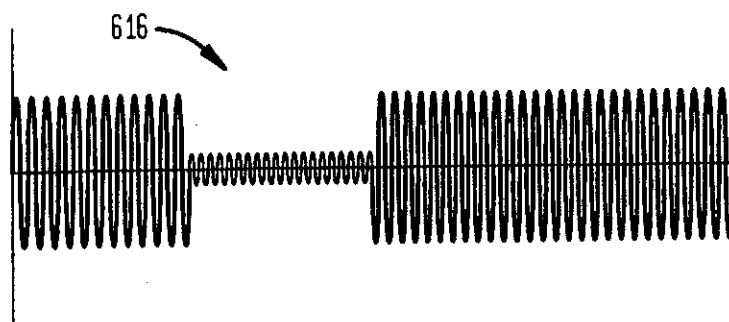


FIG. 56B

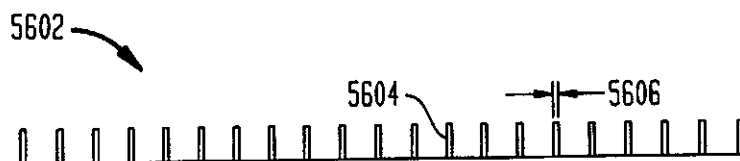


FIG. 56C

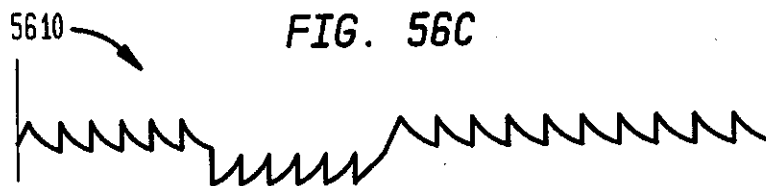
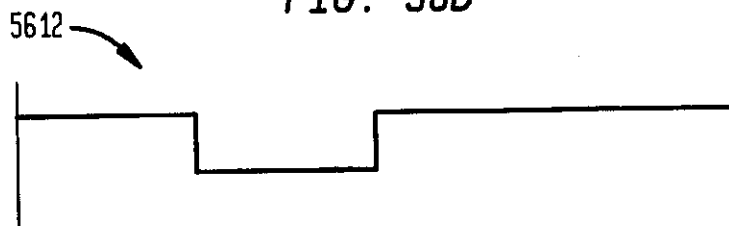


FIG. 56D



68/283

FIG. 57A

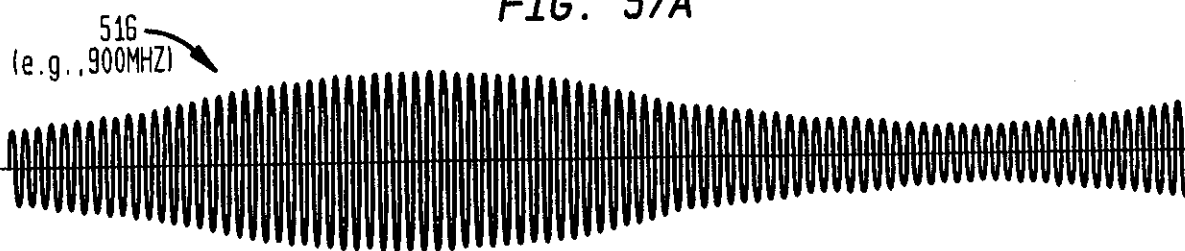


FIG. 57B

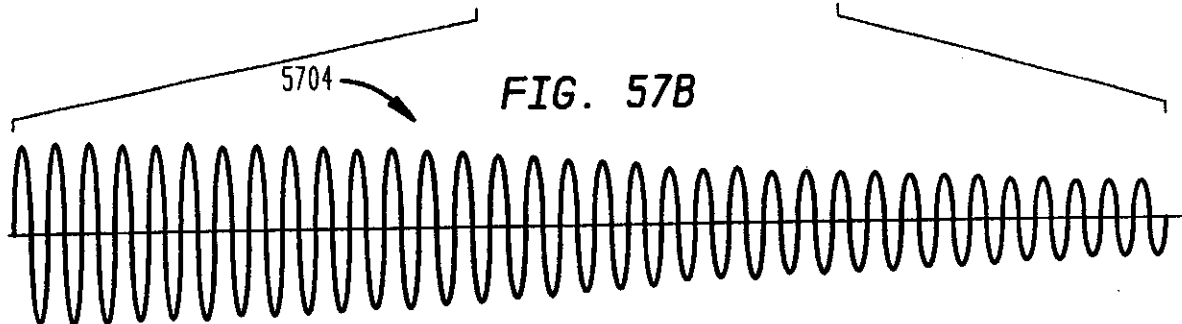


FIG. 57D

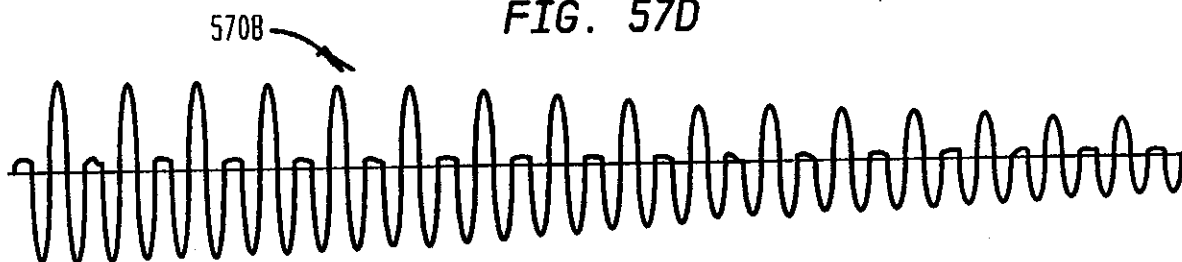


FIG. 57C

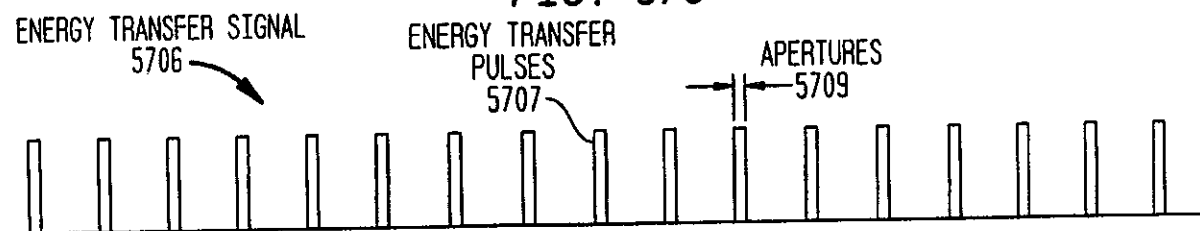


FIG. 57E

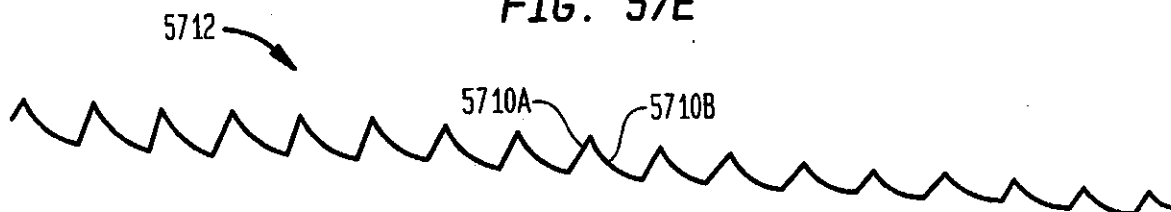
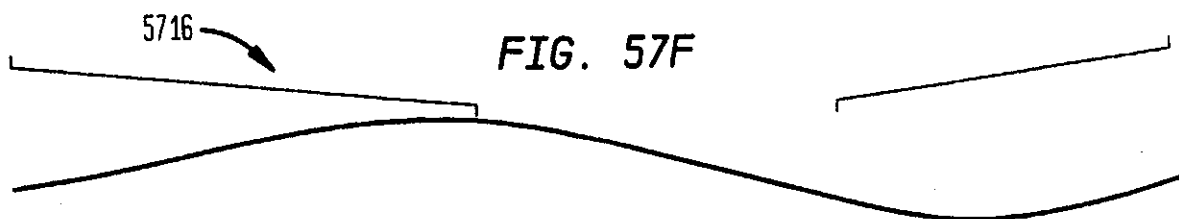


FIG. 57F



70/283

FIG. 59A

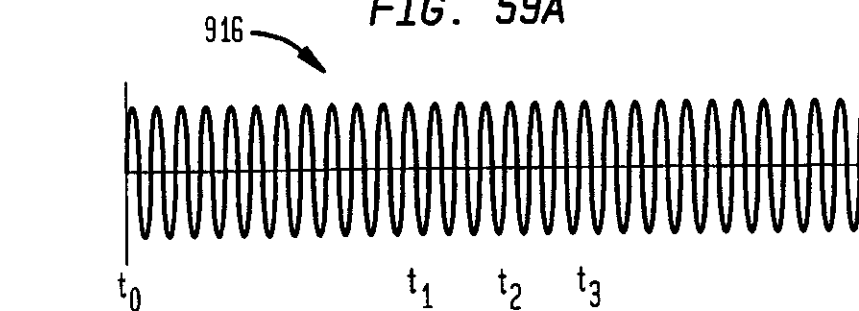


FIG. 59B

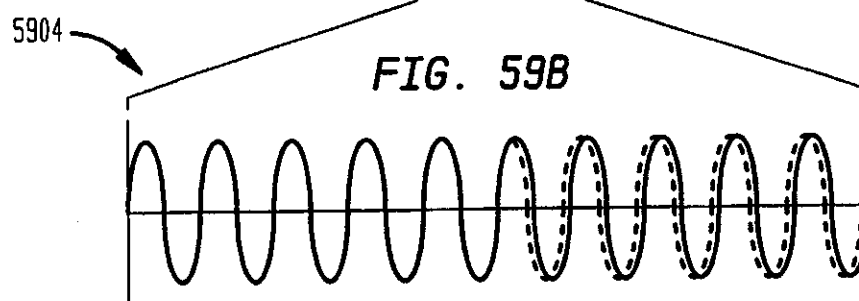


FIG. 59D

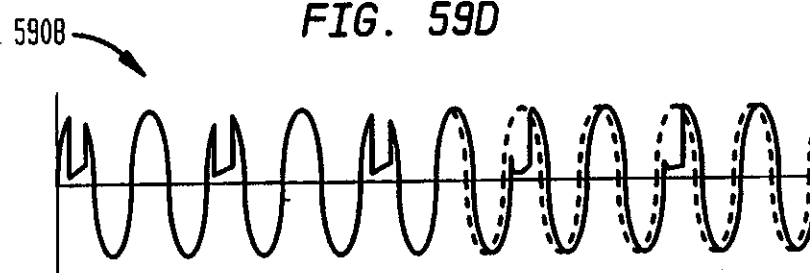


FIG. 59C

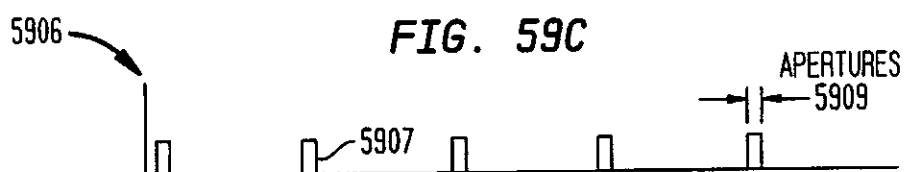


FIG. 59E

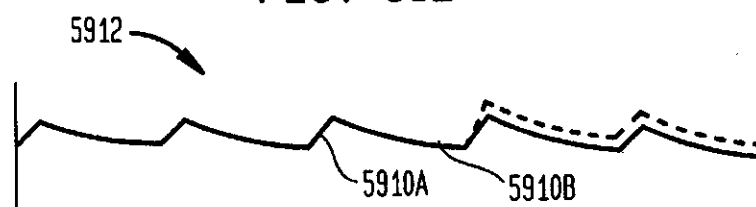
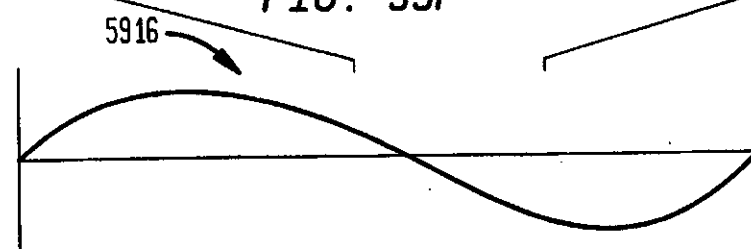


FIG. 59F



71/283

FIG. 60A

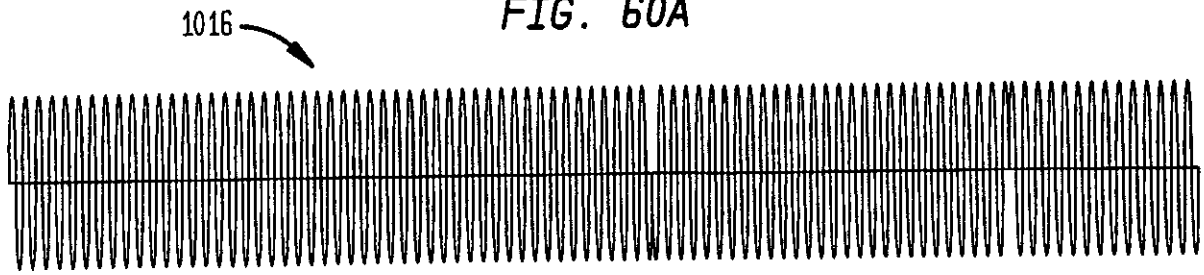


FIG. 60B

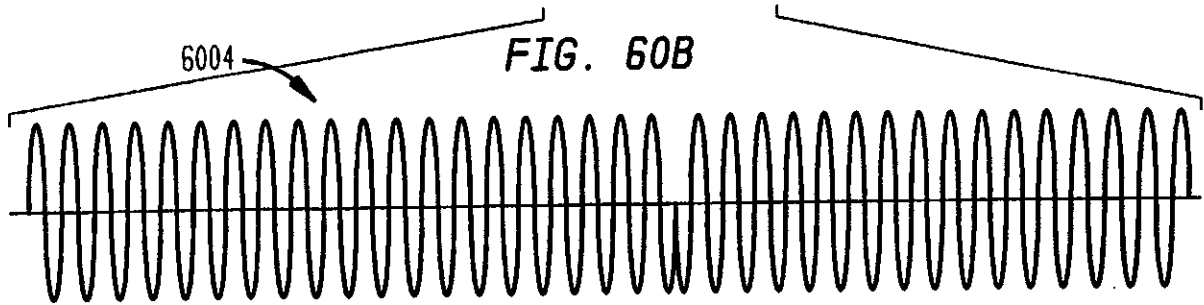


FIG. 60D

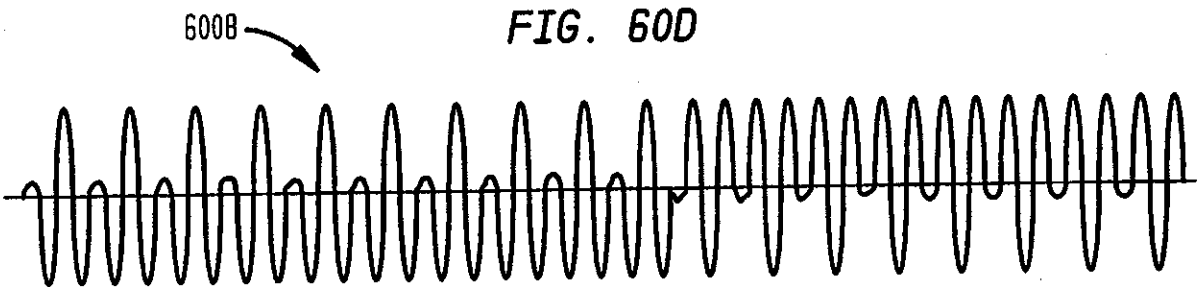


FIG. 60C

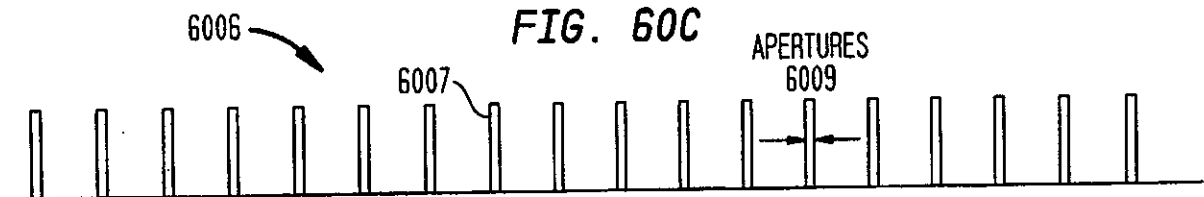


FIG. 60E

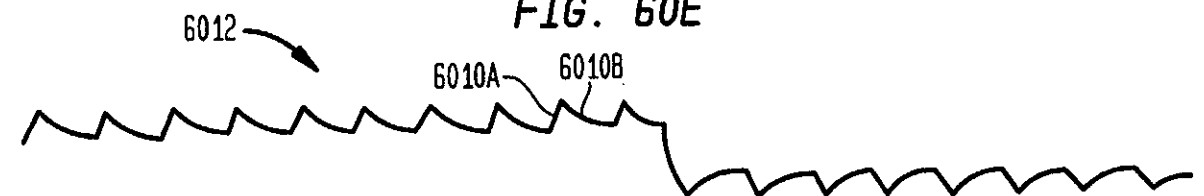
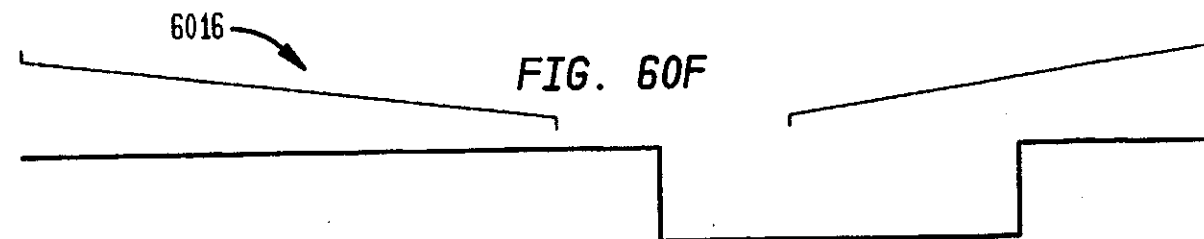
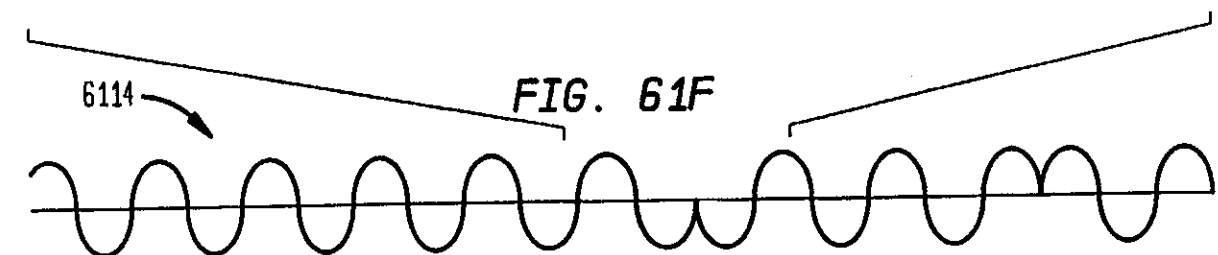
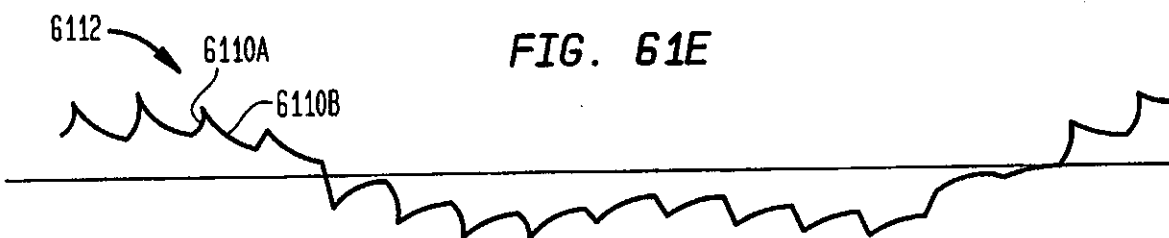
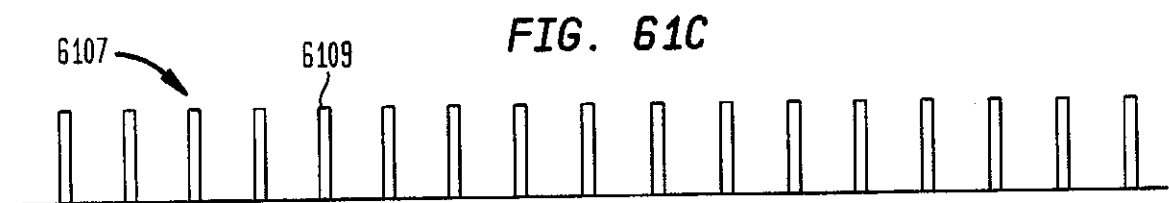
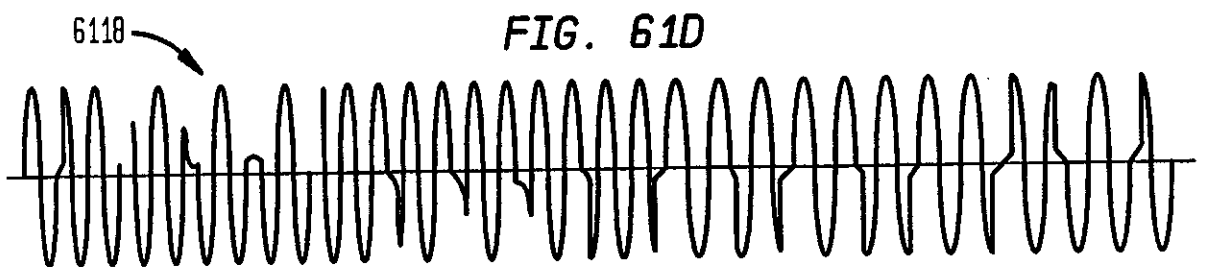
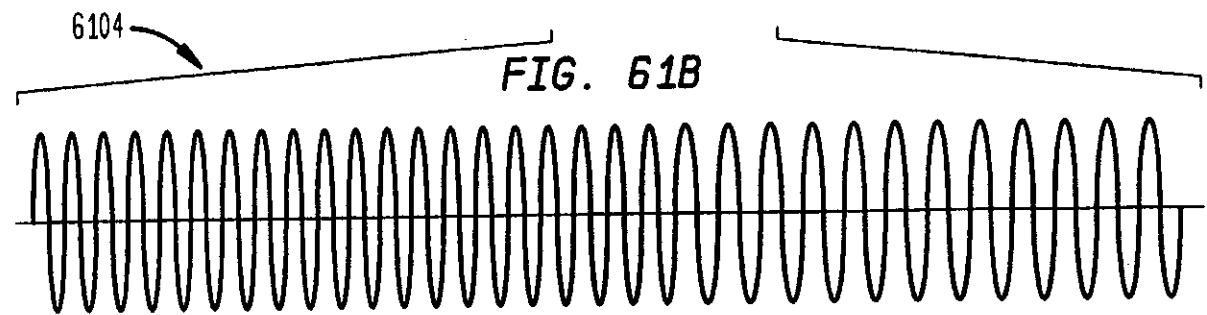
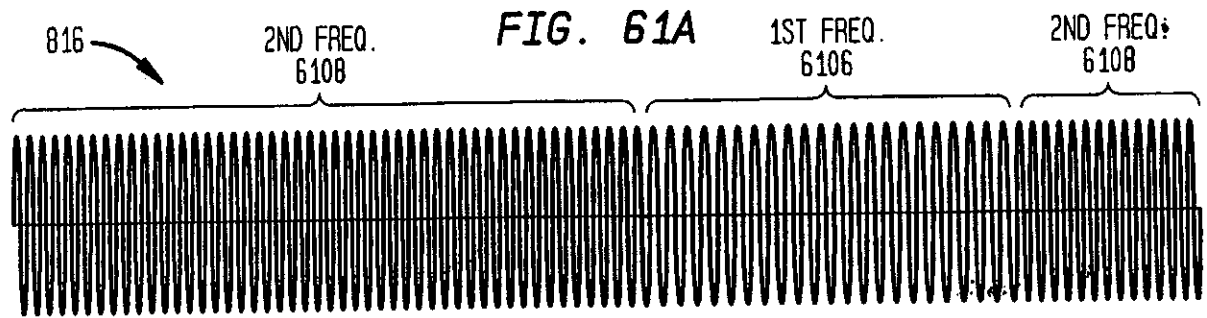


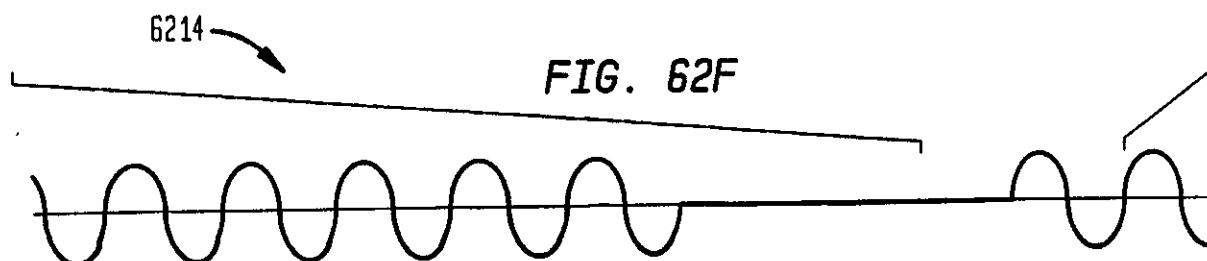
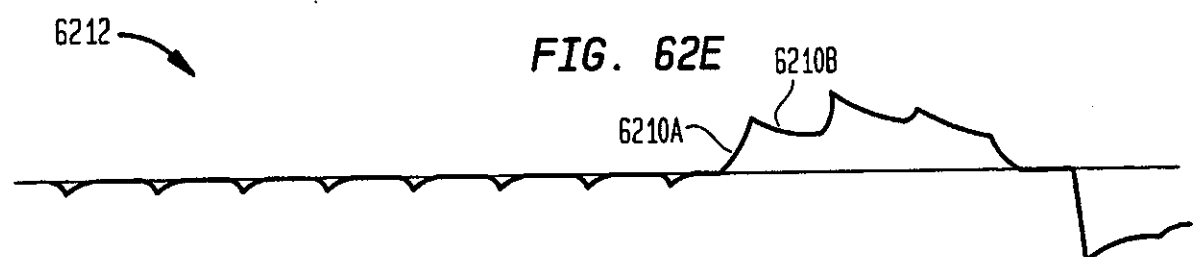
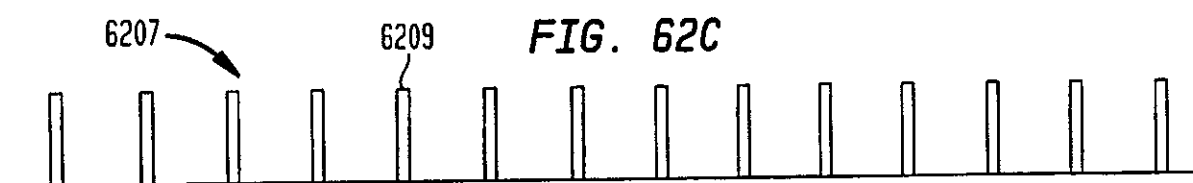
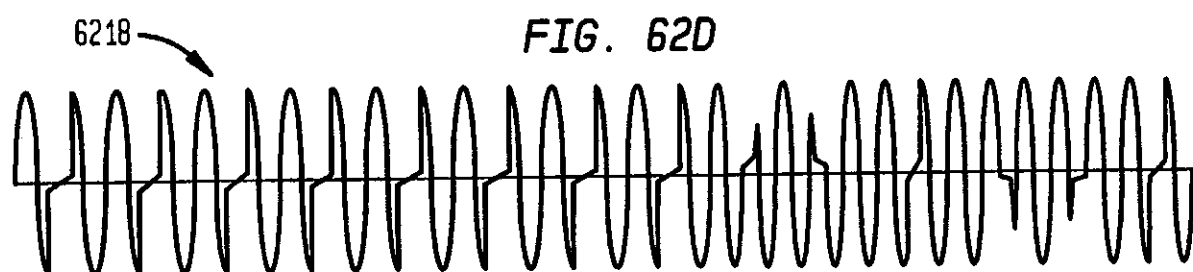
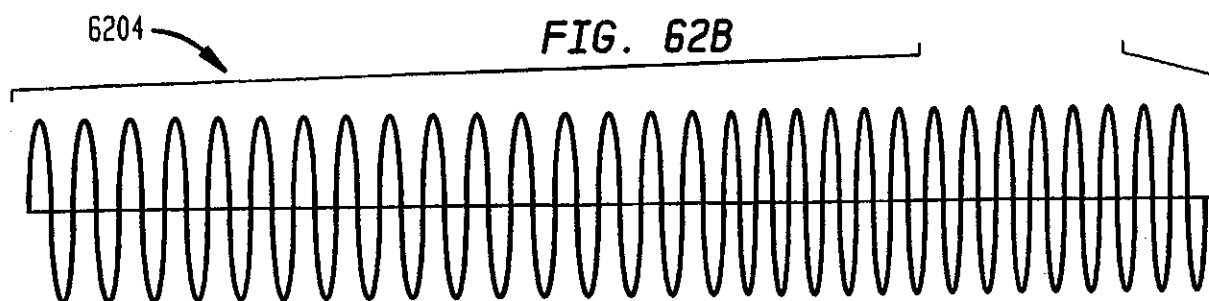
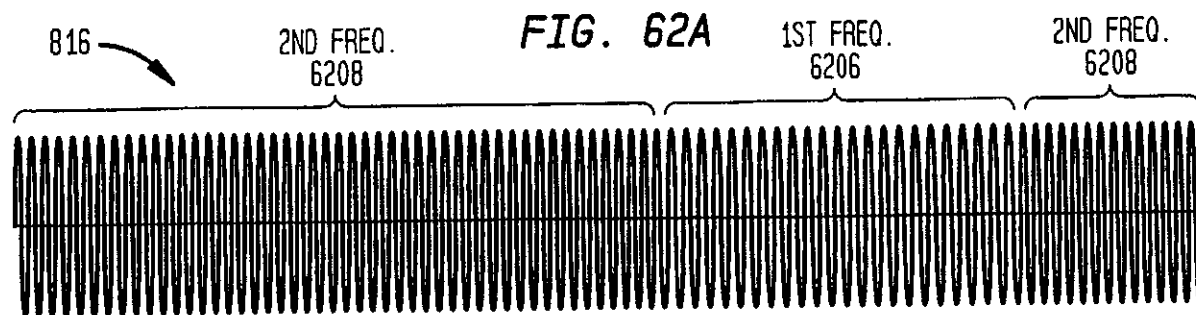
FIG. 60F



72/283



73/283



74/283

FIG. 63

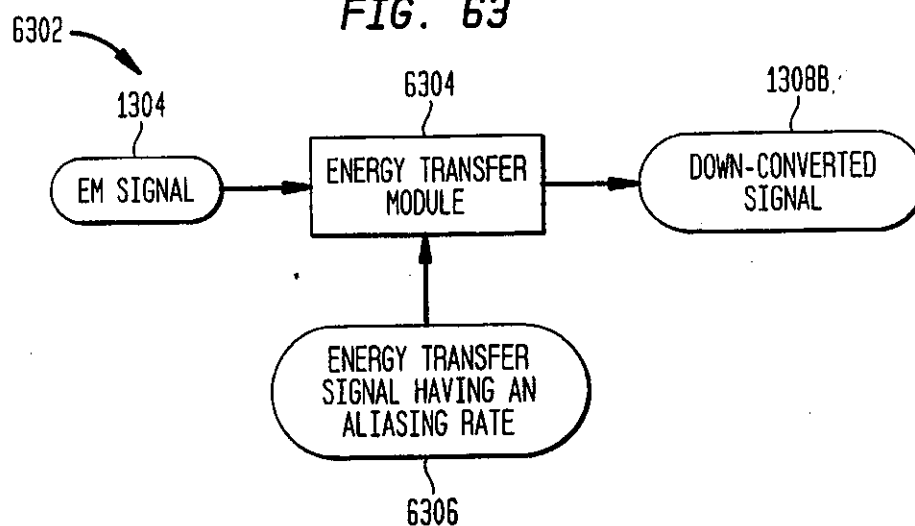


FIG. 64A

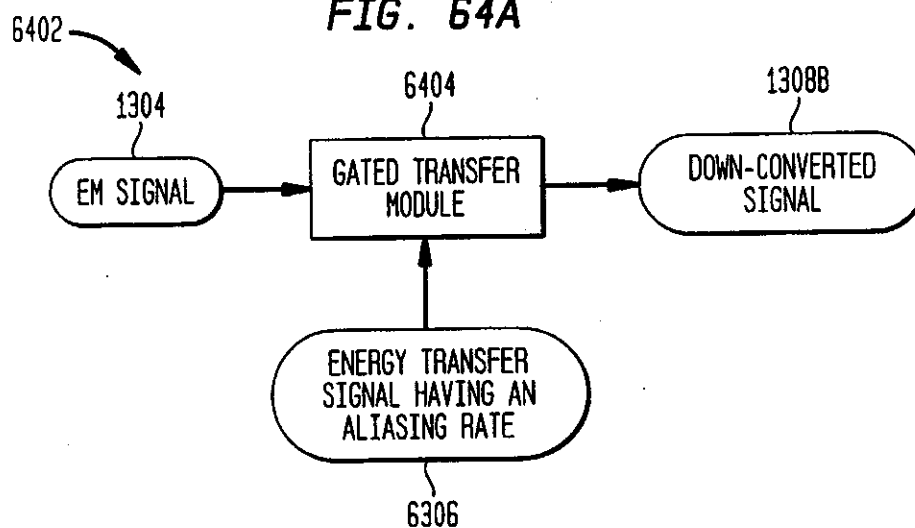
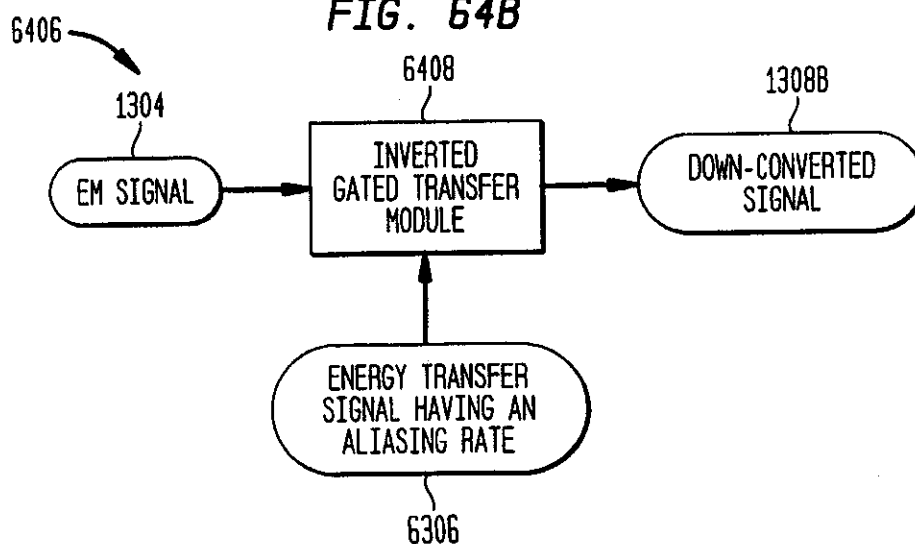


FIG. 64B



75/283

FIG. 65

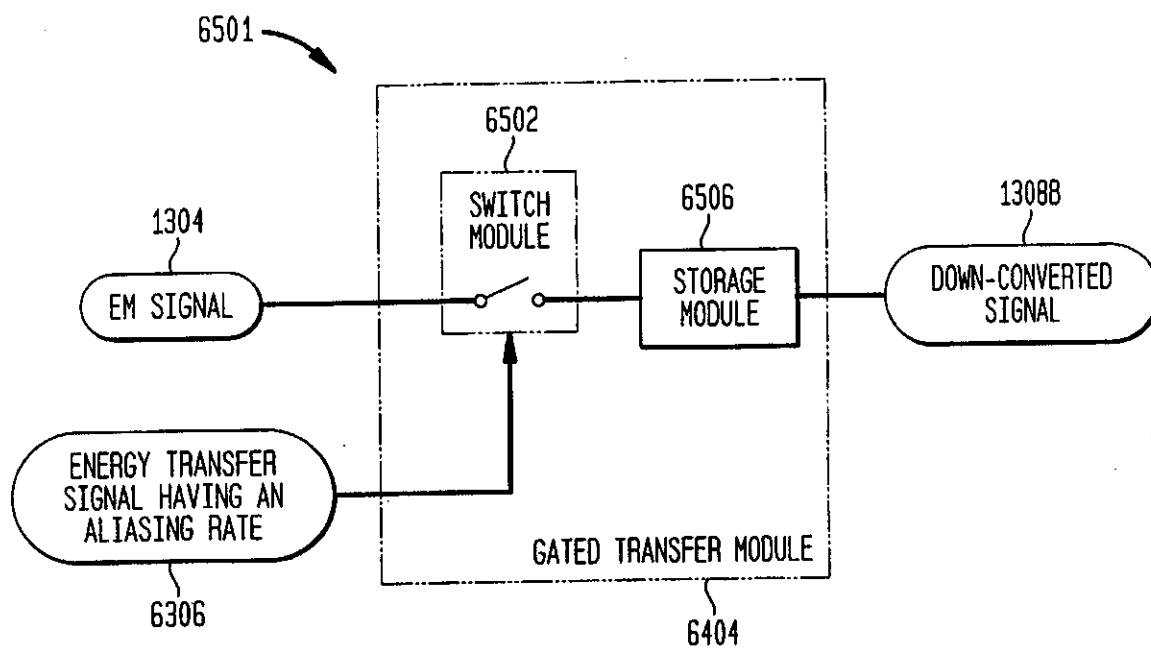


FIG. 66A

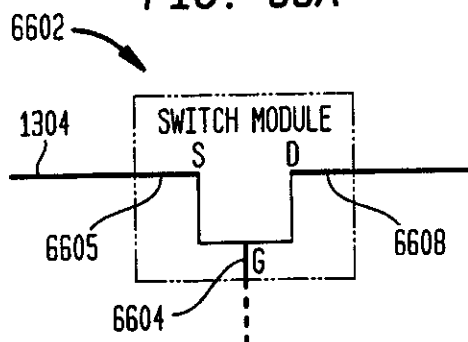
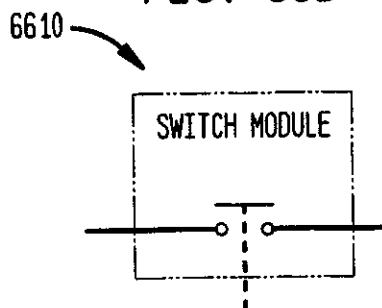


FIG. 66B



76/283

FIG. 66C

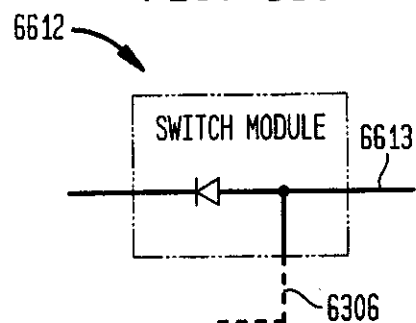
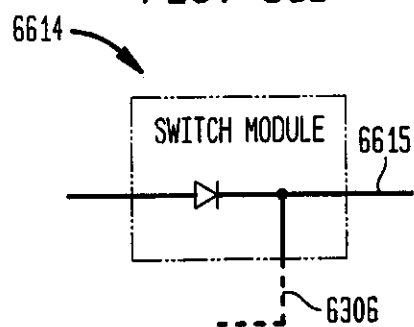
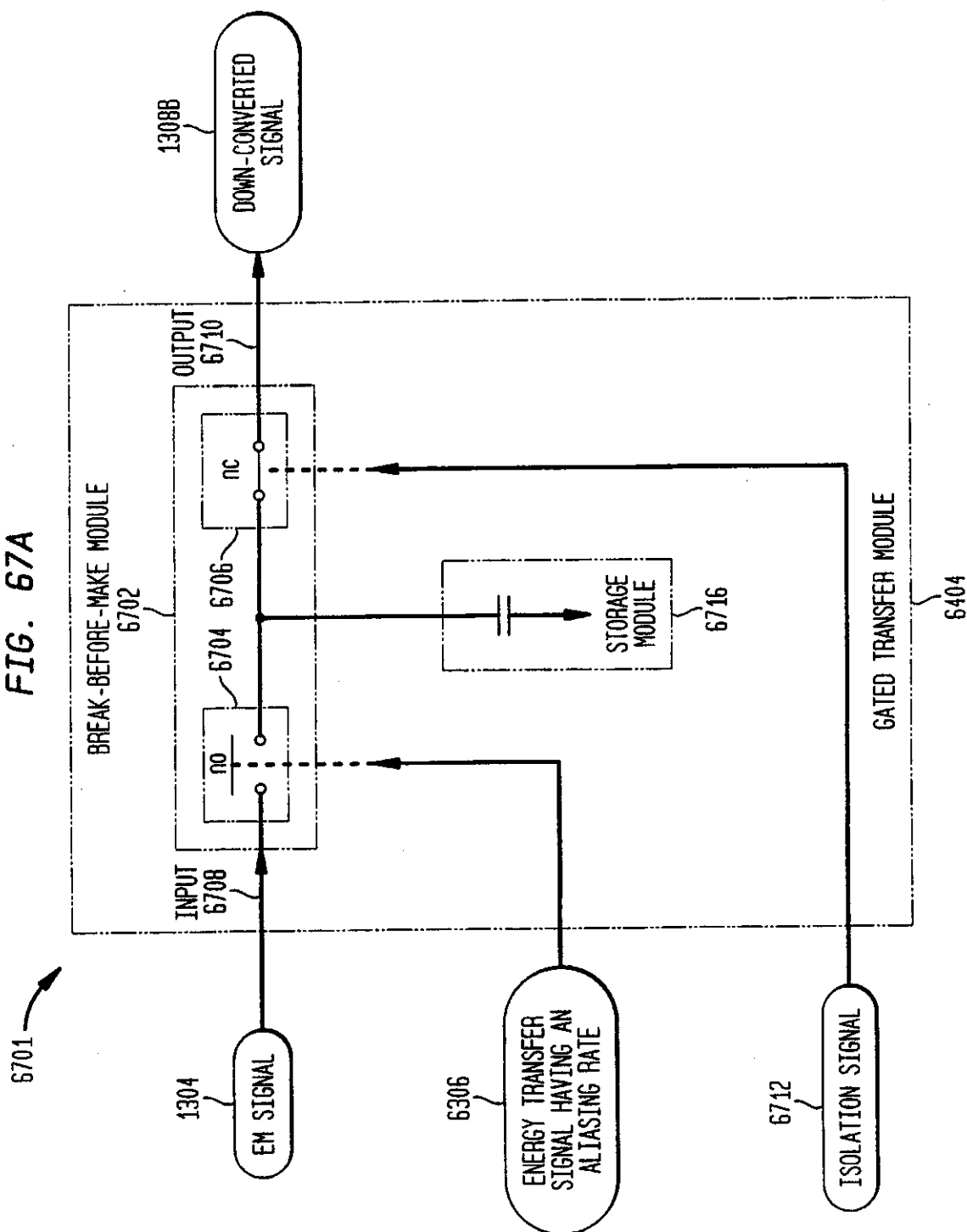


FIG. 66D



77/283

FIG. 67A



78/283

FIG. 67B

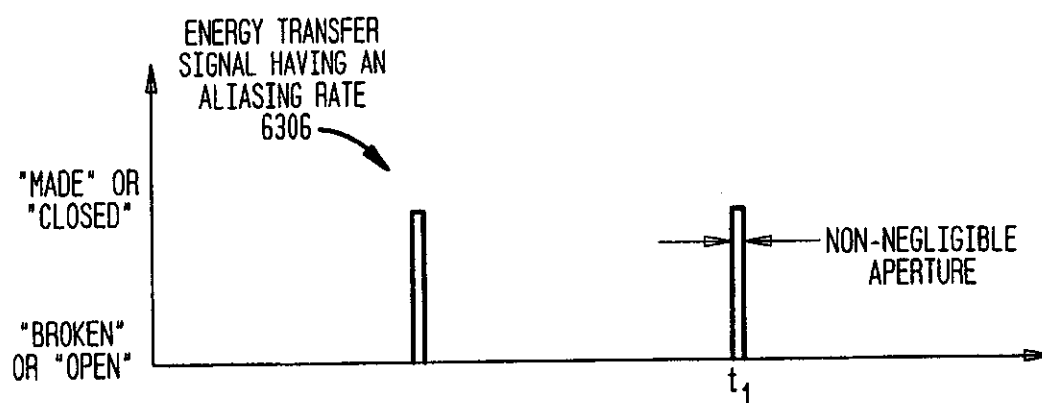
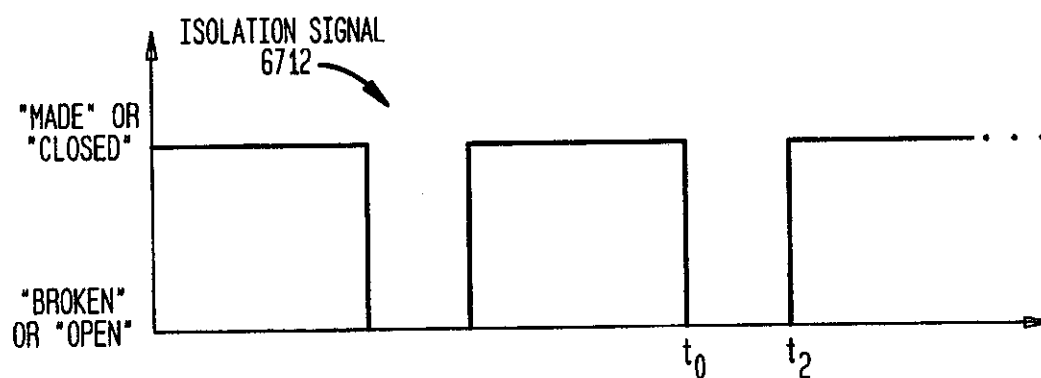


FIG. 67C



79/283

FIG. 68A

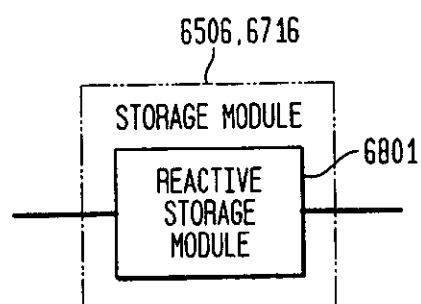


FIG. 68B

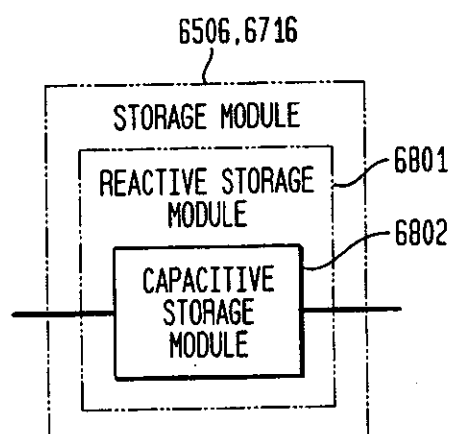
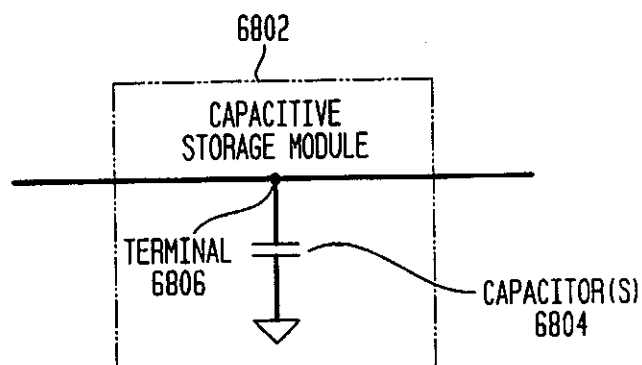


FIG. 68C



80/283

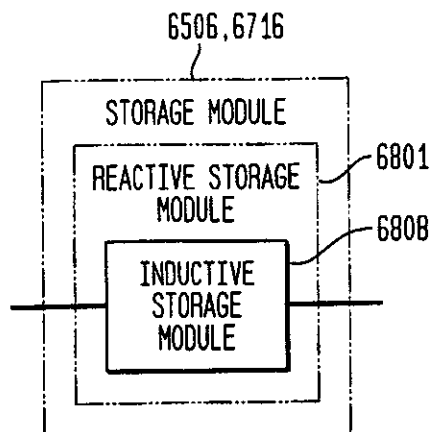
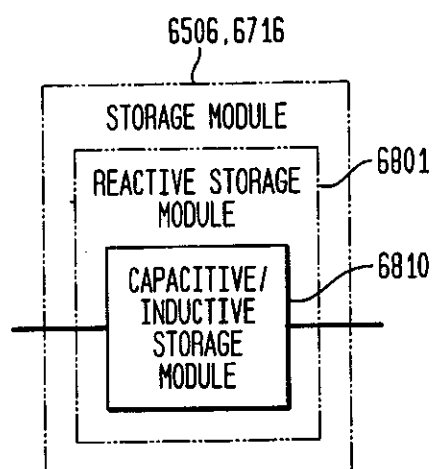
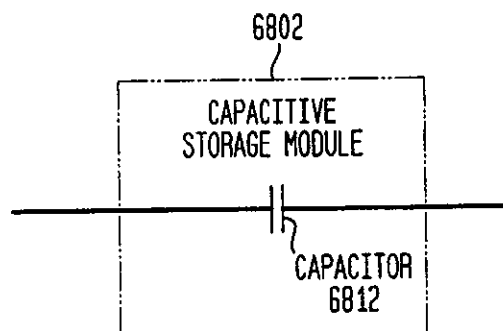
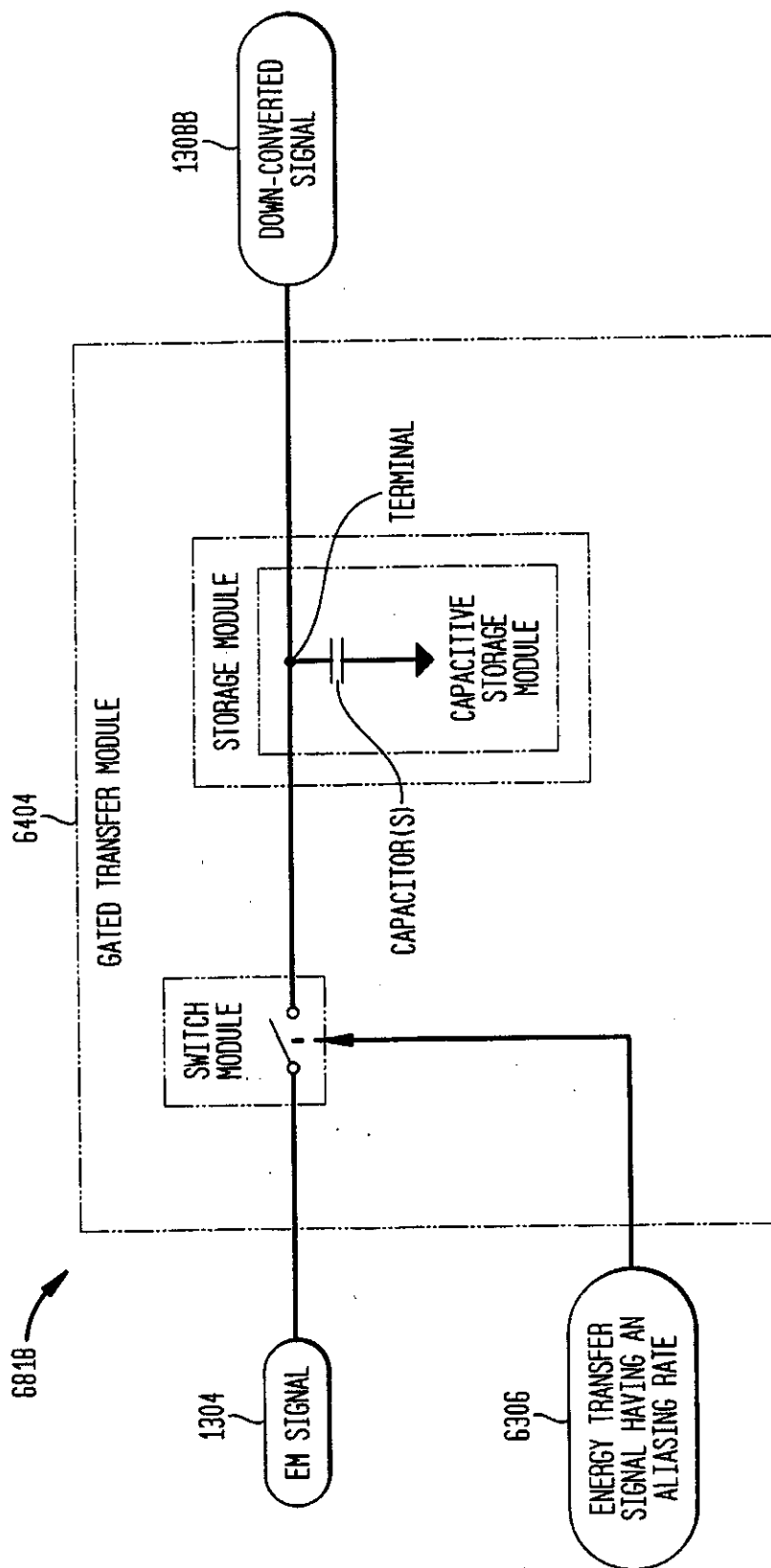
FIG. 68D**FIG. 68E****FIG. 68F**

FIG. 68G



82/283

FIG. 68H

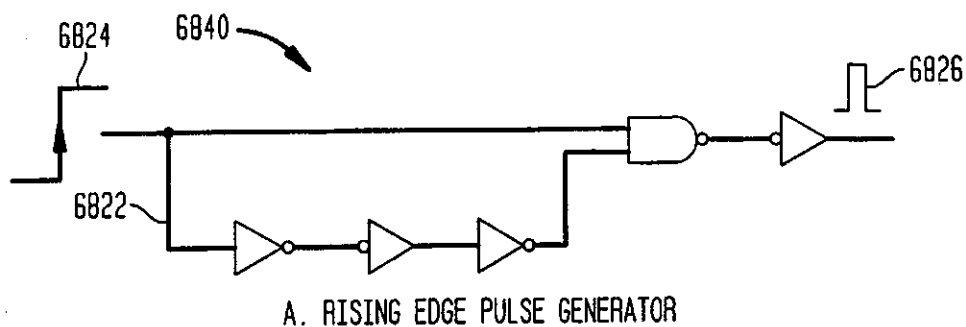


FIG. 68I

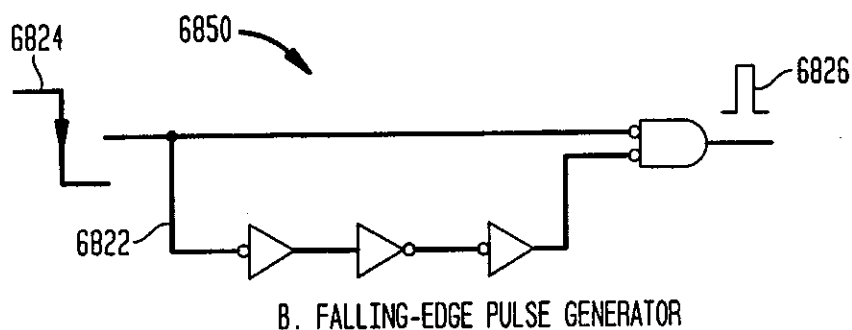
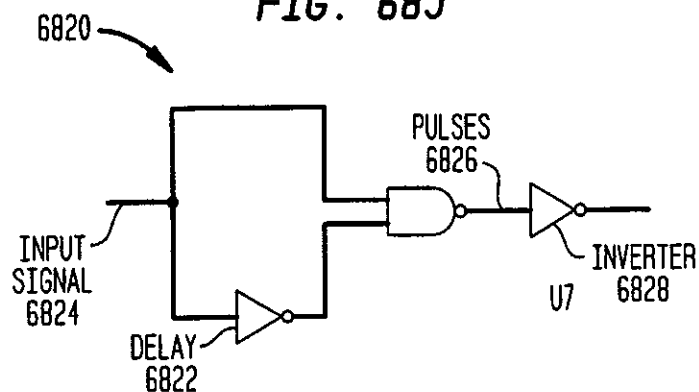
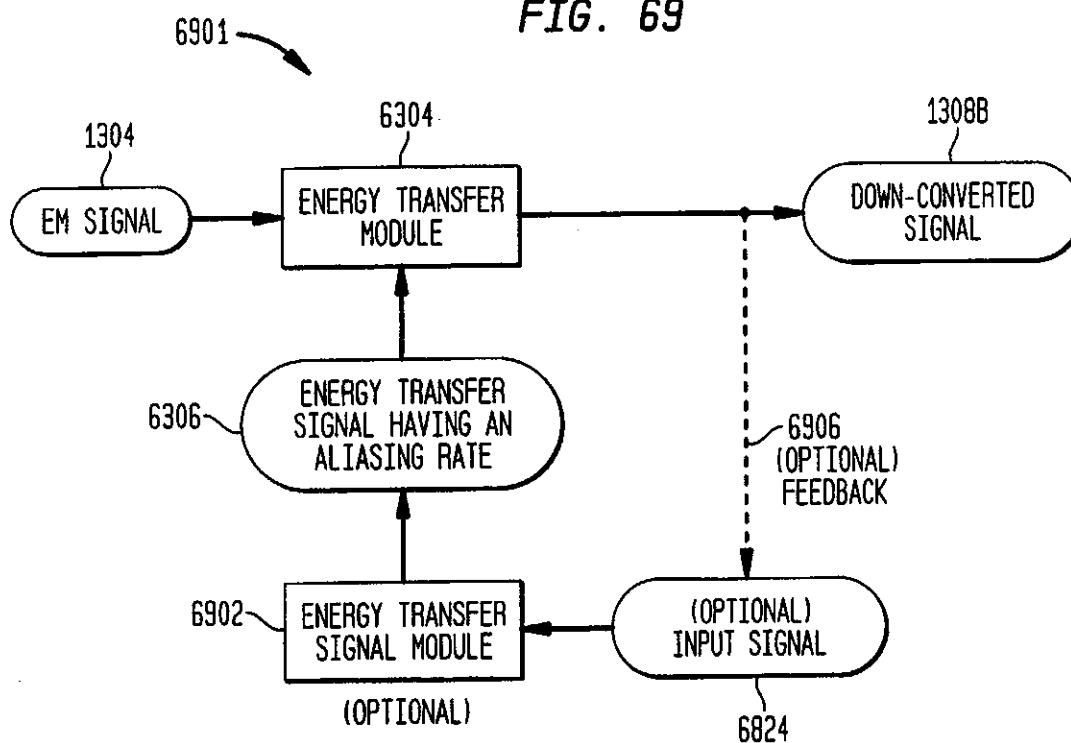


FIG. 68J



84/283

FIG. 69



85/283

FIG. 70

IMPEDANCE MATCHED ALIASING MODULE

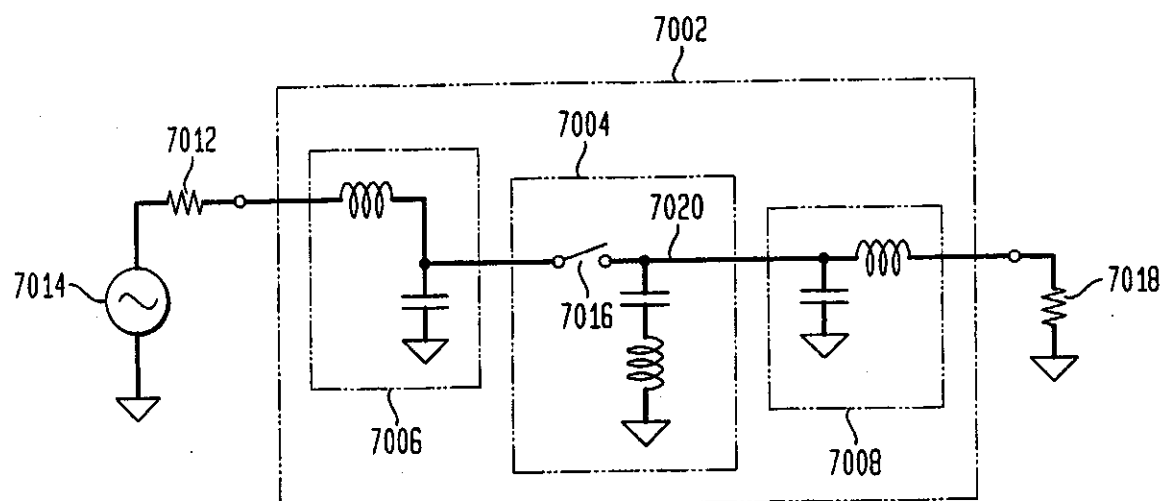


FIG. 71A

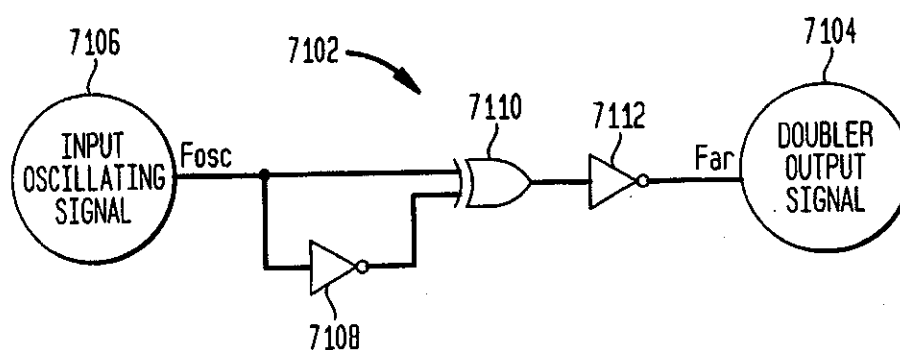


FIG. 71B

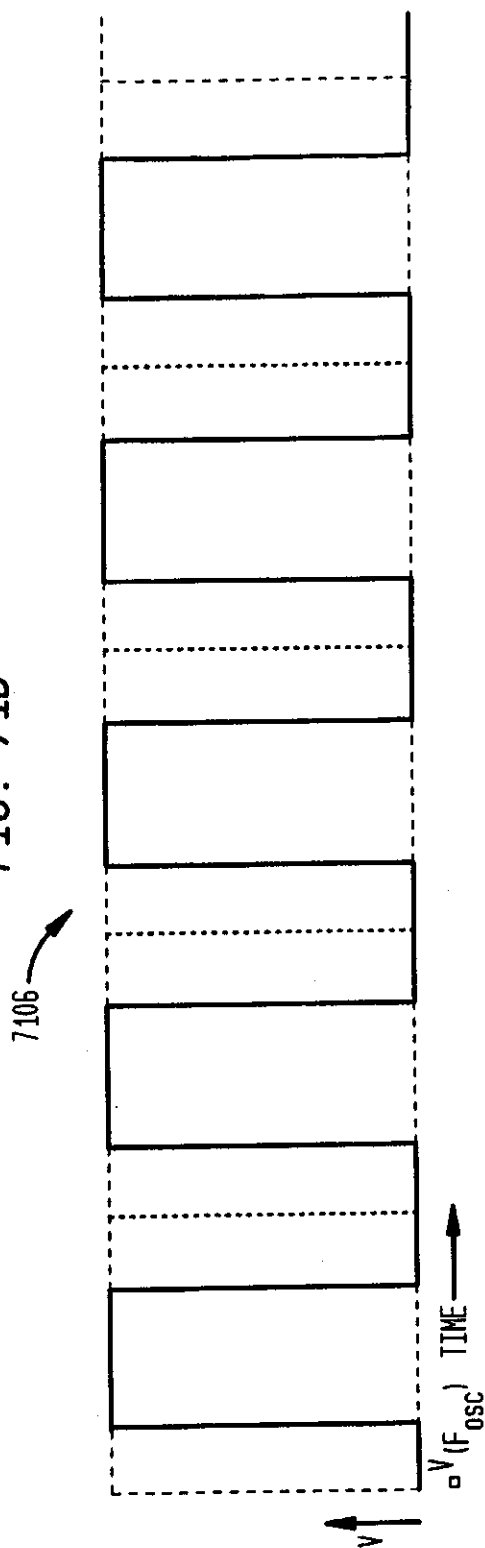
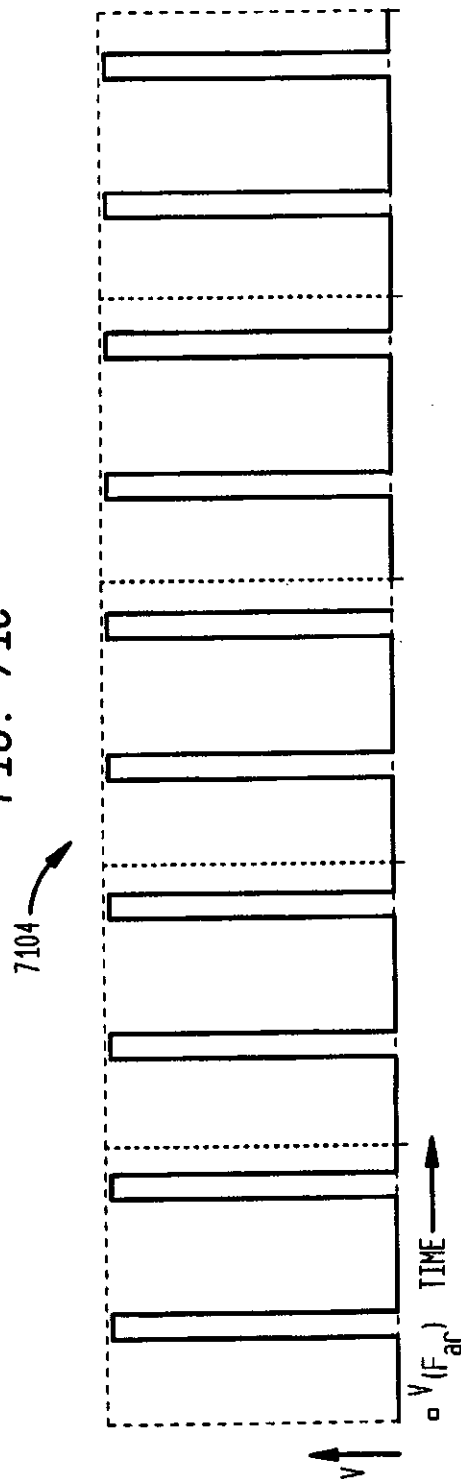


FIG. 71C



87/283

FIG. 72

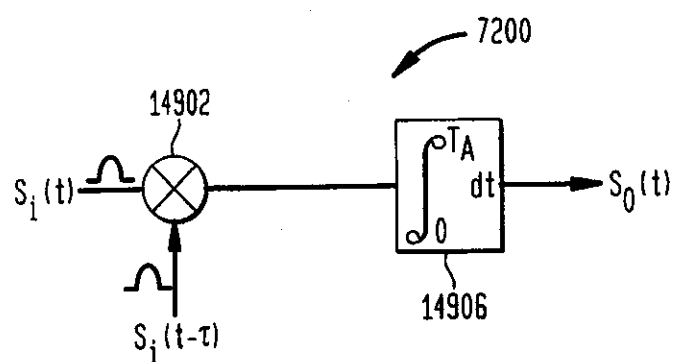
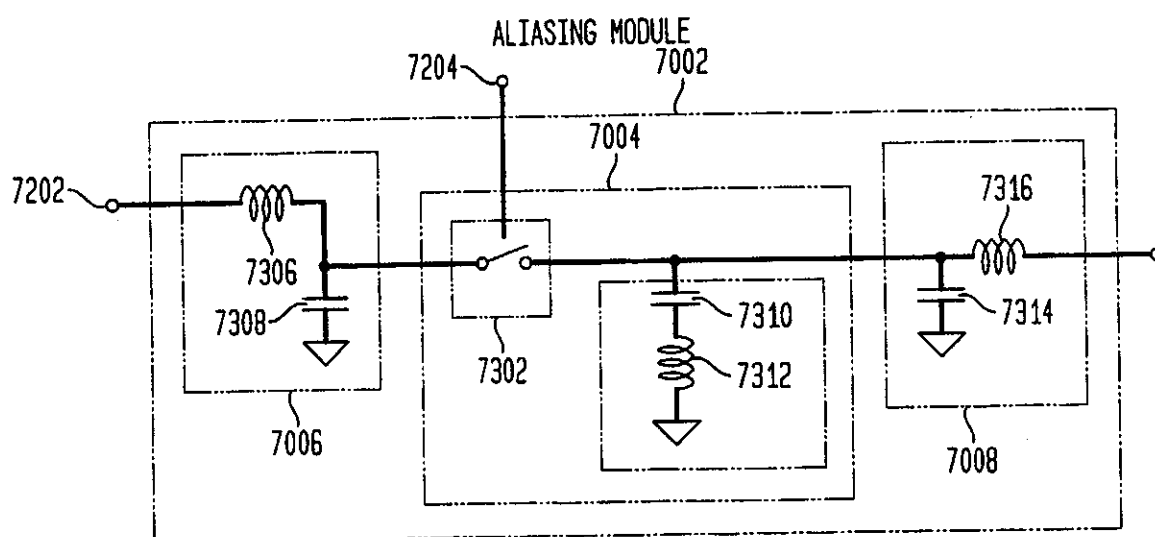
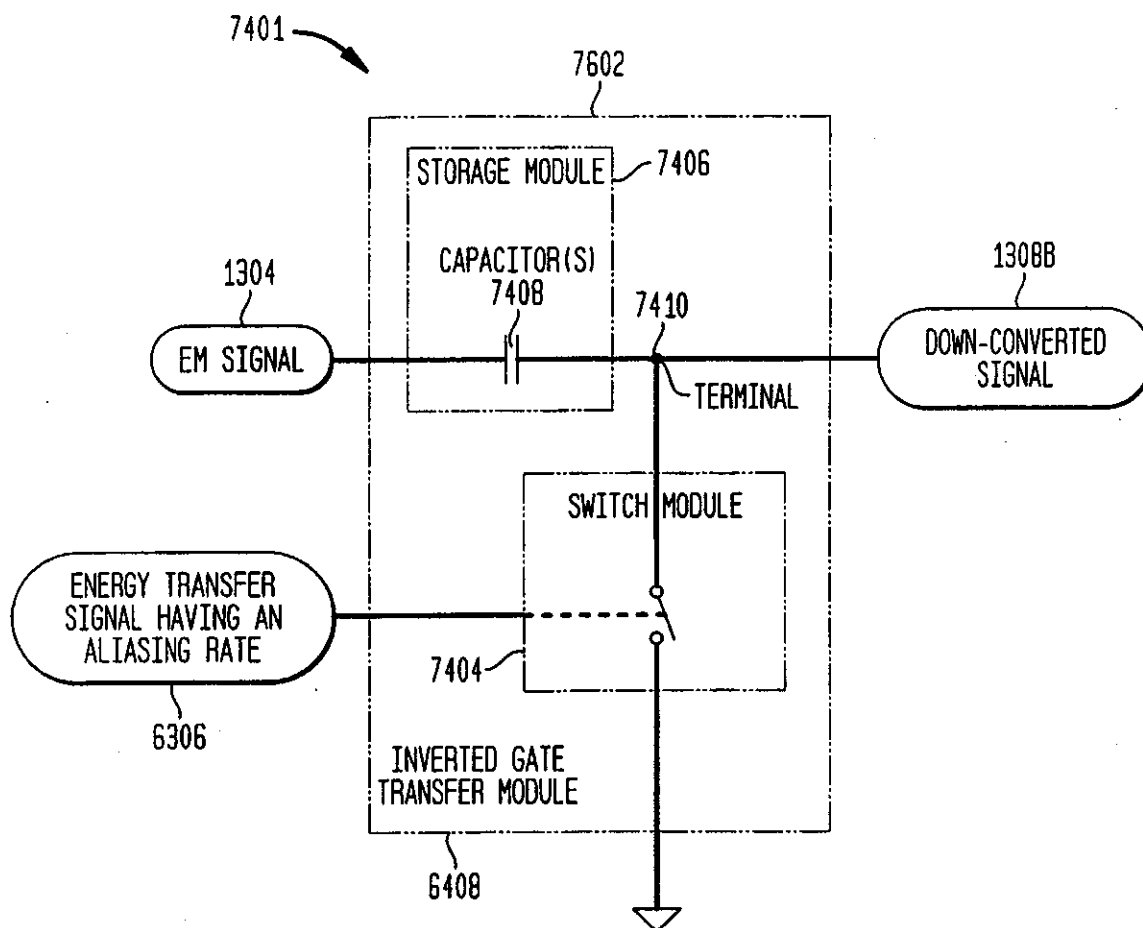


FIG. 73



88/283

FIG. 74



89/283

FIG. 75A

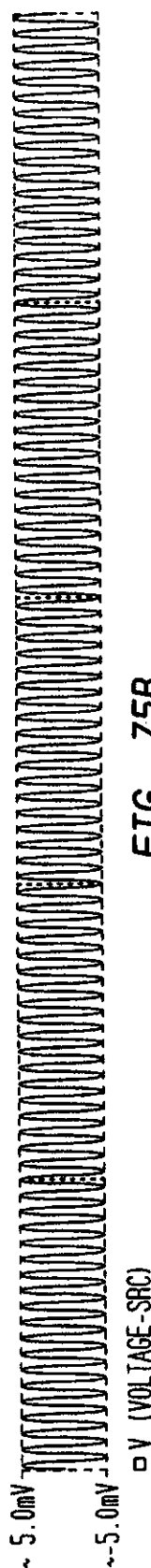


FIG. 75B

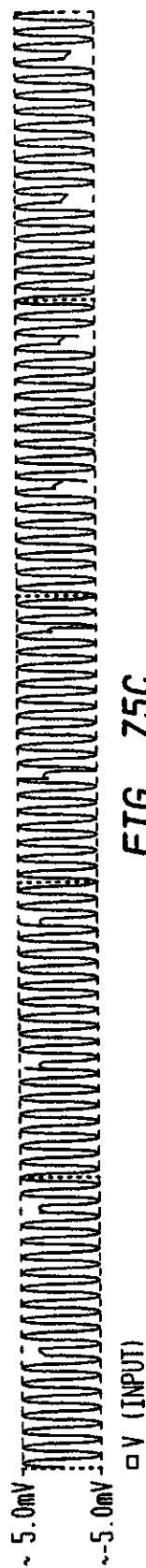


FIG. 75C

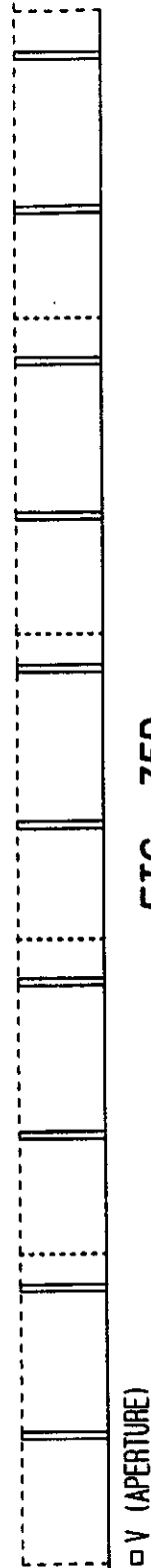


FIG. 75D

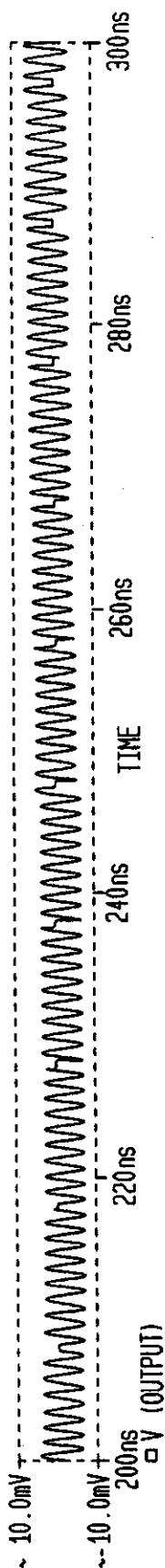
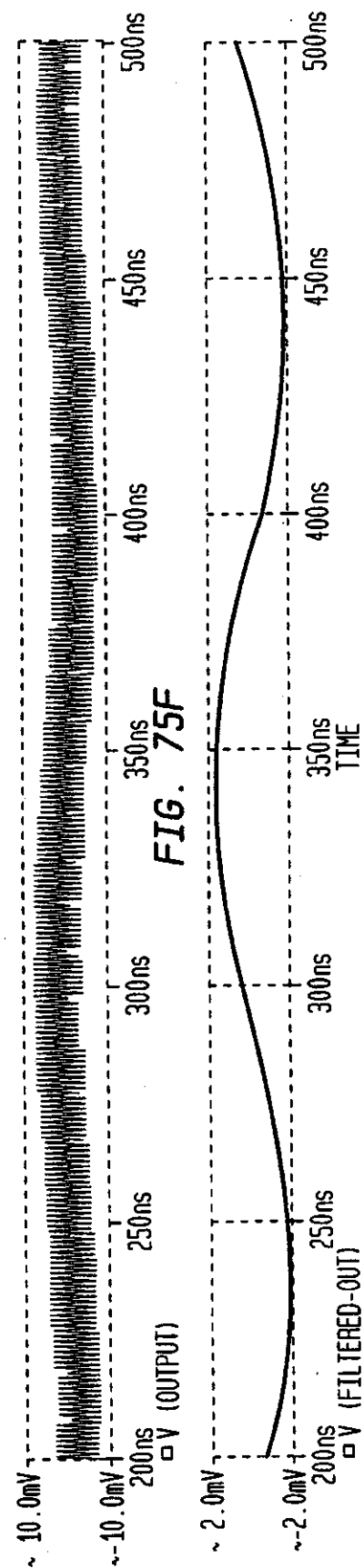


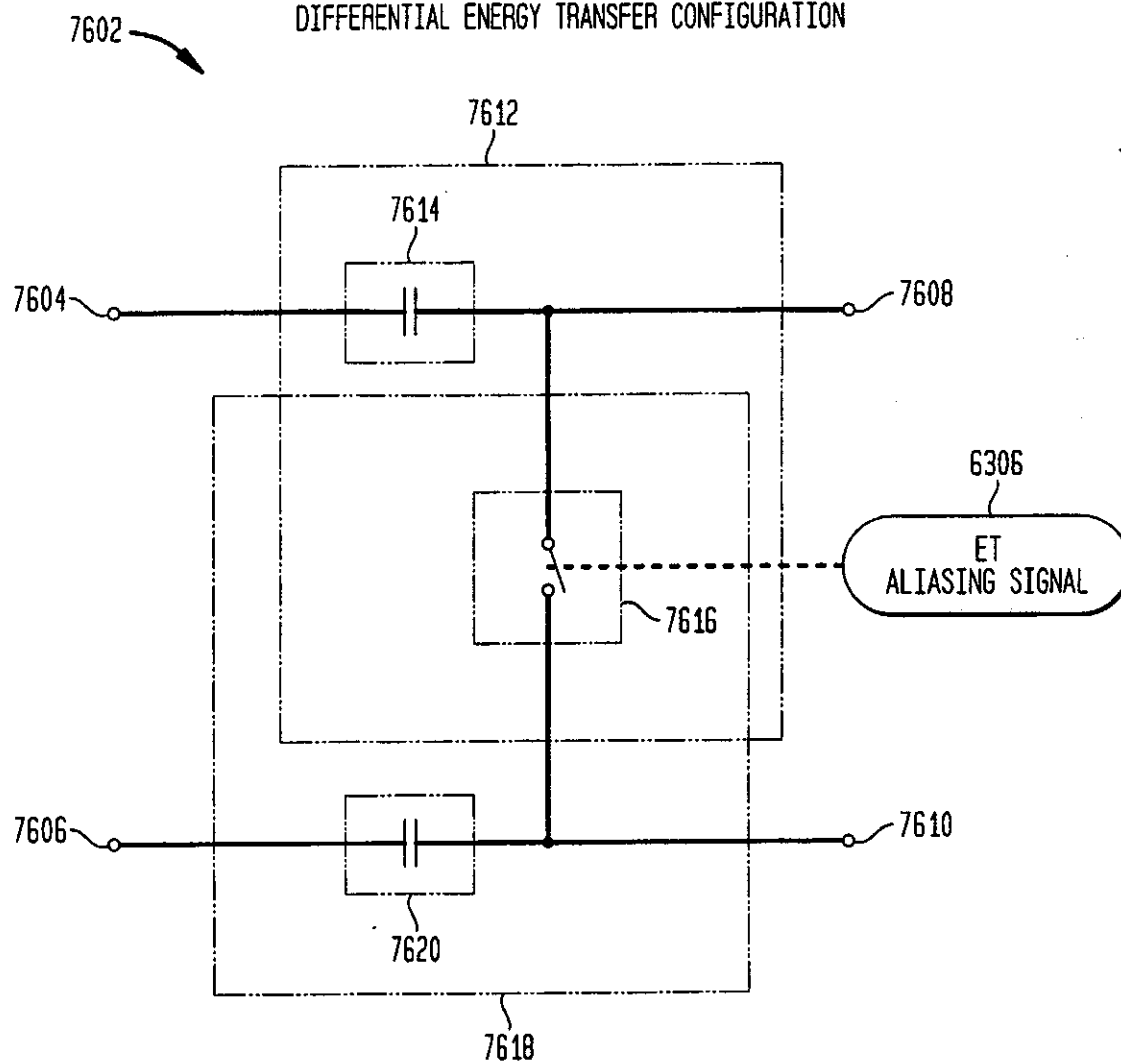
FIG. 75E



90/283

FIG. 76A

DIFFERENTIAL ENERGY TRANSFER CONFIGURATION



91/283

FIG. 76B

DIFFERENTIAL INPUT TO DIFFERENTIAL OUTPUT

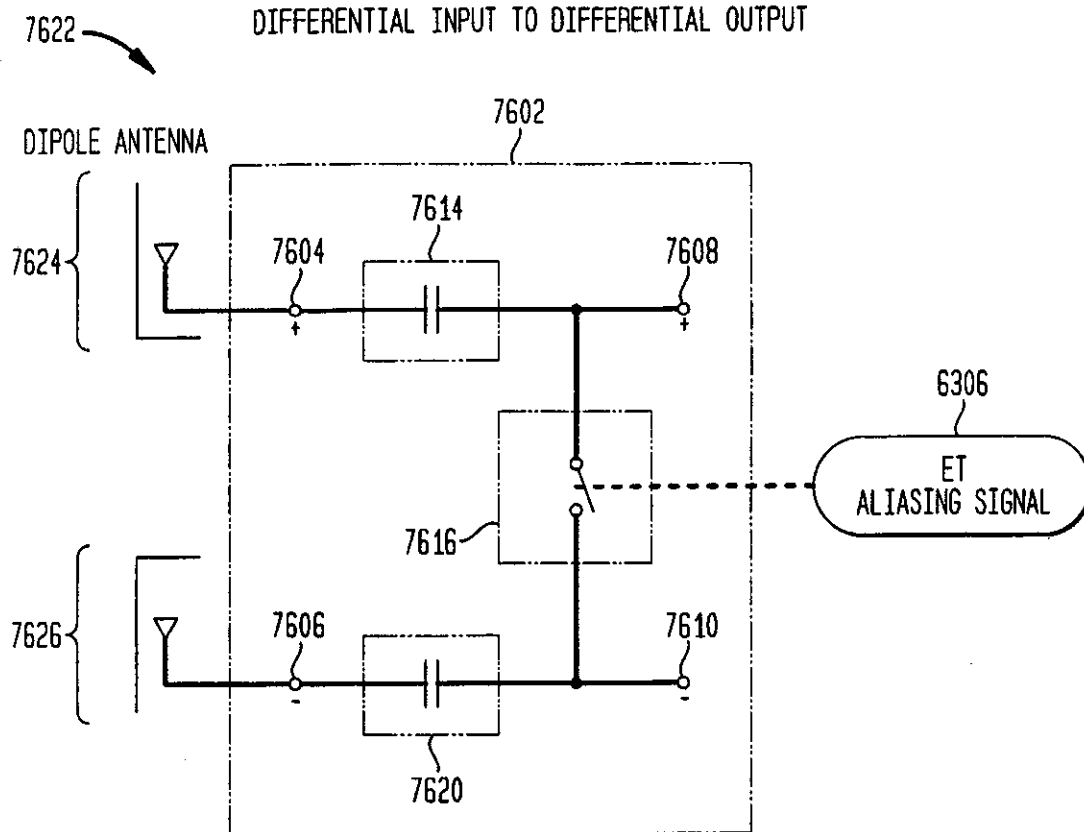
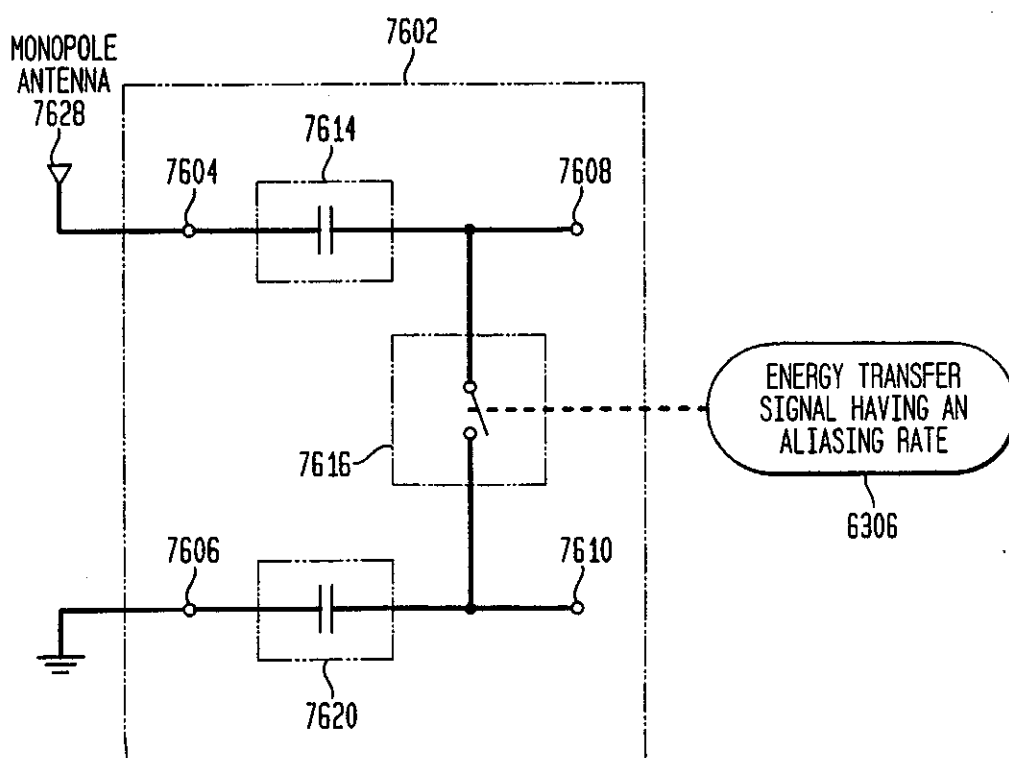


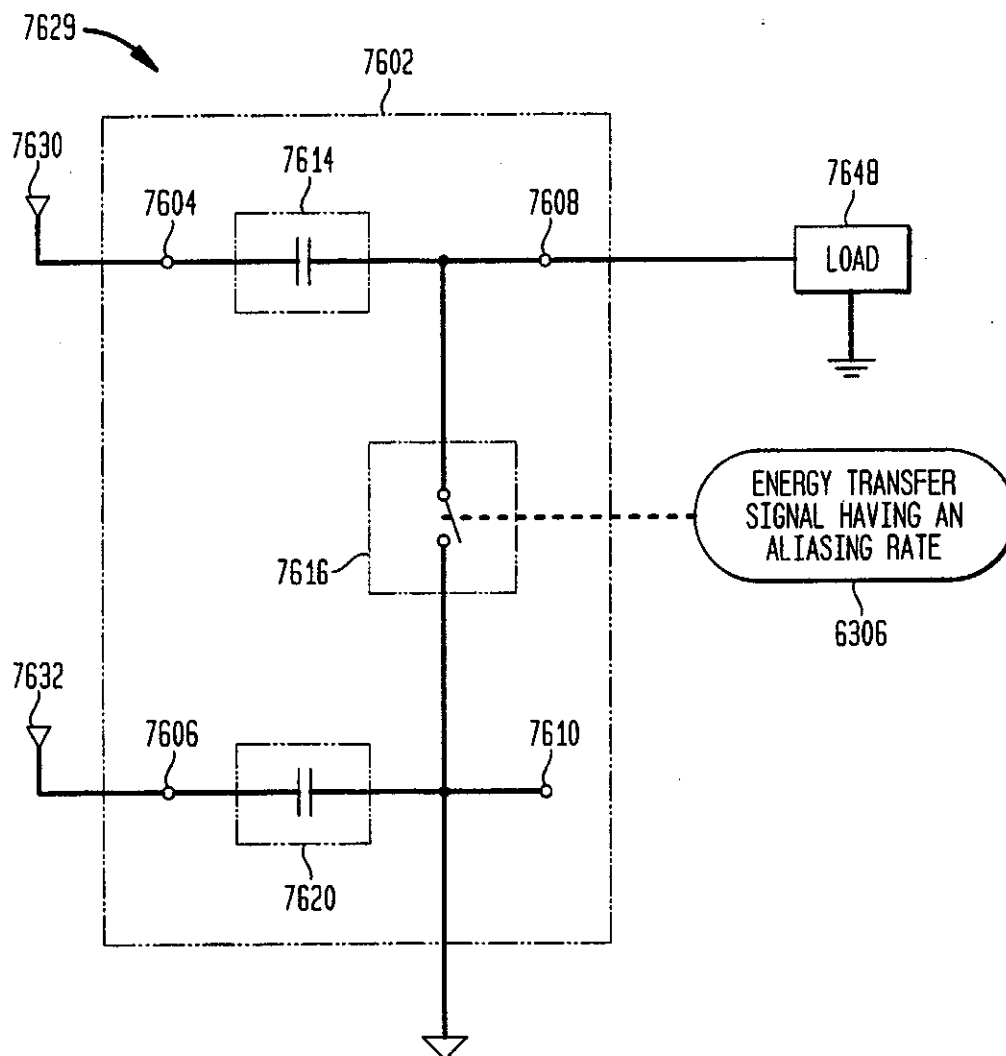
FIG. 76C

SINGLE INPUT TO DIFFERENTIAL OUTPUT



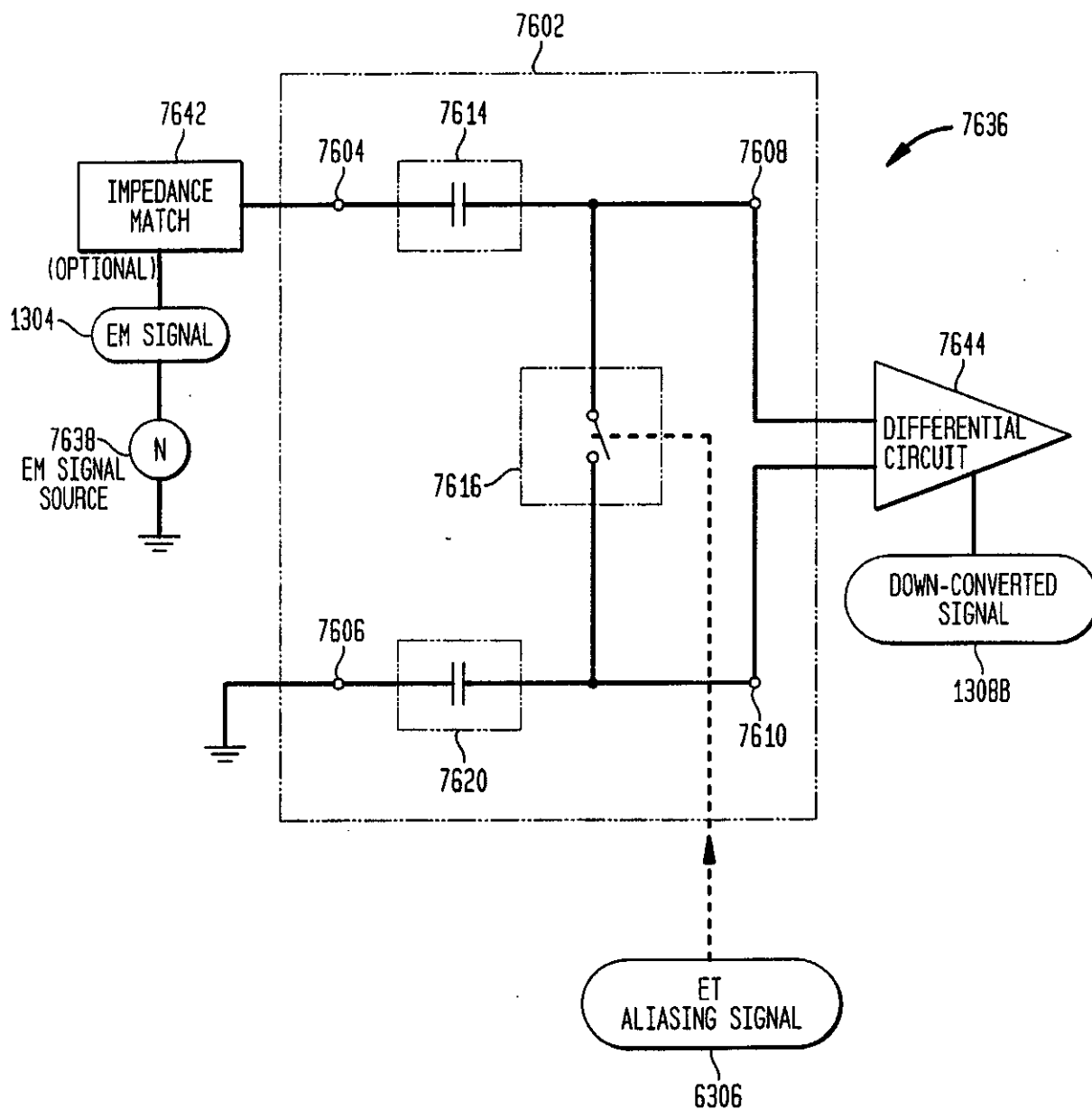
92/283

FIG. 76D
DIFFERENTIAL INPUT TO SINGLE OUTPUT



93/283

FIG. 76E
EXAMPLE INPUT/OUTPUT CIRCUITRY



94/283

FIG. 77A

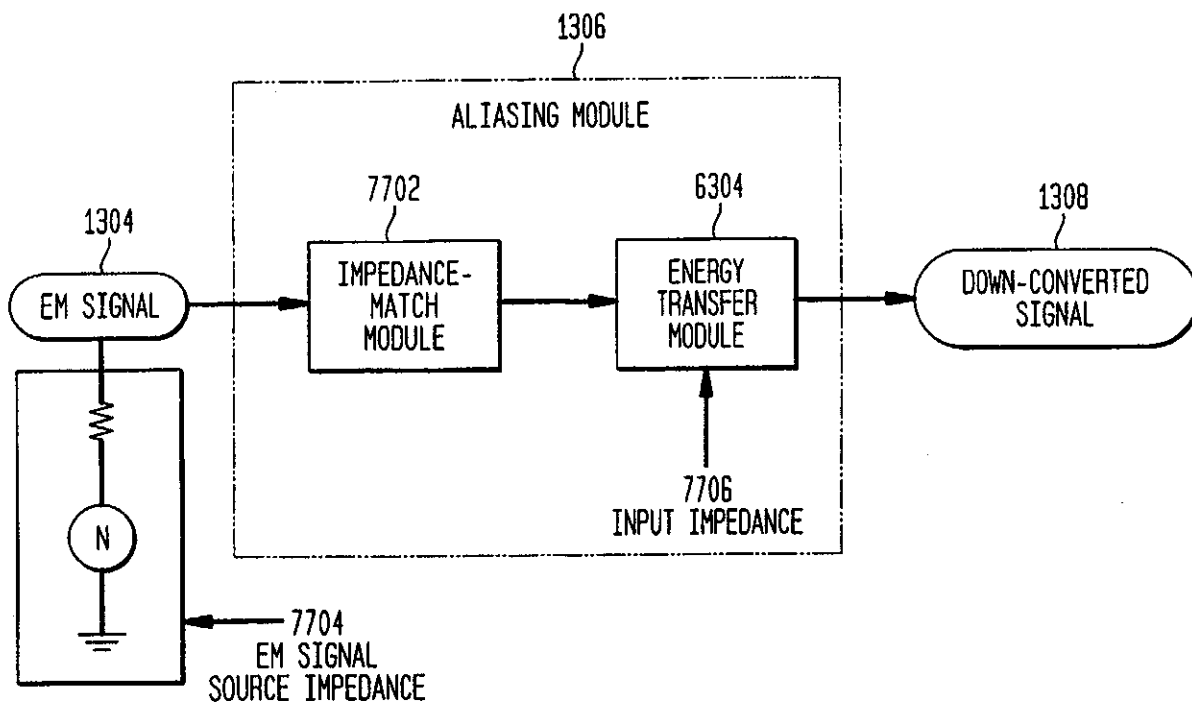
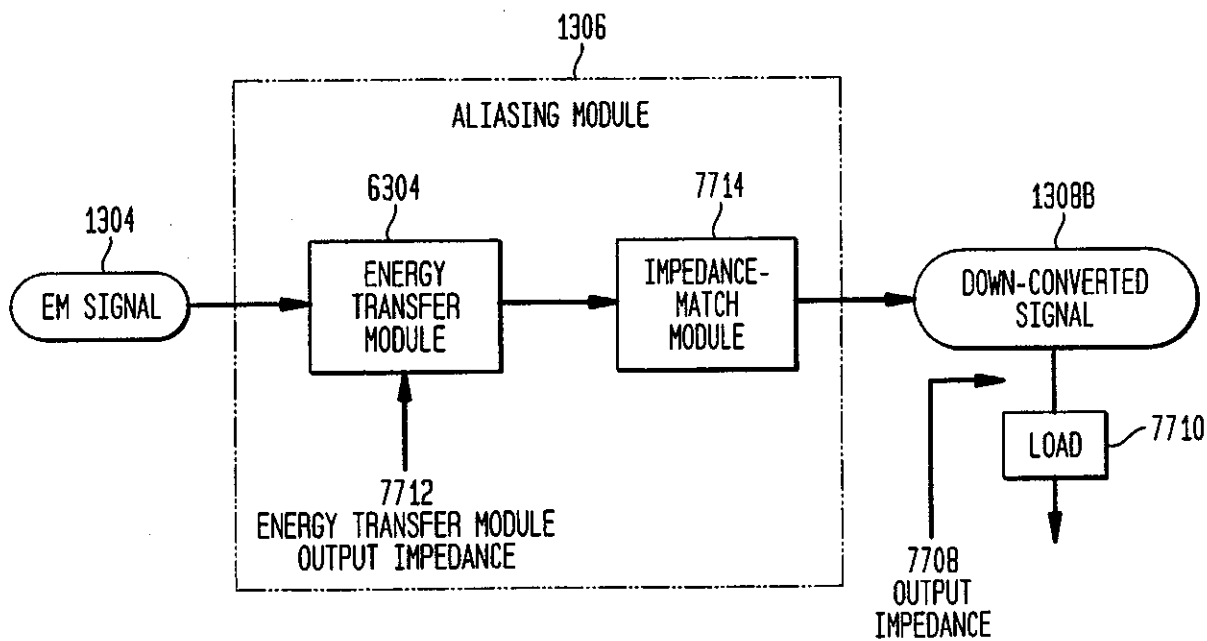
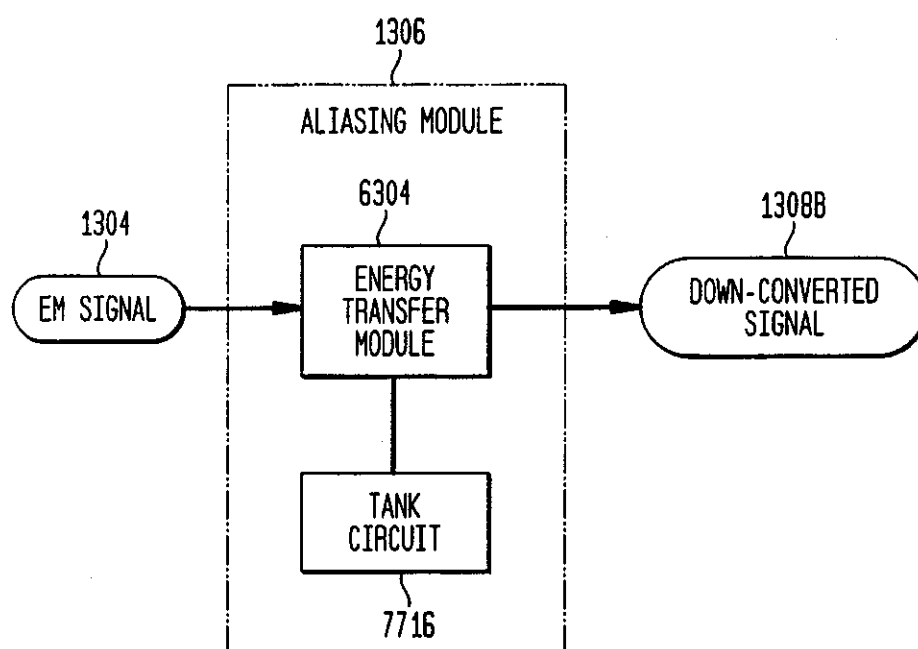


FIG. 77B



95/283

FIG. 77C



96/283

FIG. 78A

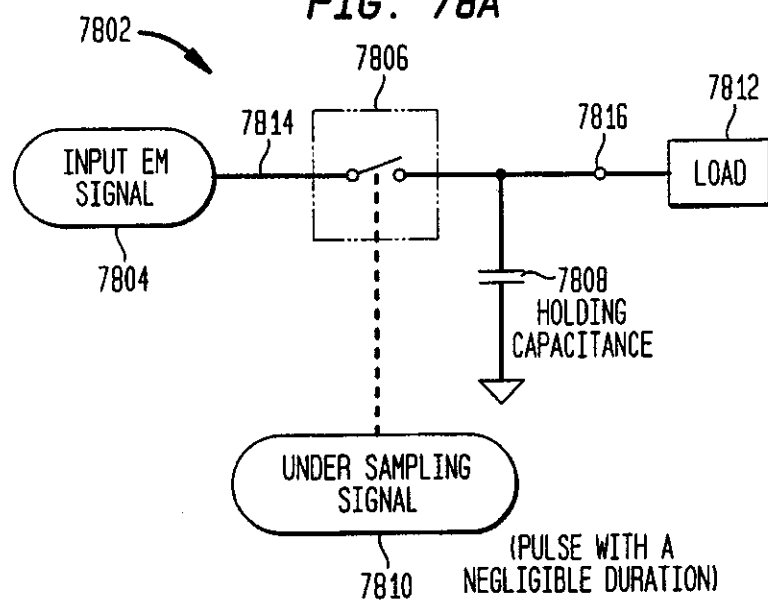
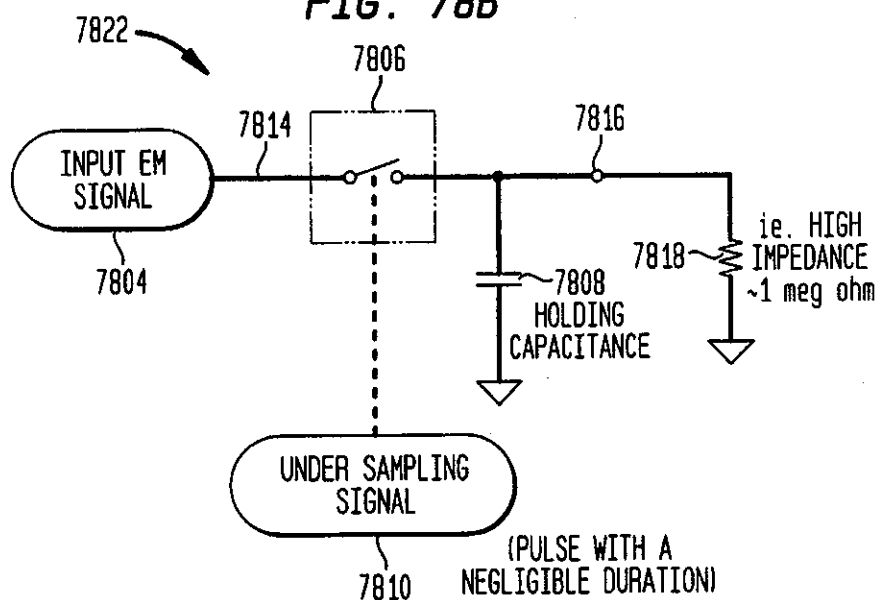


FIG. 78B



97/283

FIG. 79A

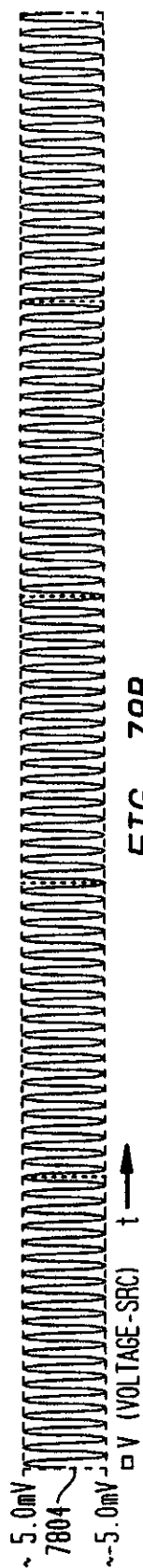


FIG. 79B

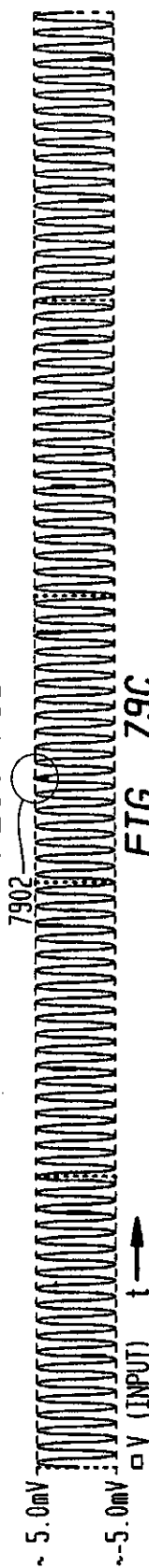


FIG. 79C



FIG. 79D

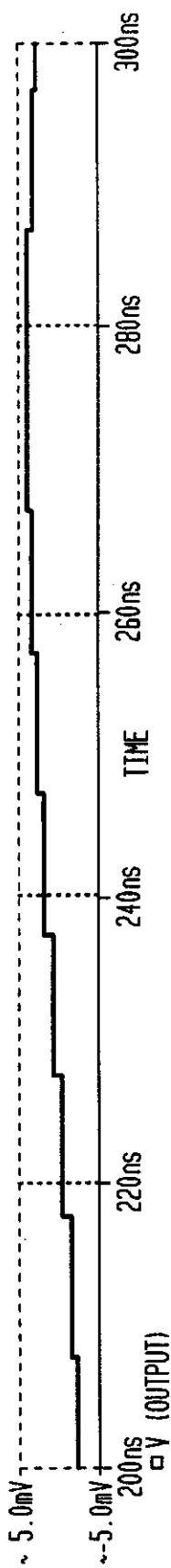


FIG. 79E

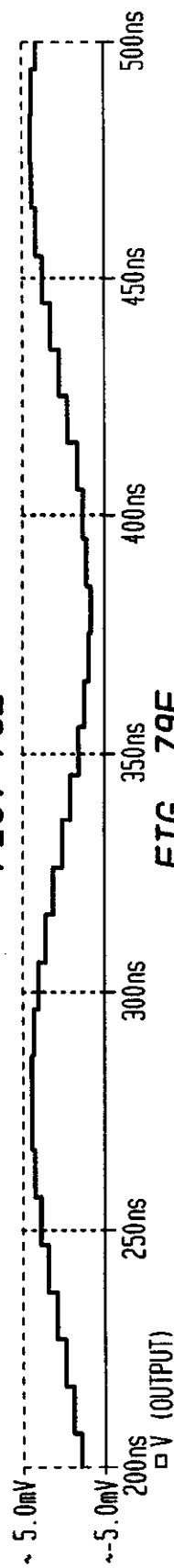


FIG. 79F

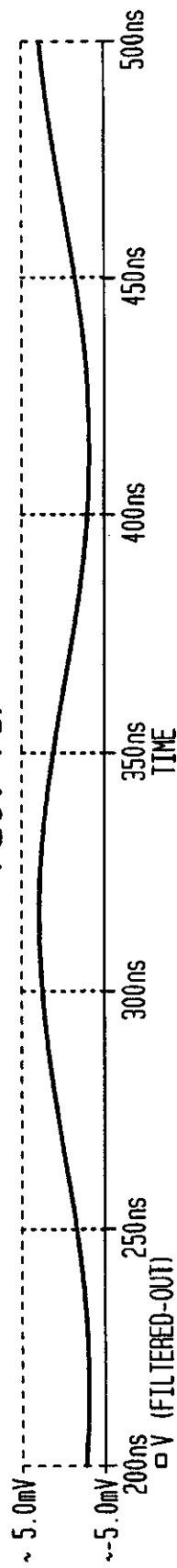


FIG. 80A

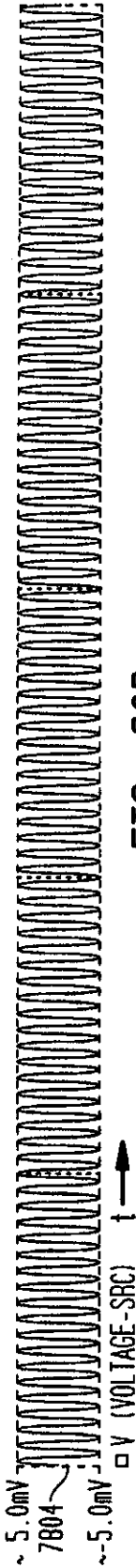


FIG. 80B

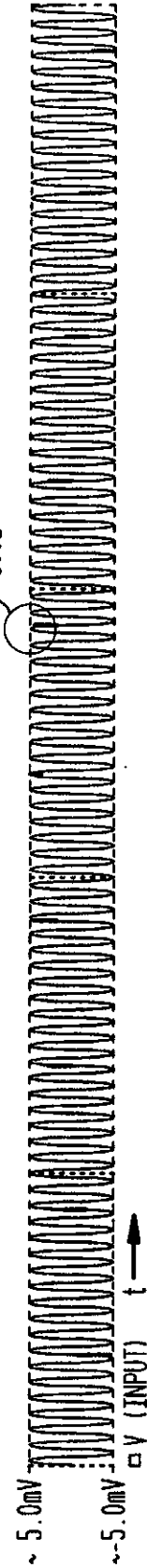


FIG. 80C

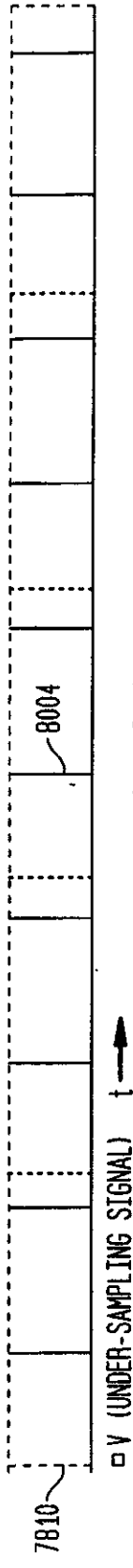


FIG. 80D

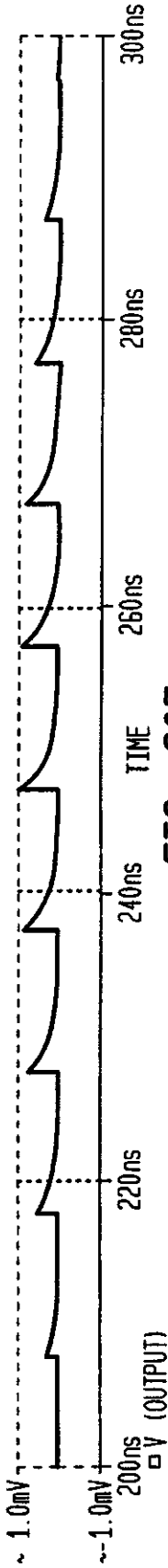


FIG. 80E

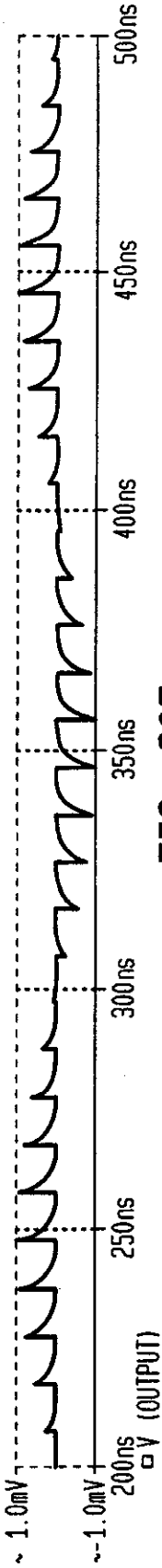
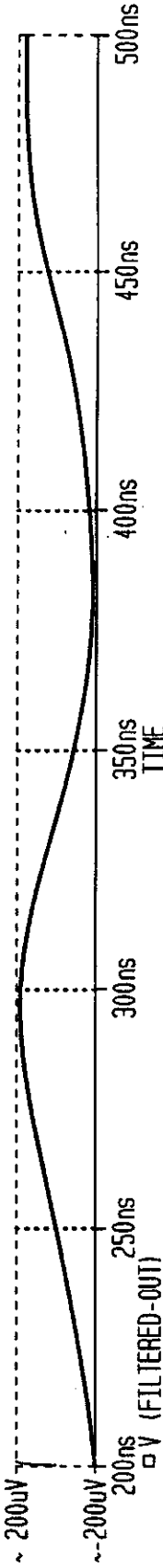


FIG. 80F



99/283

FIG. 81A



FIG. 81B

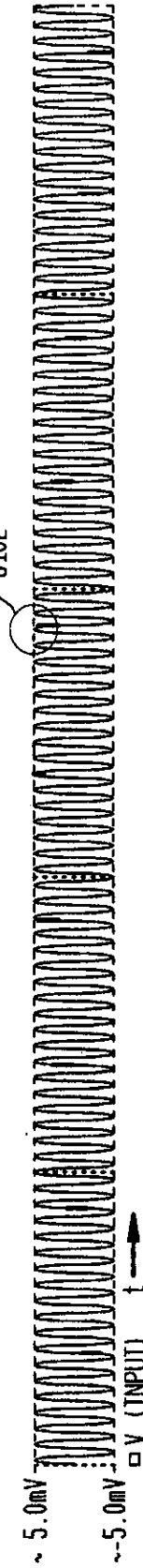


FIG. 81C

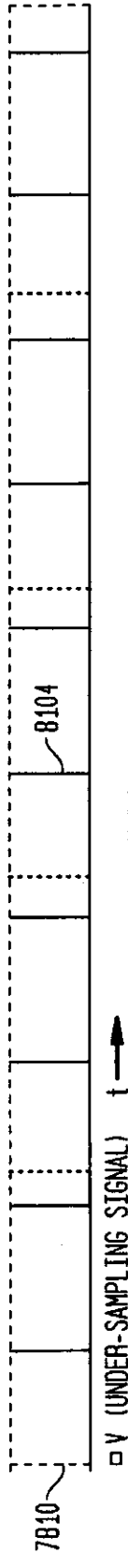


FIG. 81D

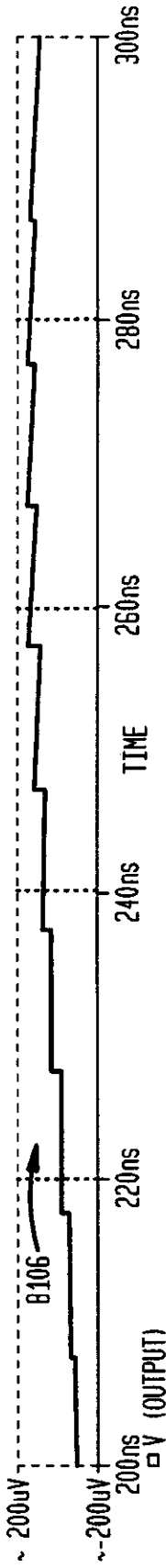


FIG. 81E

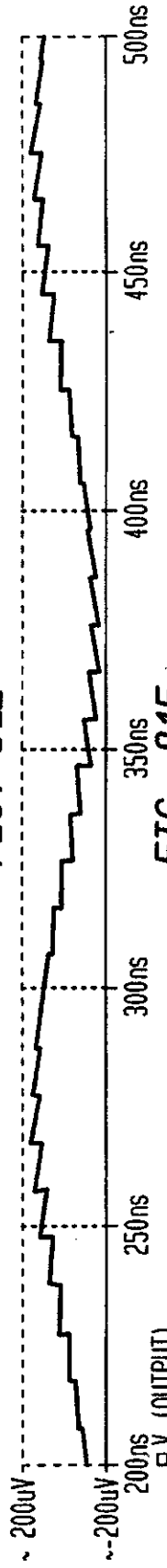
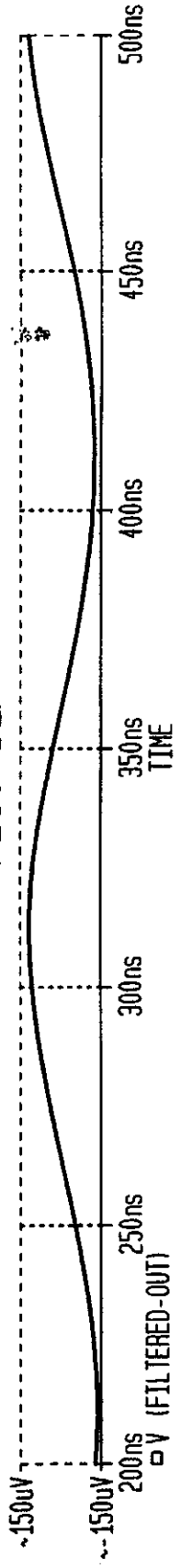


FIG. 81F



100/283

FIG. 82A

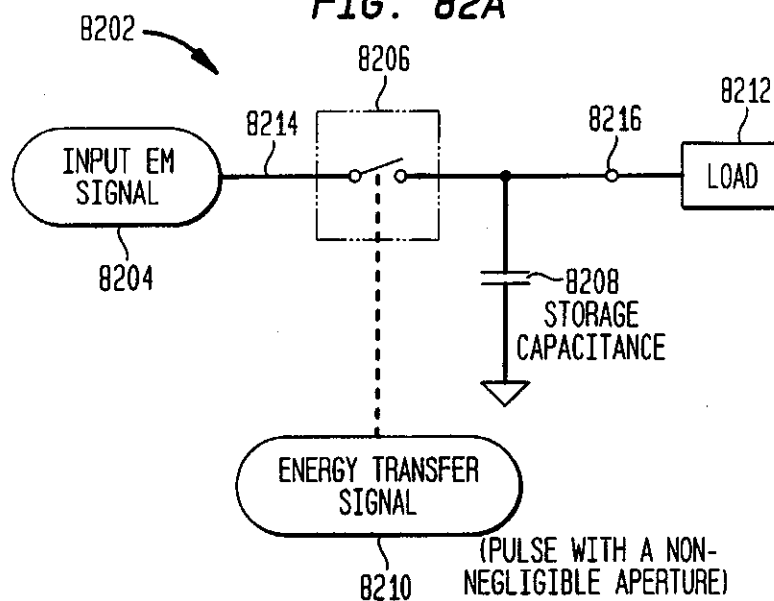
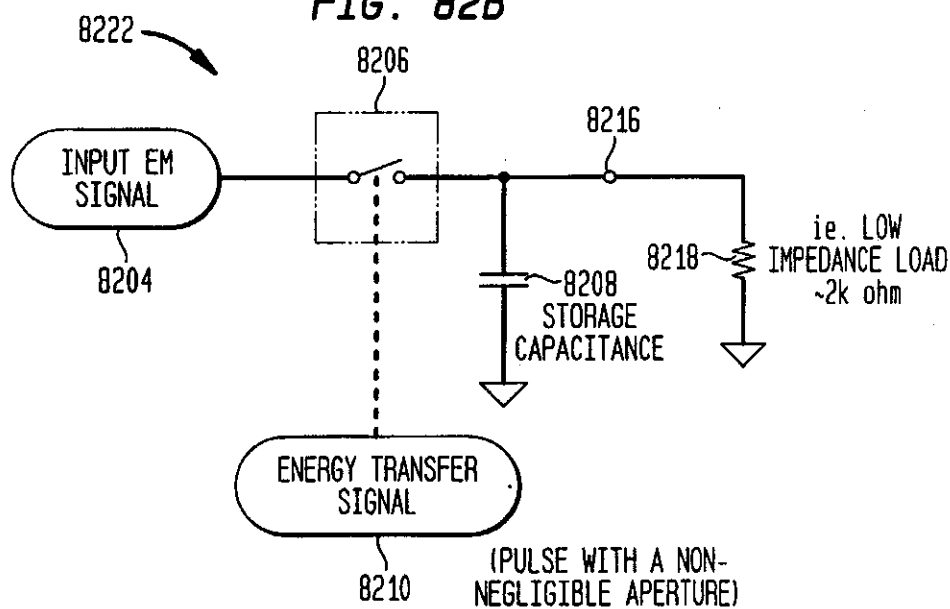


FIG. 82B



101/283

FIG. 83A

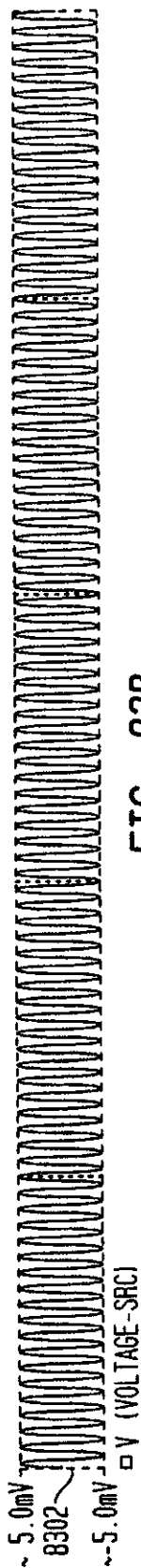


FIG. 83B

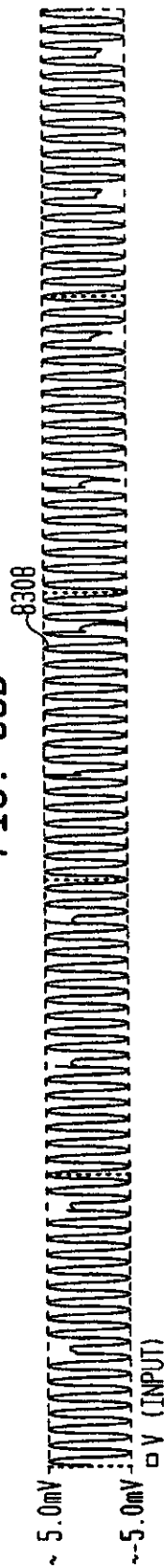


FIG. 83C

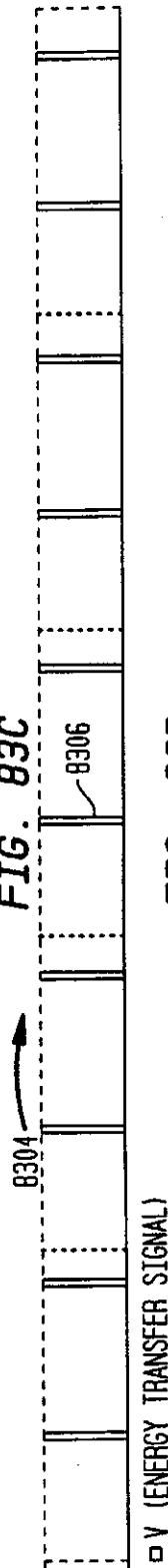


FIG. 83D

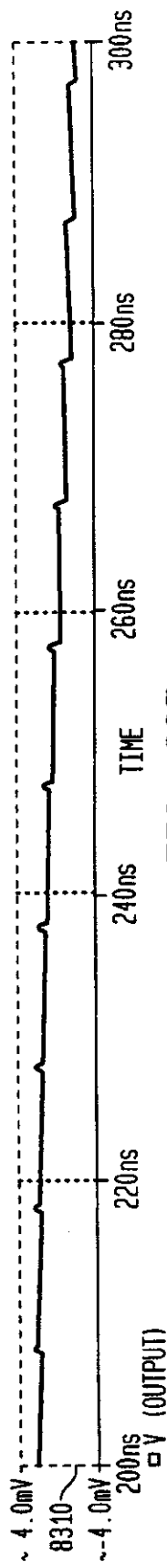


FIG. 83E

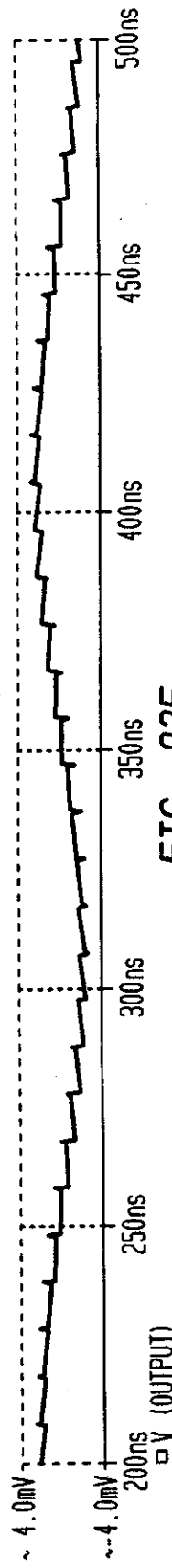
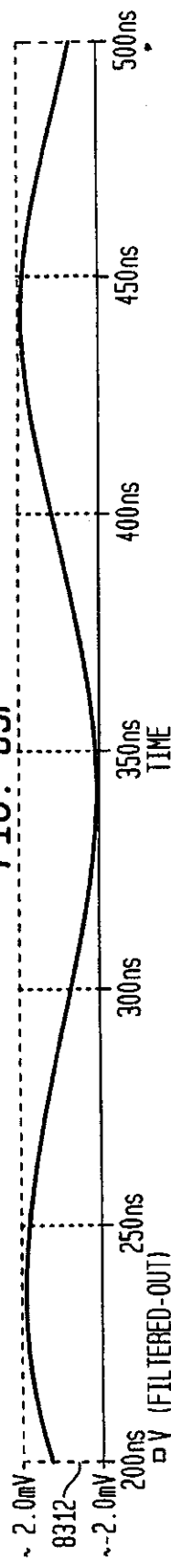


FIG. 83F



102/283

FIG. 84A

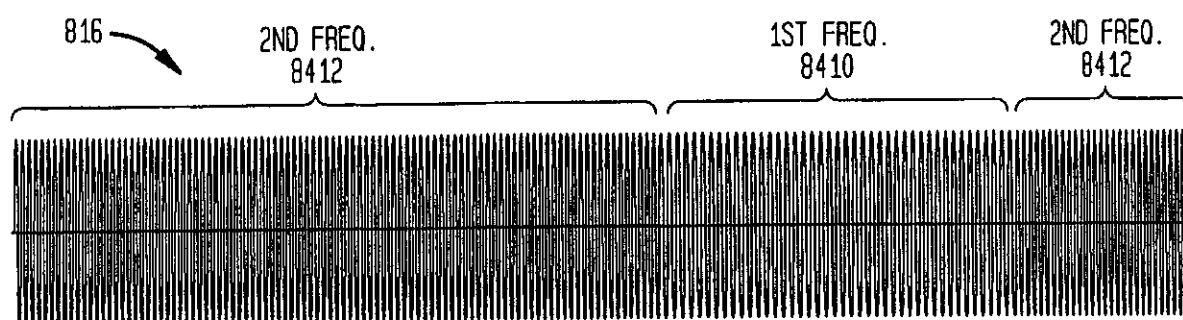


FIG. 84B

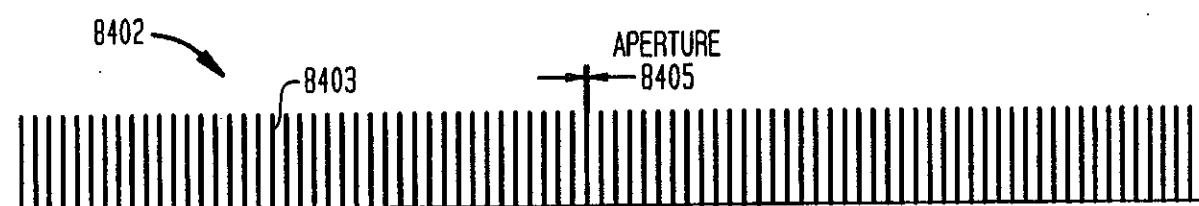


FIG. 84C

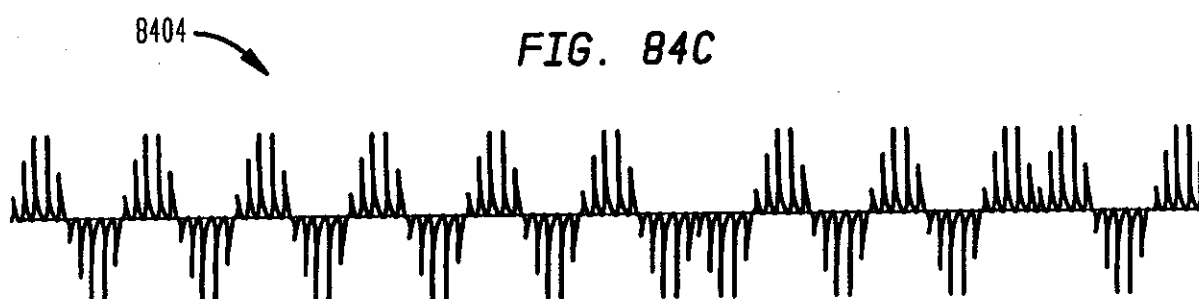


FIG. 84D

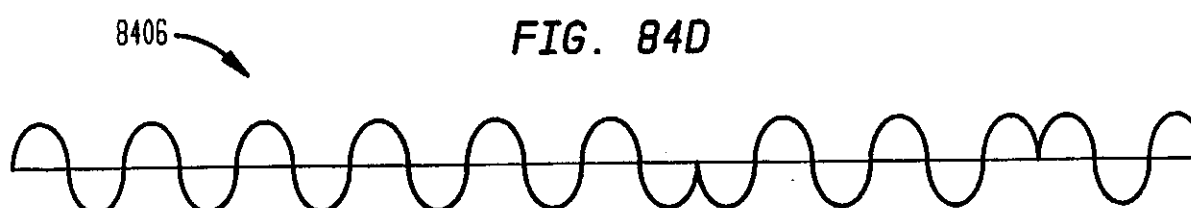


FIG. 85A

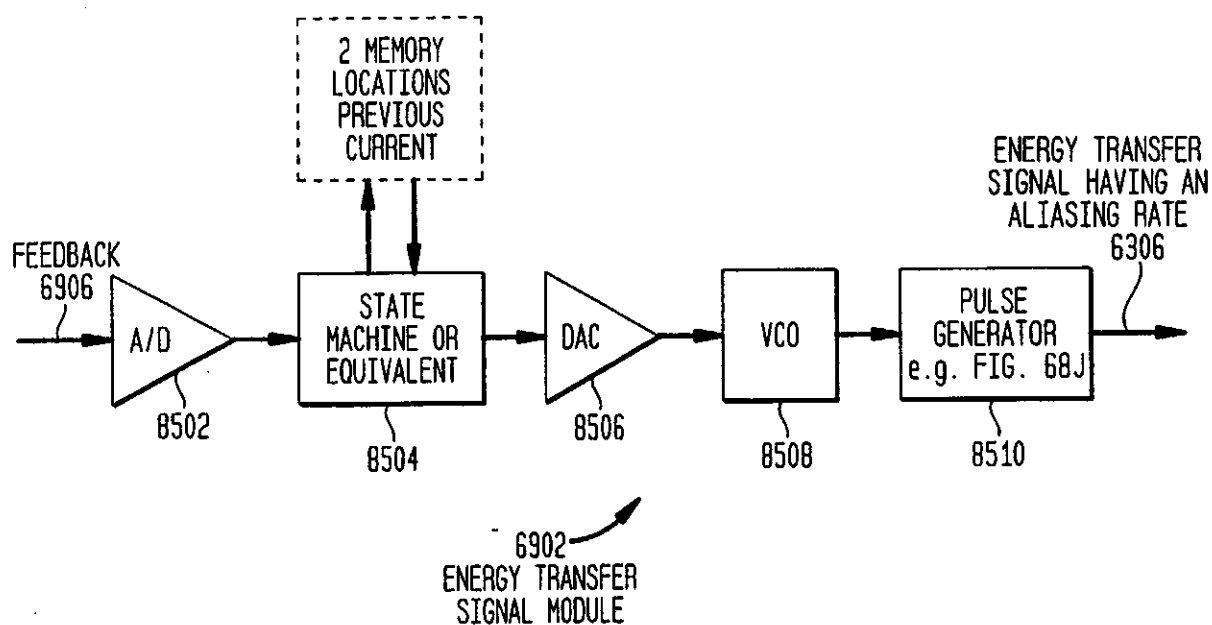
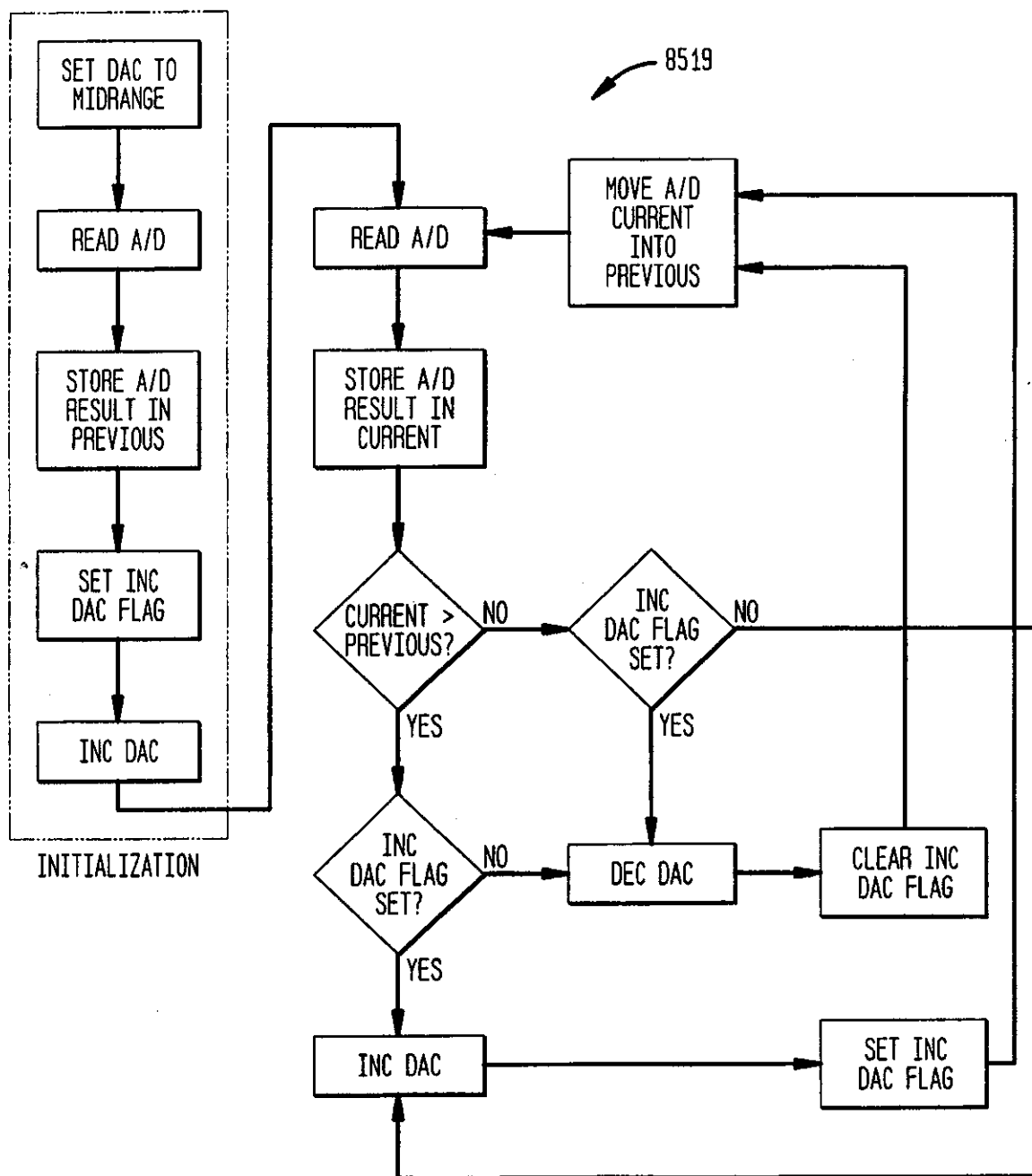
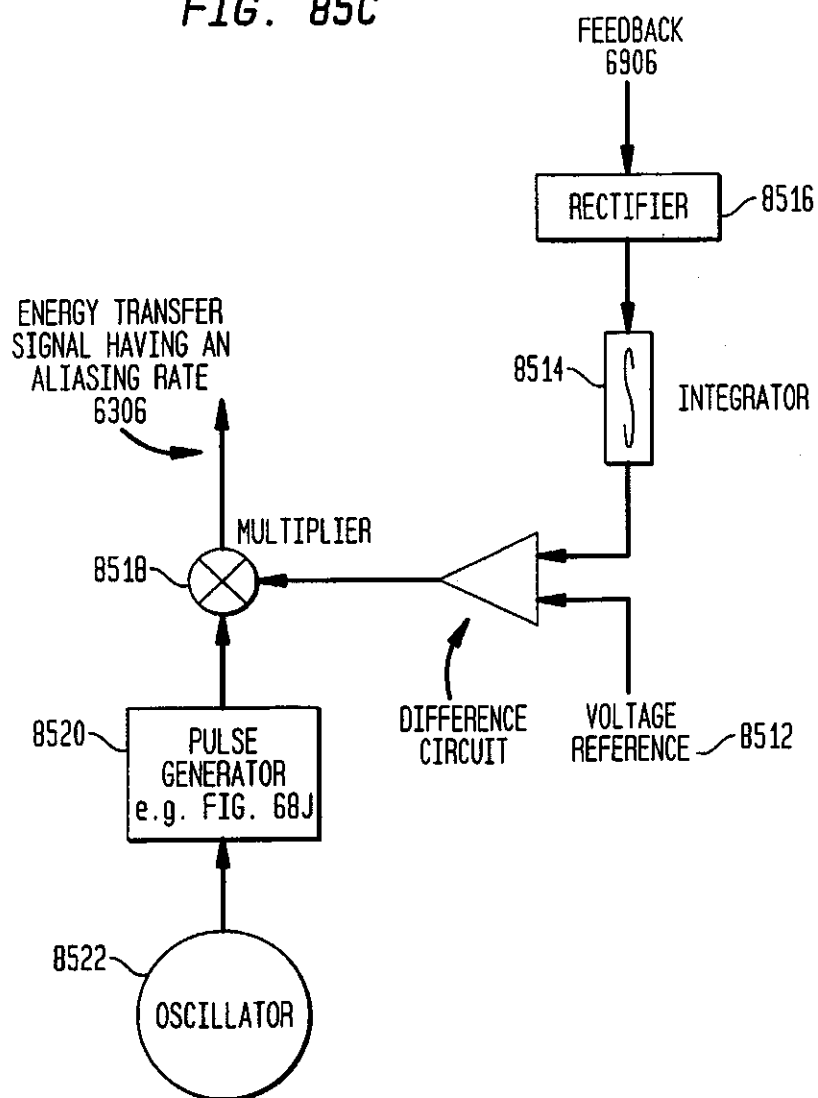


FIG. 85B



STATE MACHINE FLOWCHART

FIG. 85C



ENERGY TRANSFER SIGNAL MODULE 6902

FIG. 86

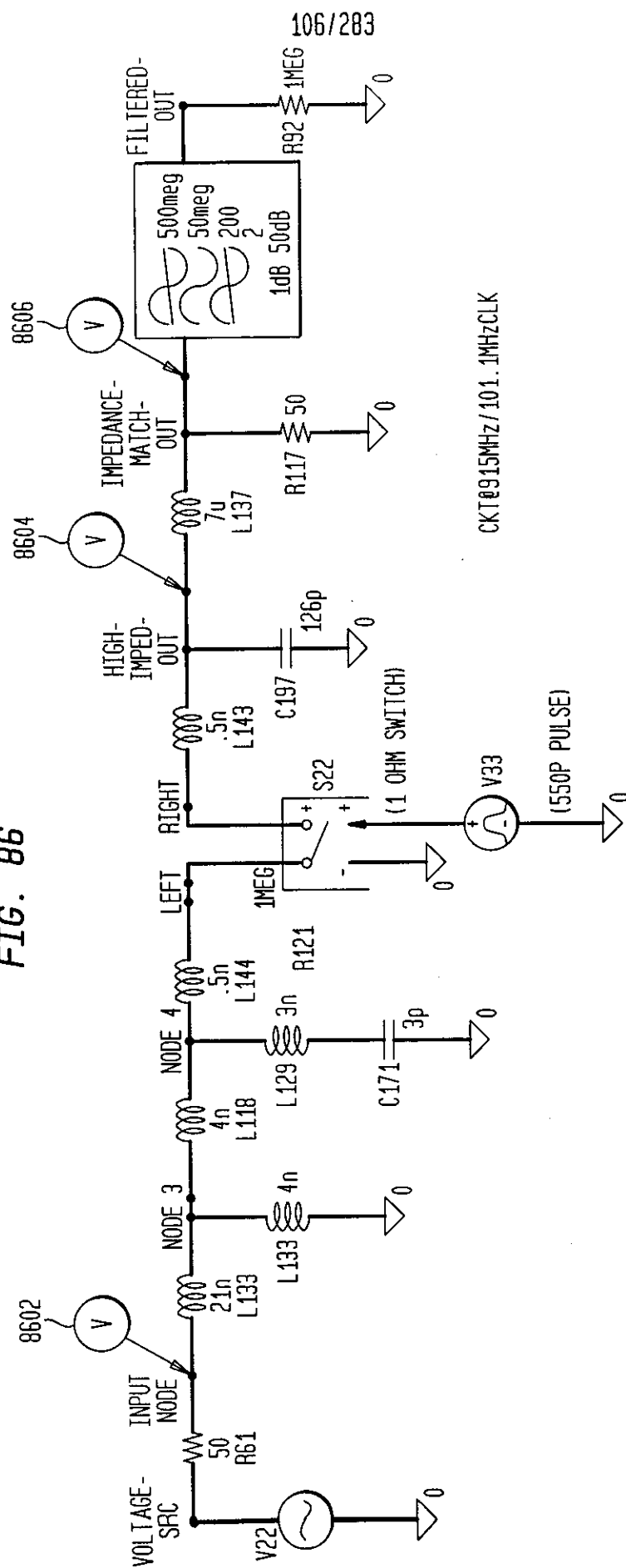


FIG. 87

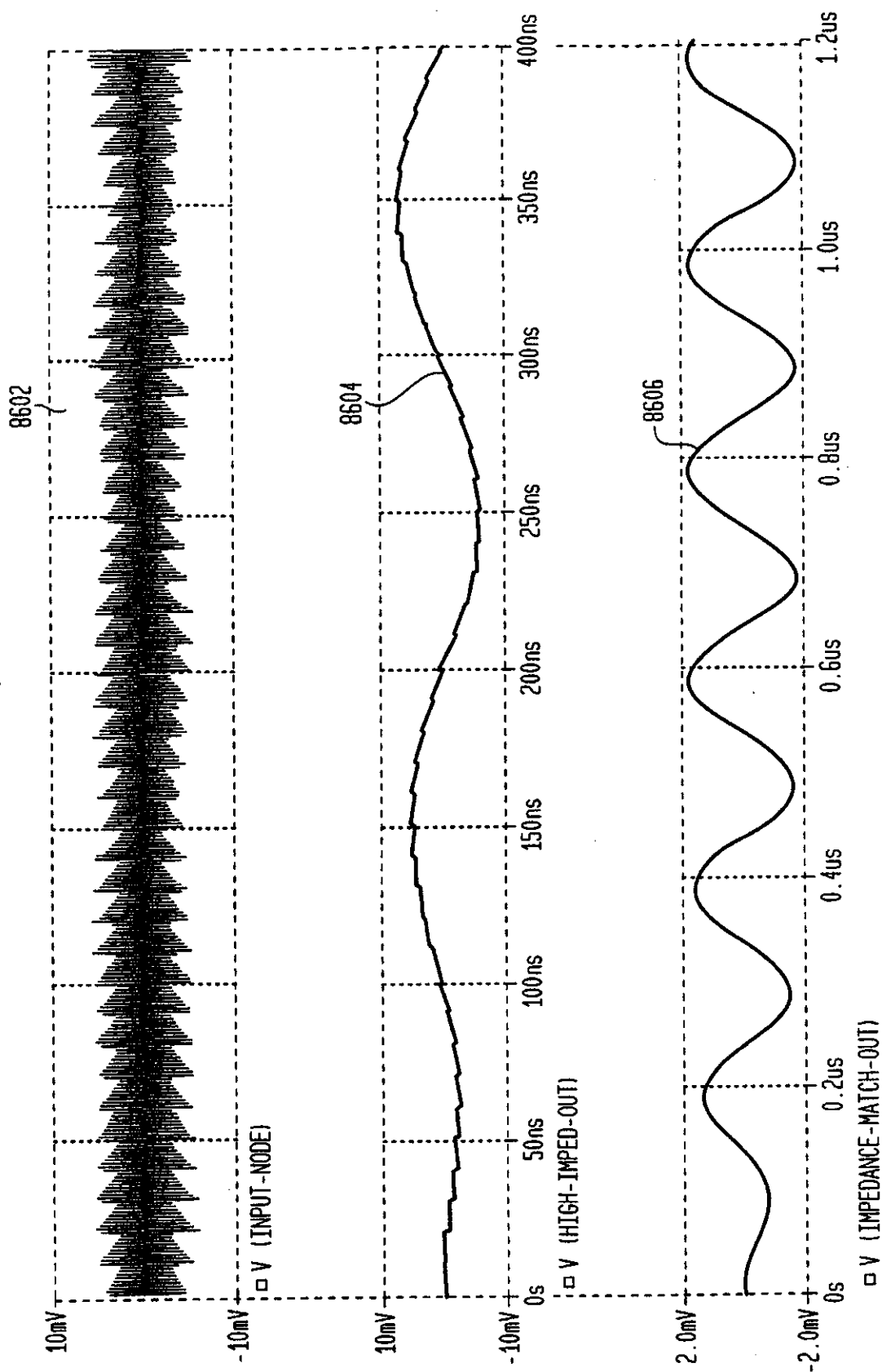


FIG. 88

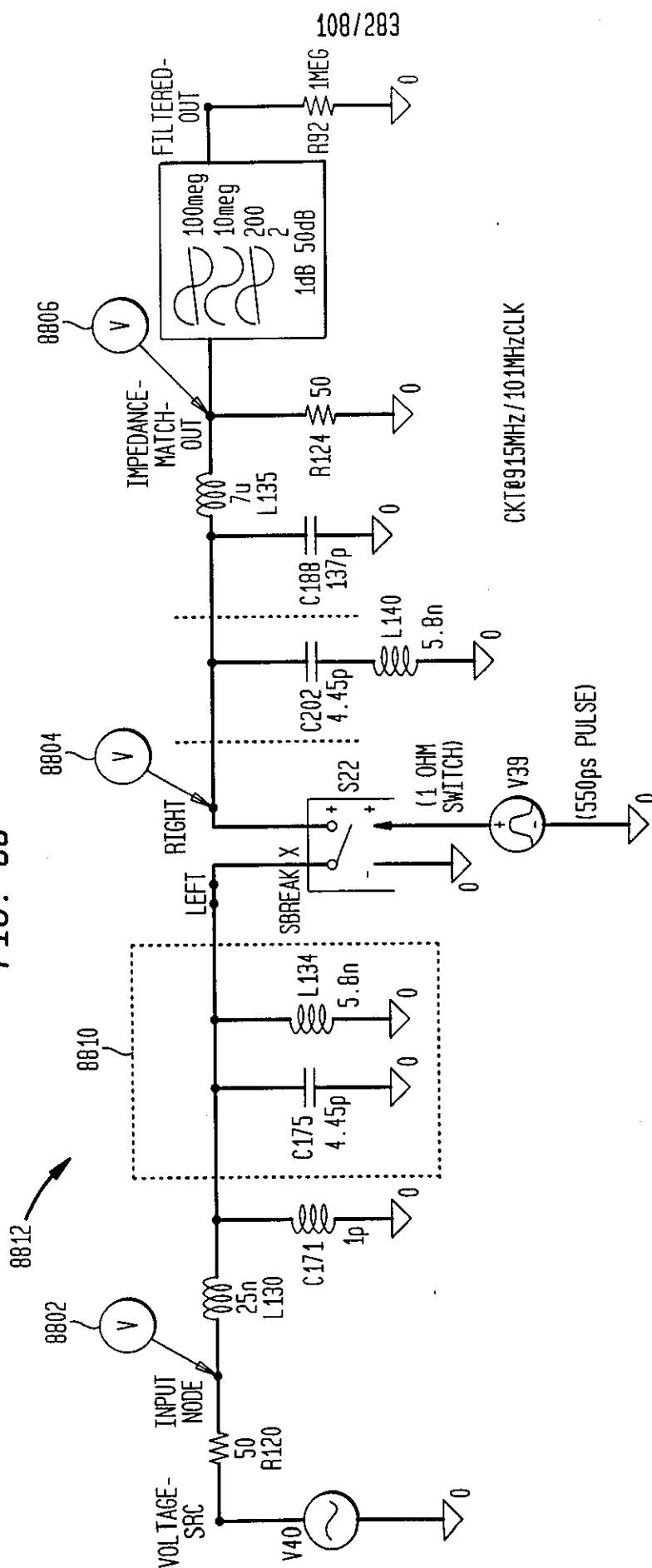


FIG. 89

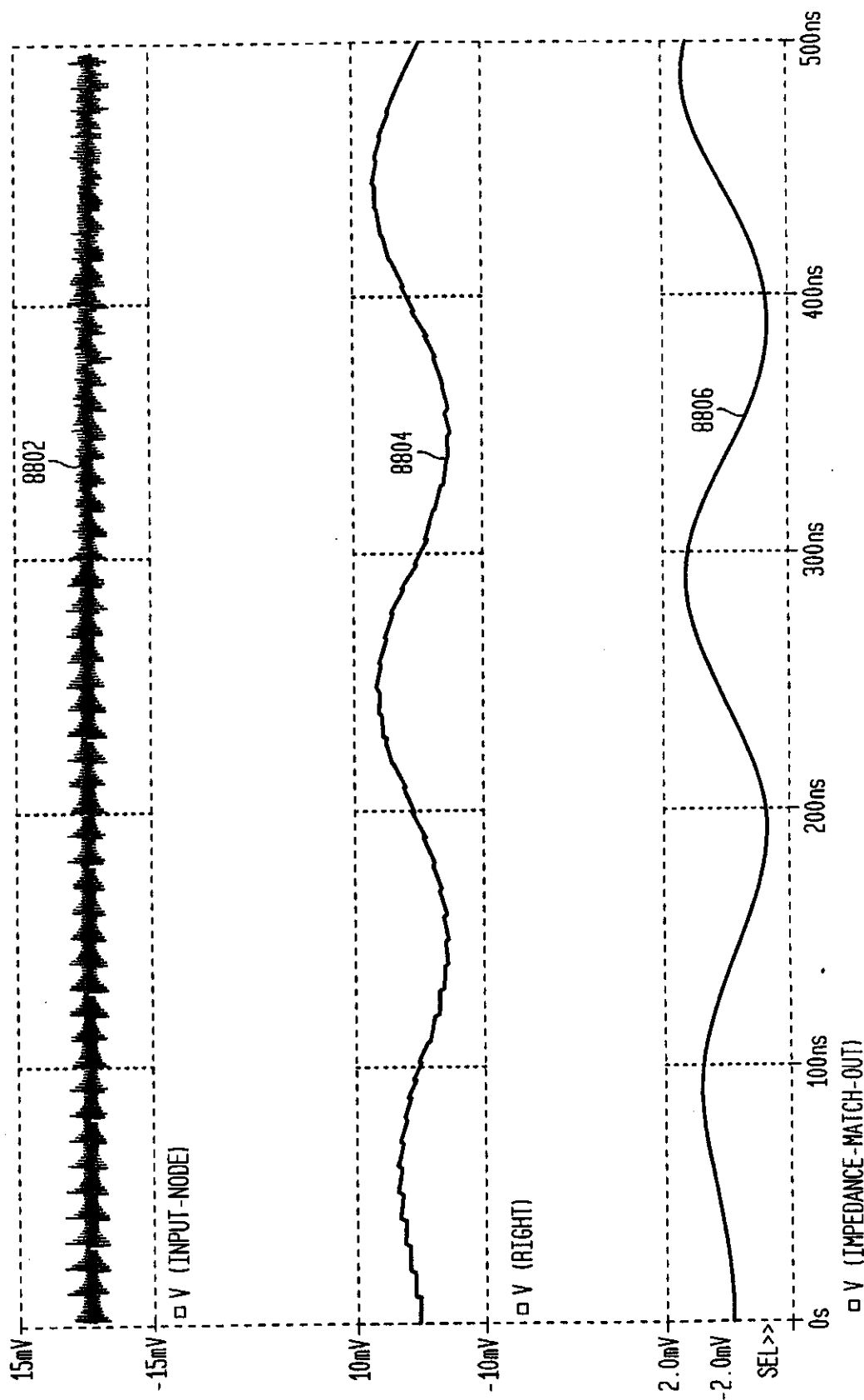


FIG. 90

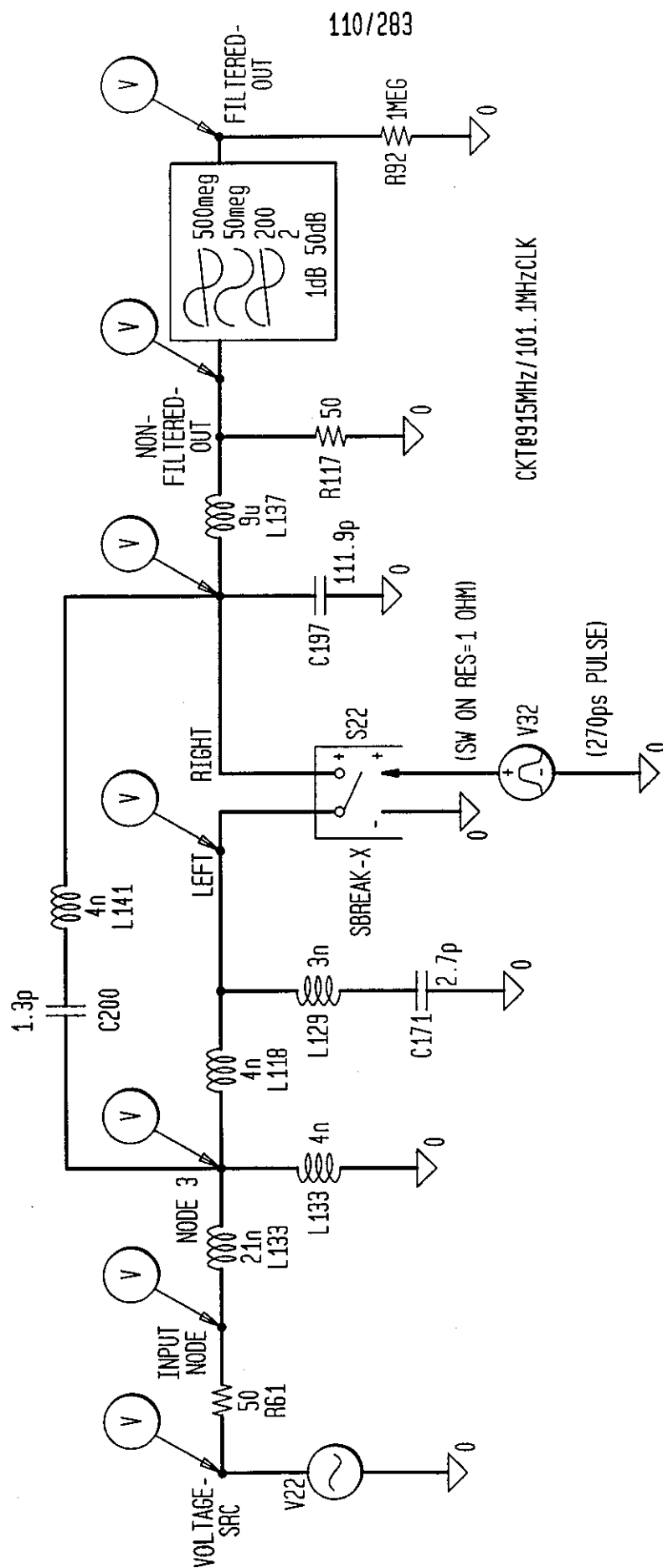
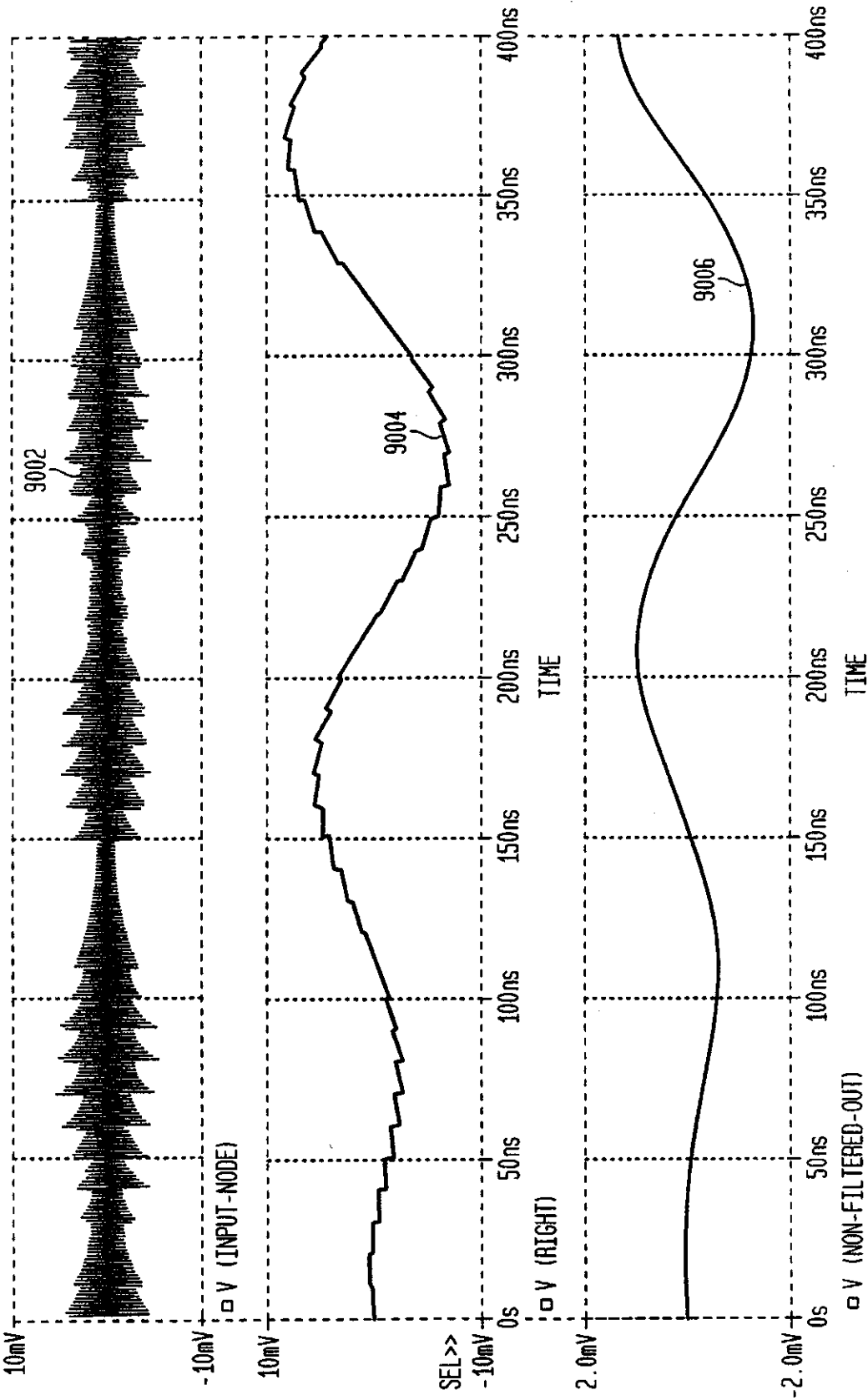


FIG. 91



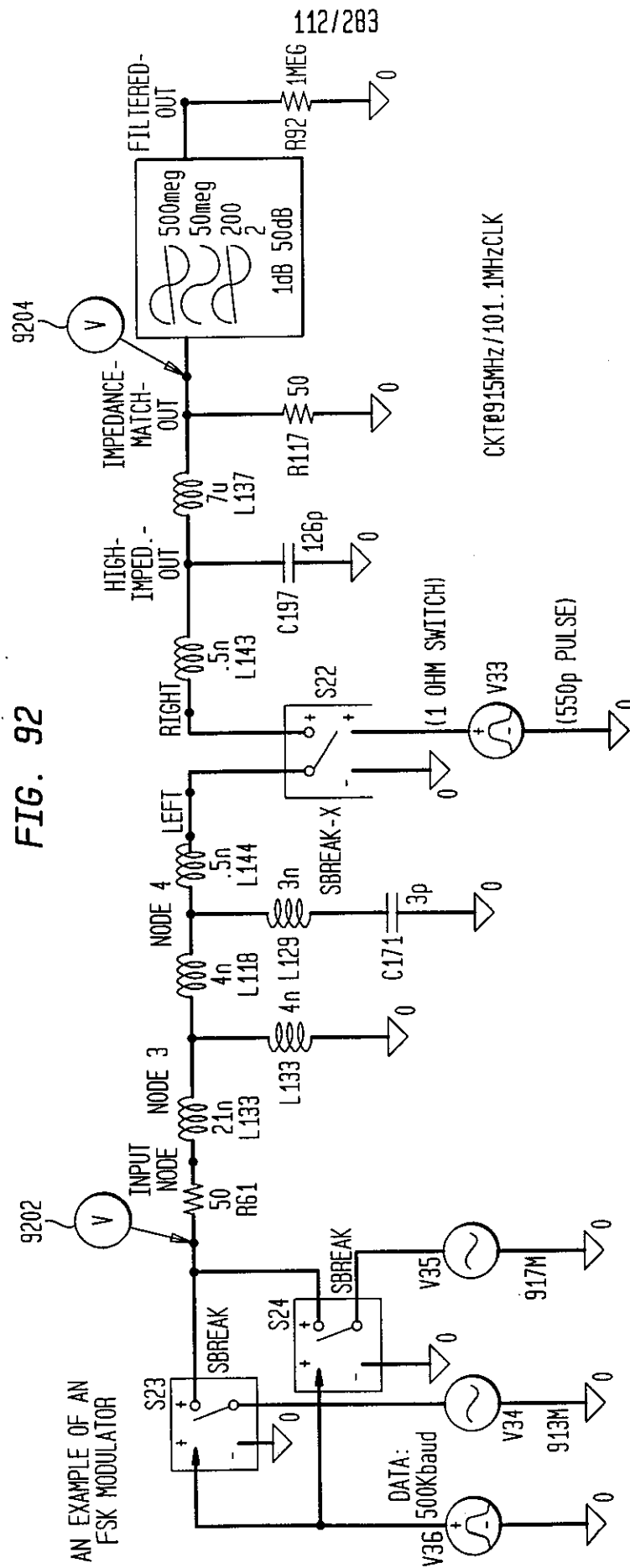
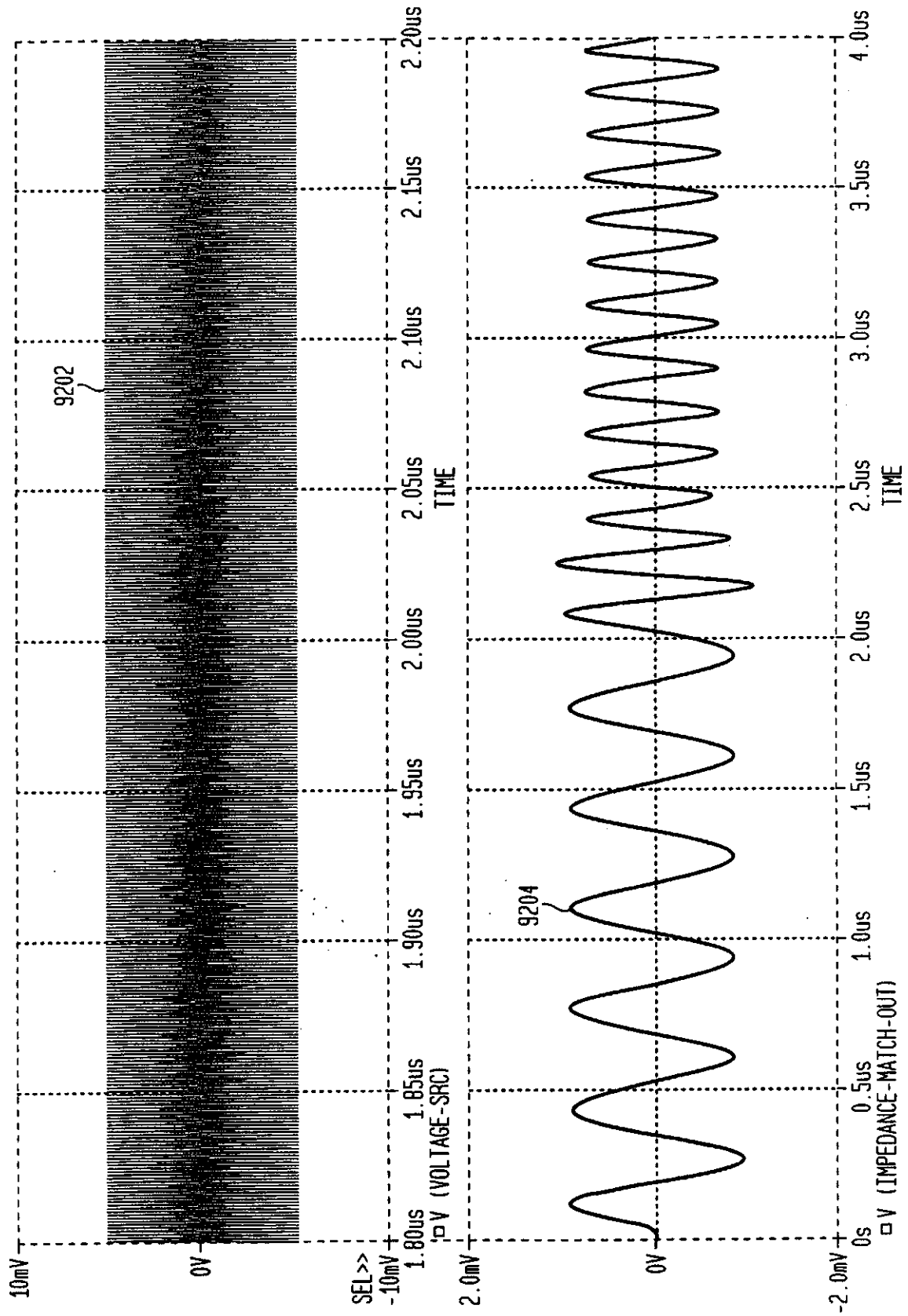


FIG. 93



114/283

FIG. 94A

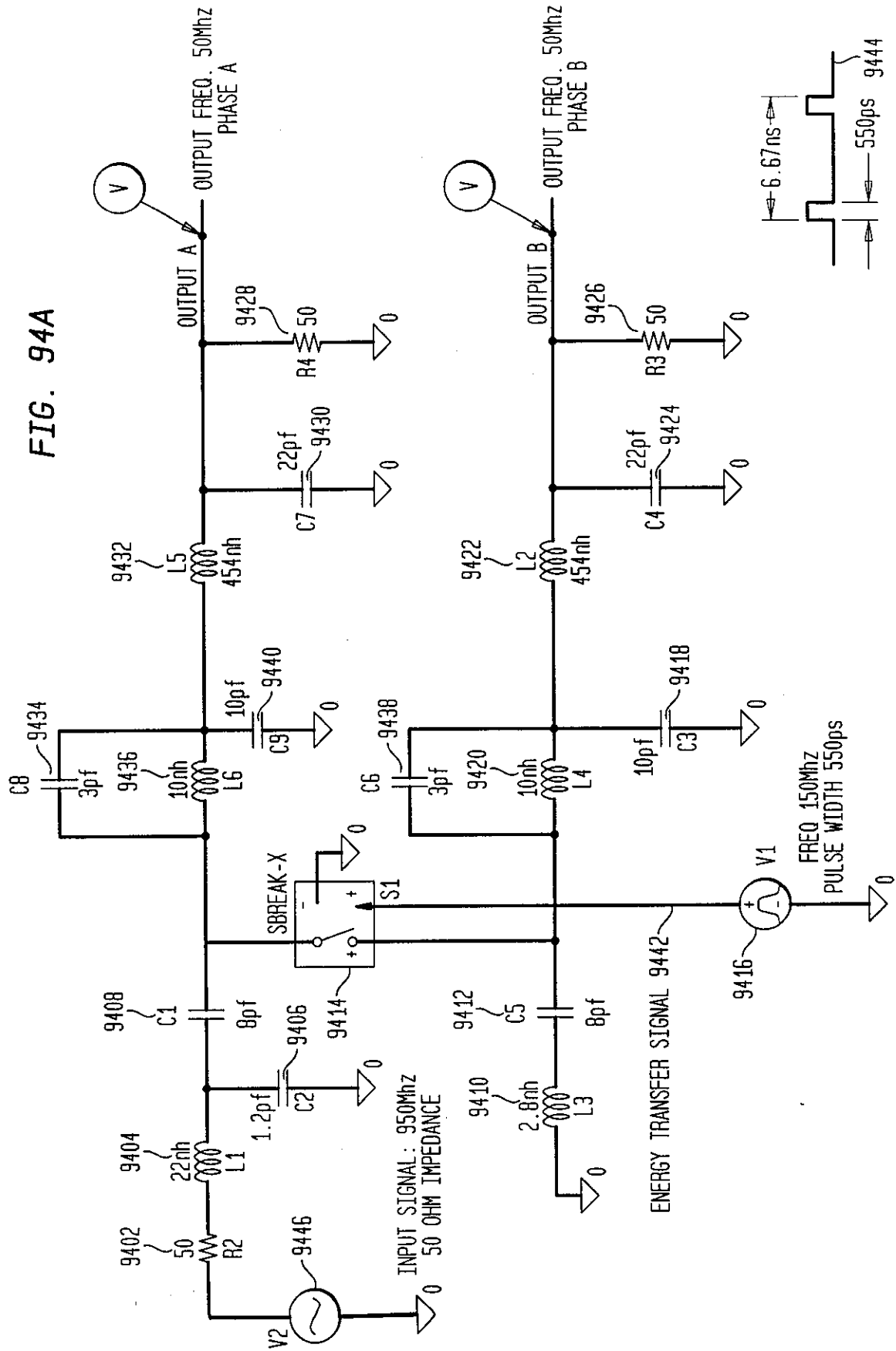


FIG. 94B

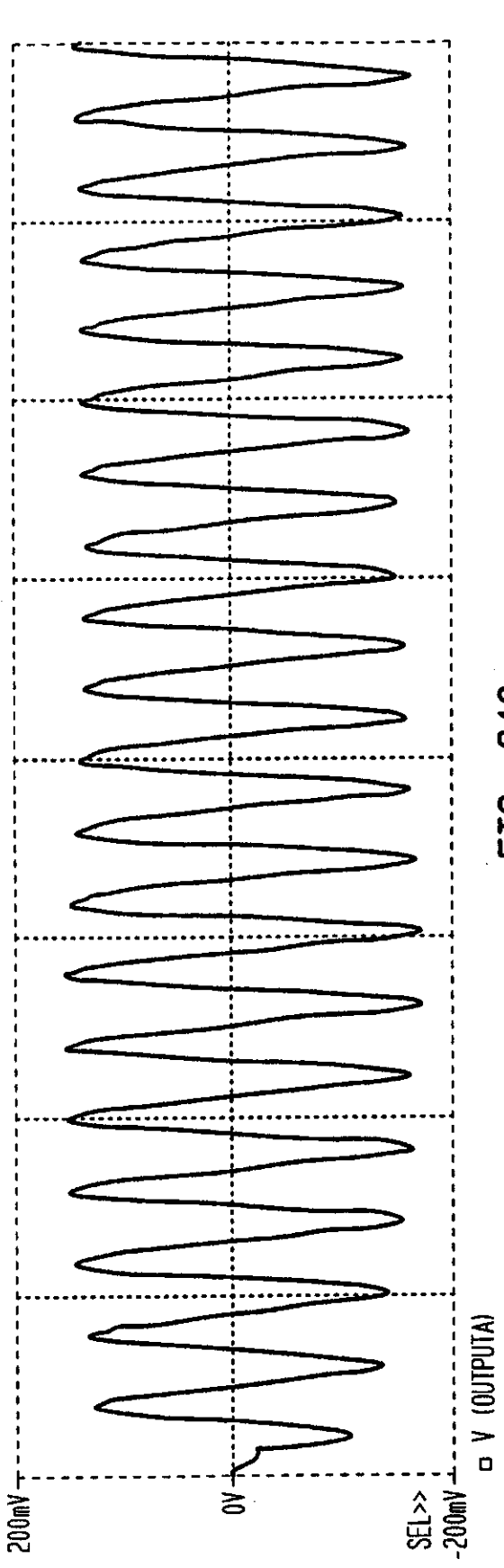


FIG. 94C

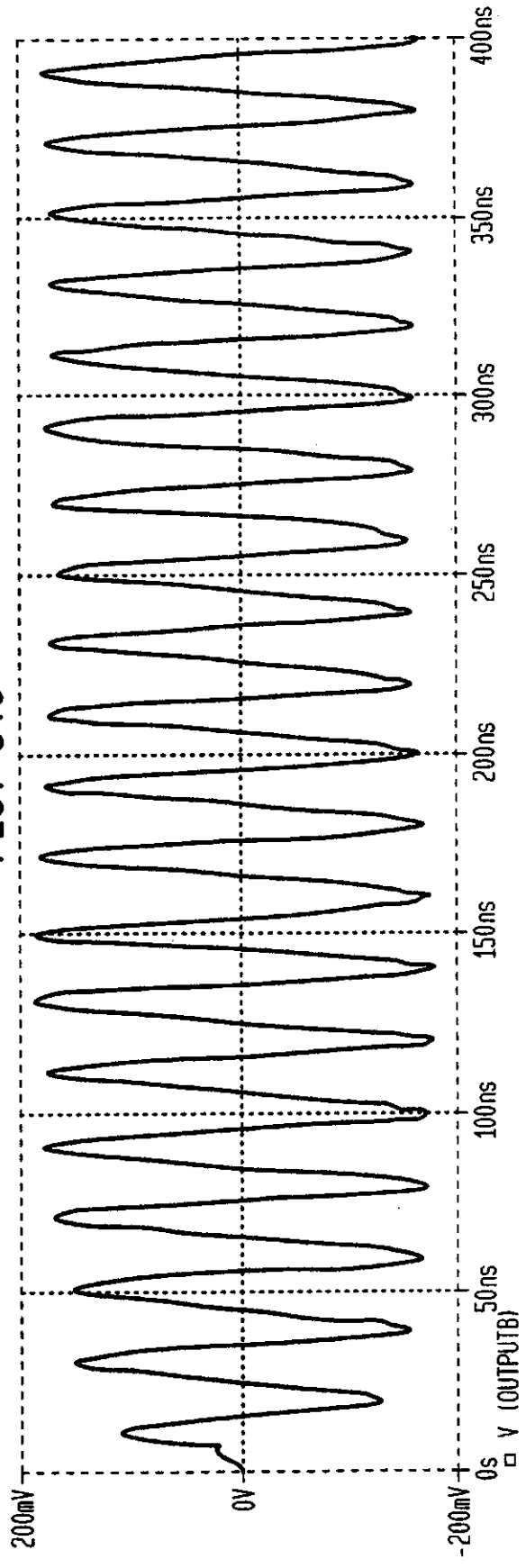
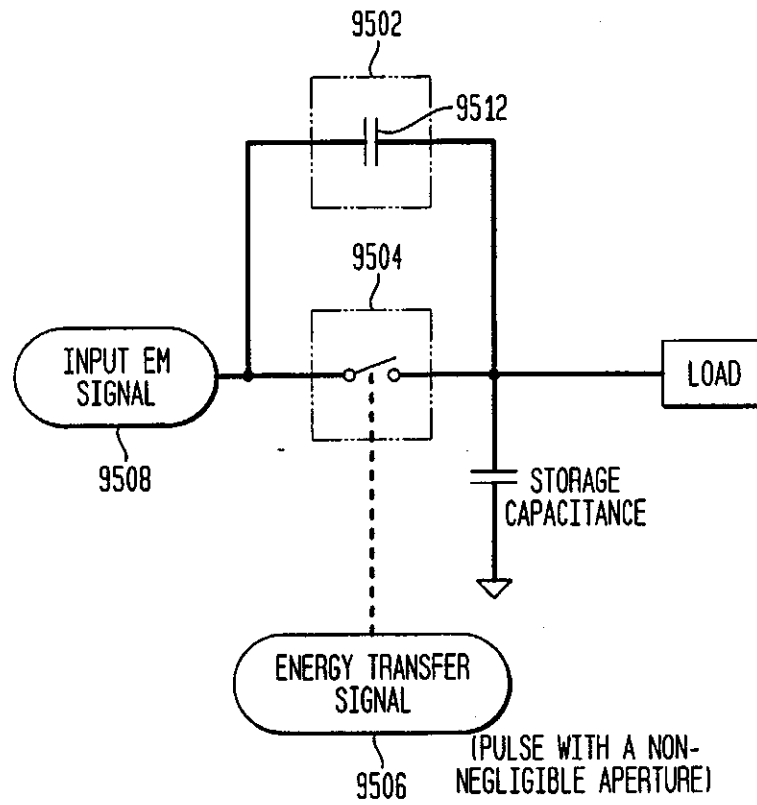
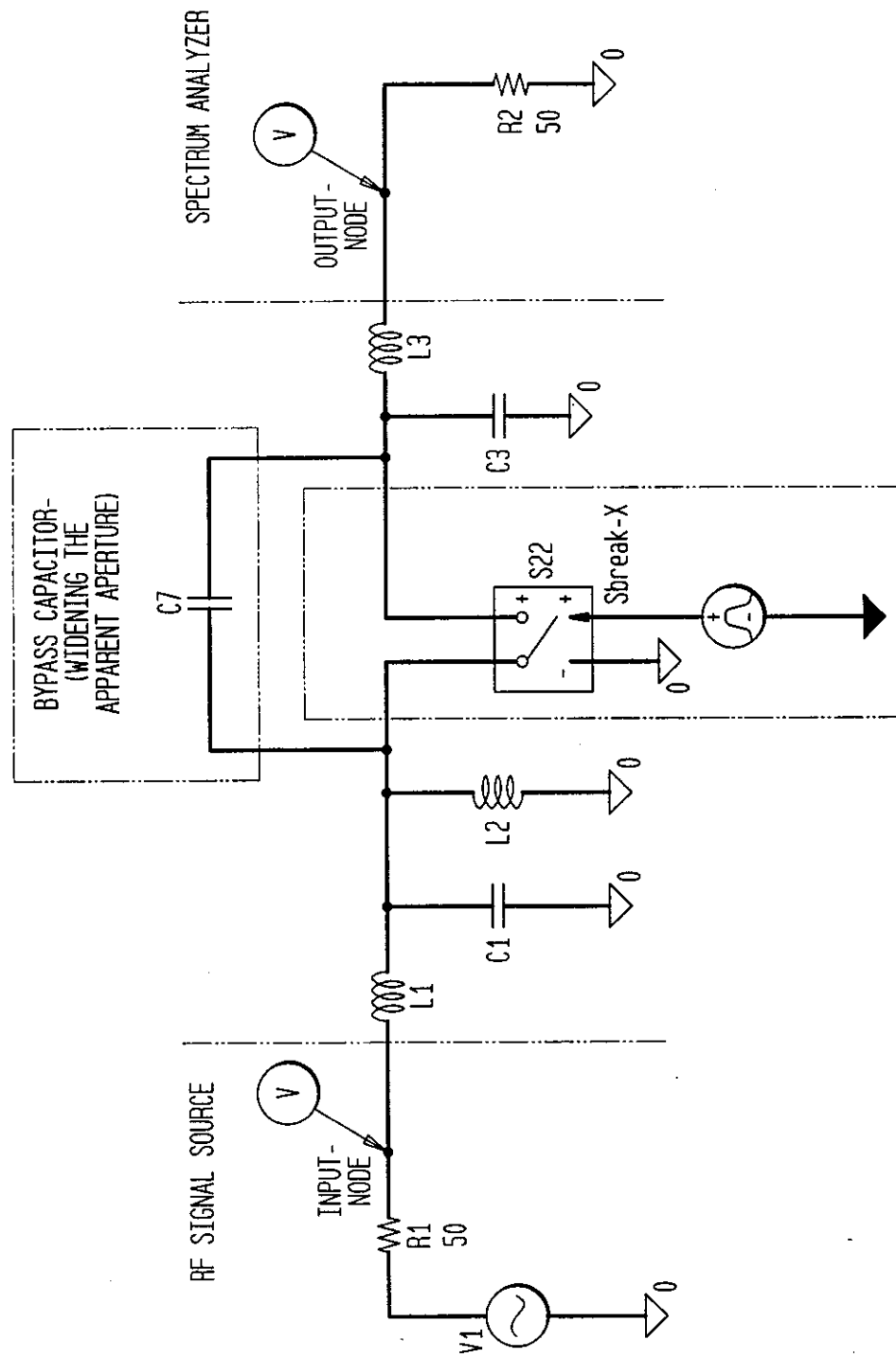


FIG. 95



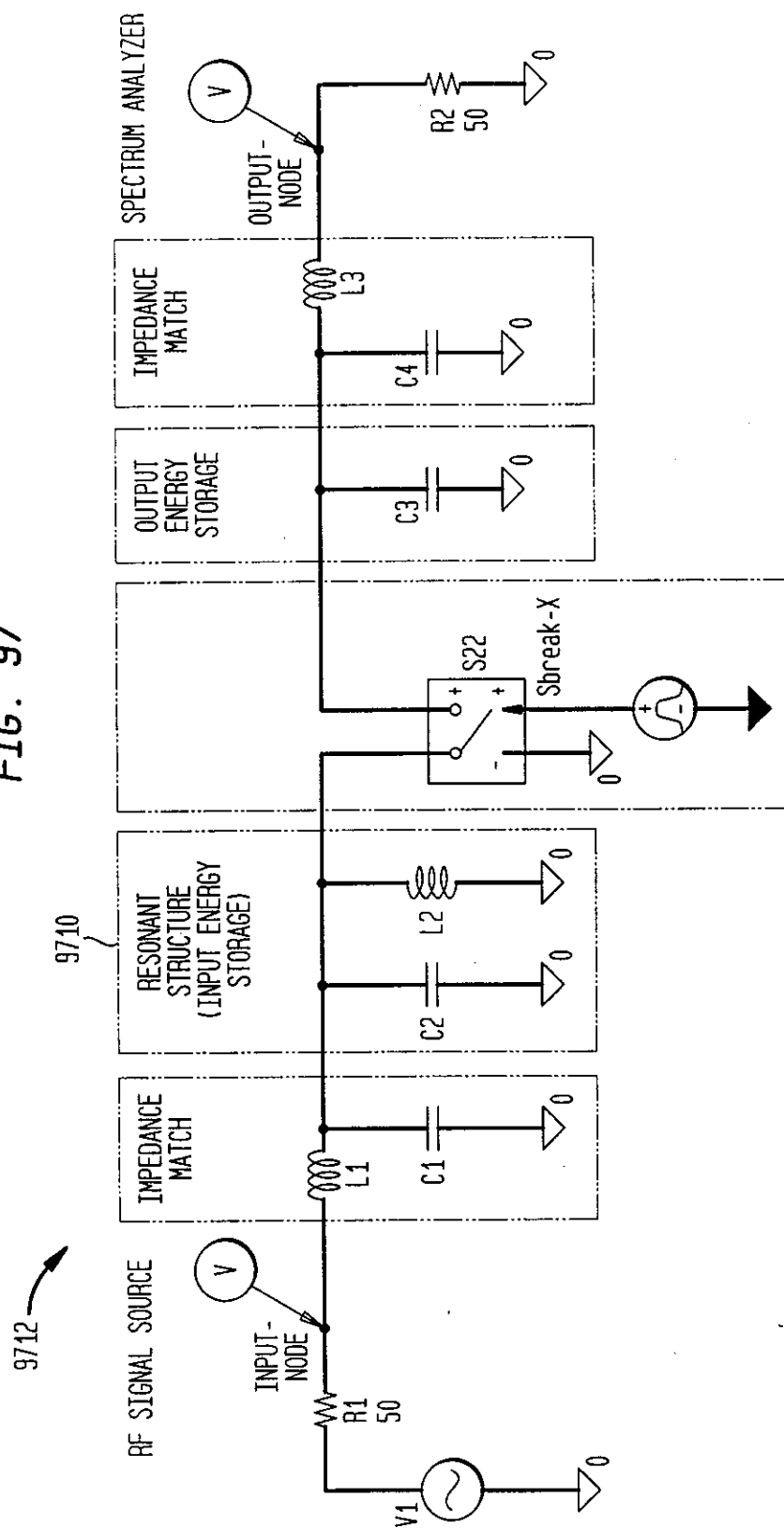
117/283

FIG. 96



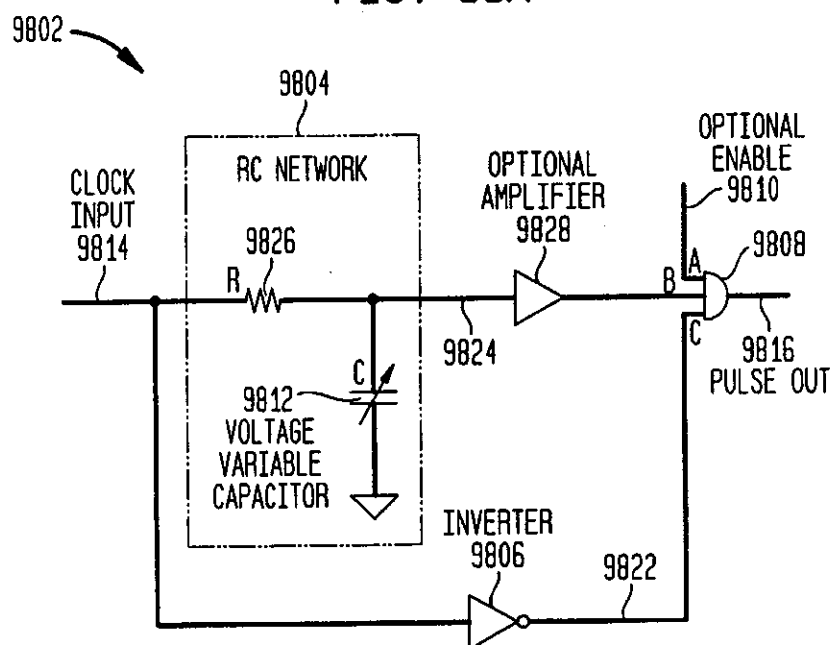
118/283

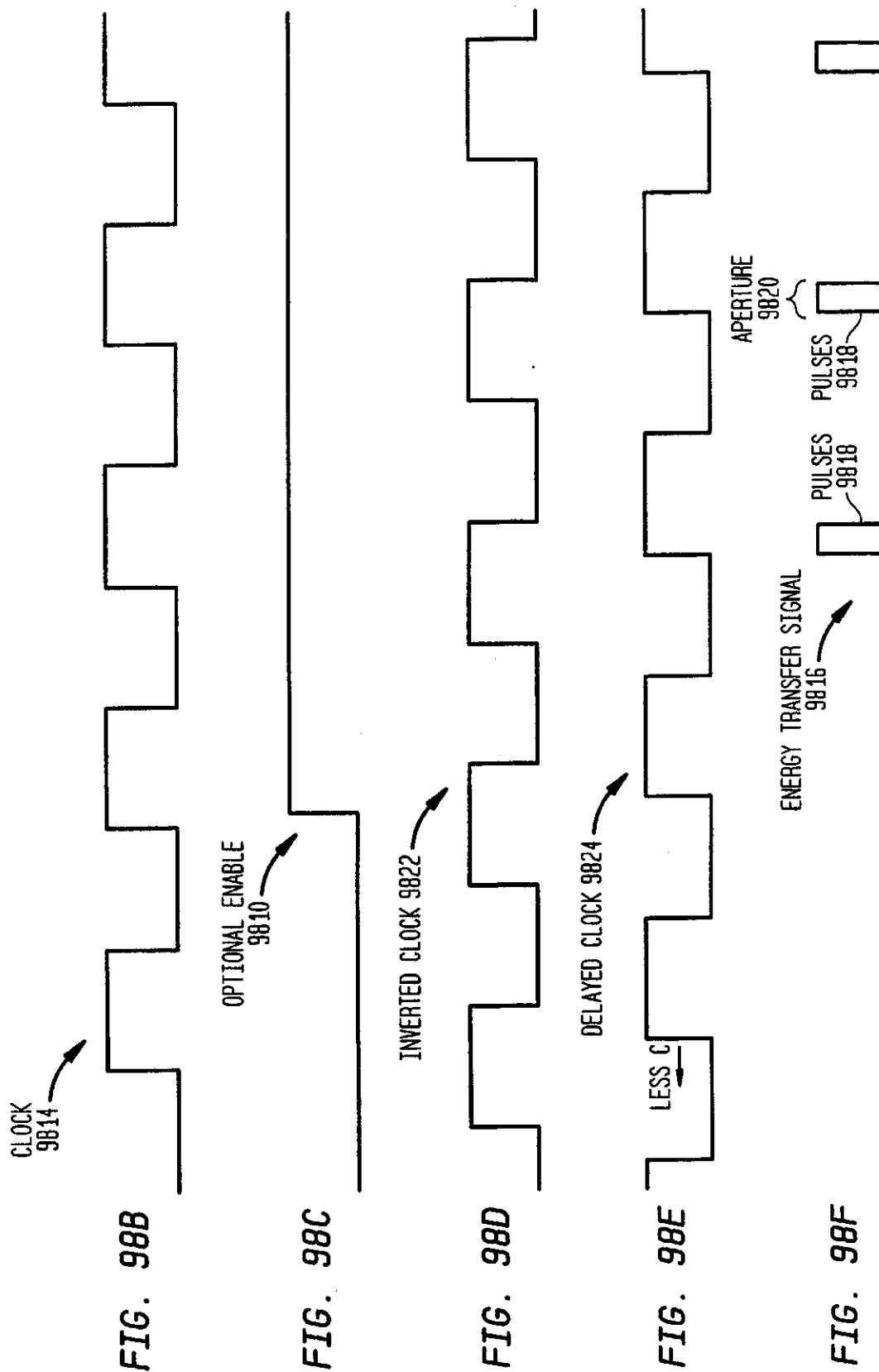
FIG. 97



119/283

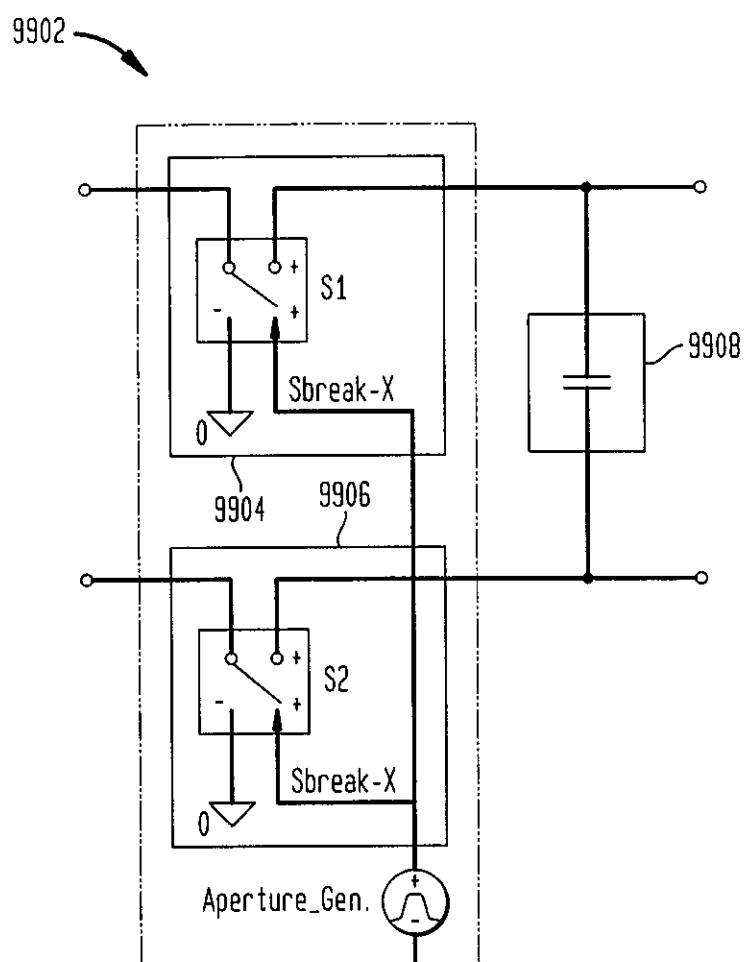
FIG. 98A





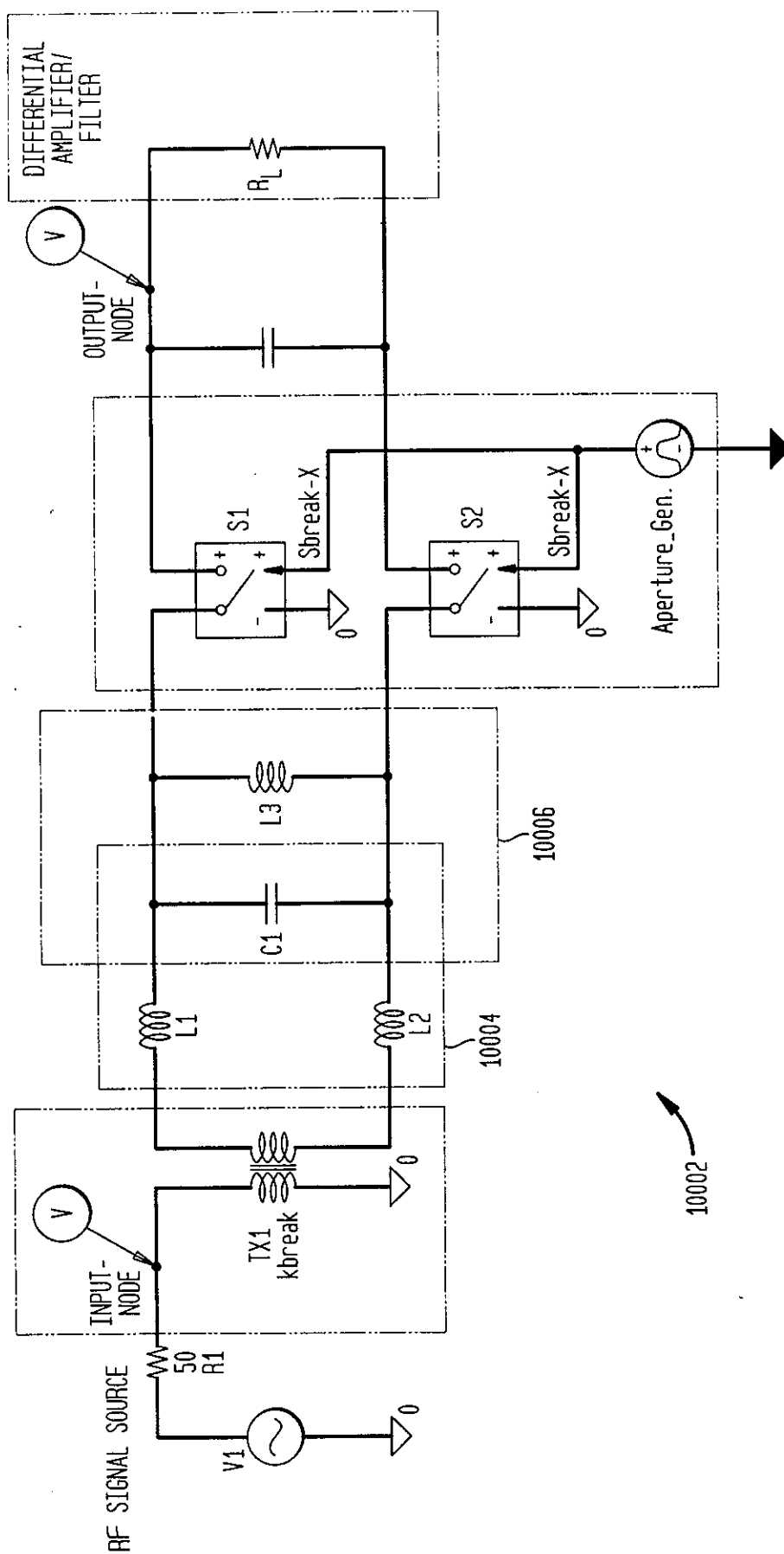
121/283

FIG. 99



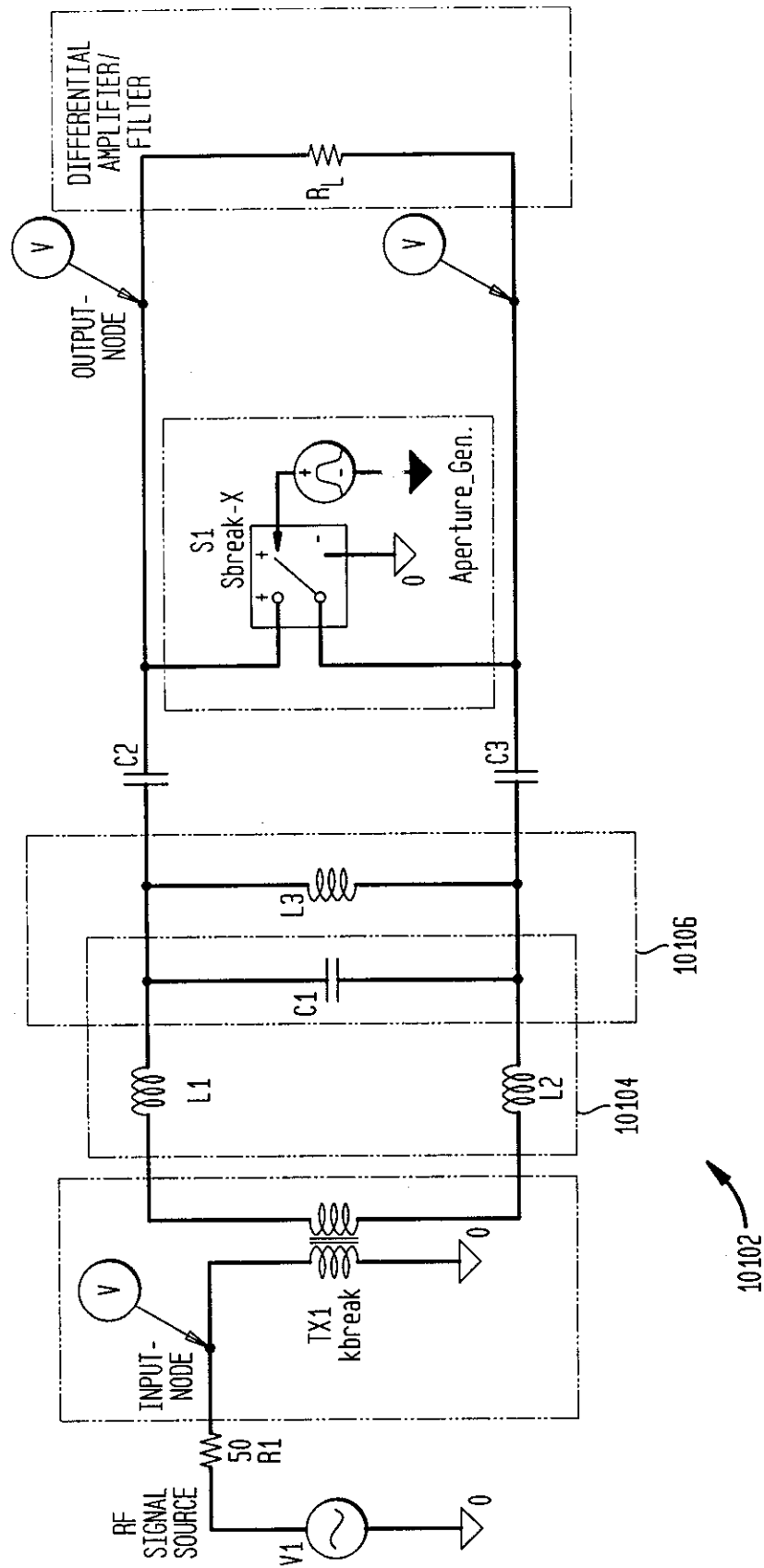
122/283

FIG. 100



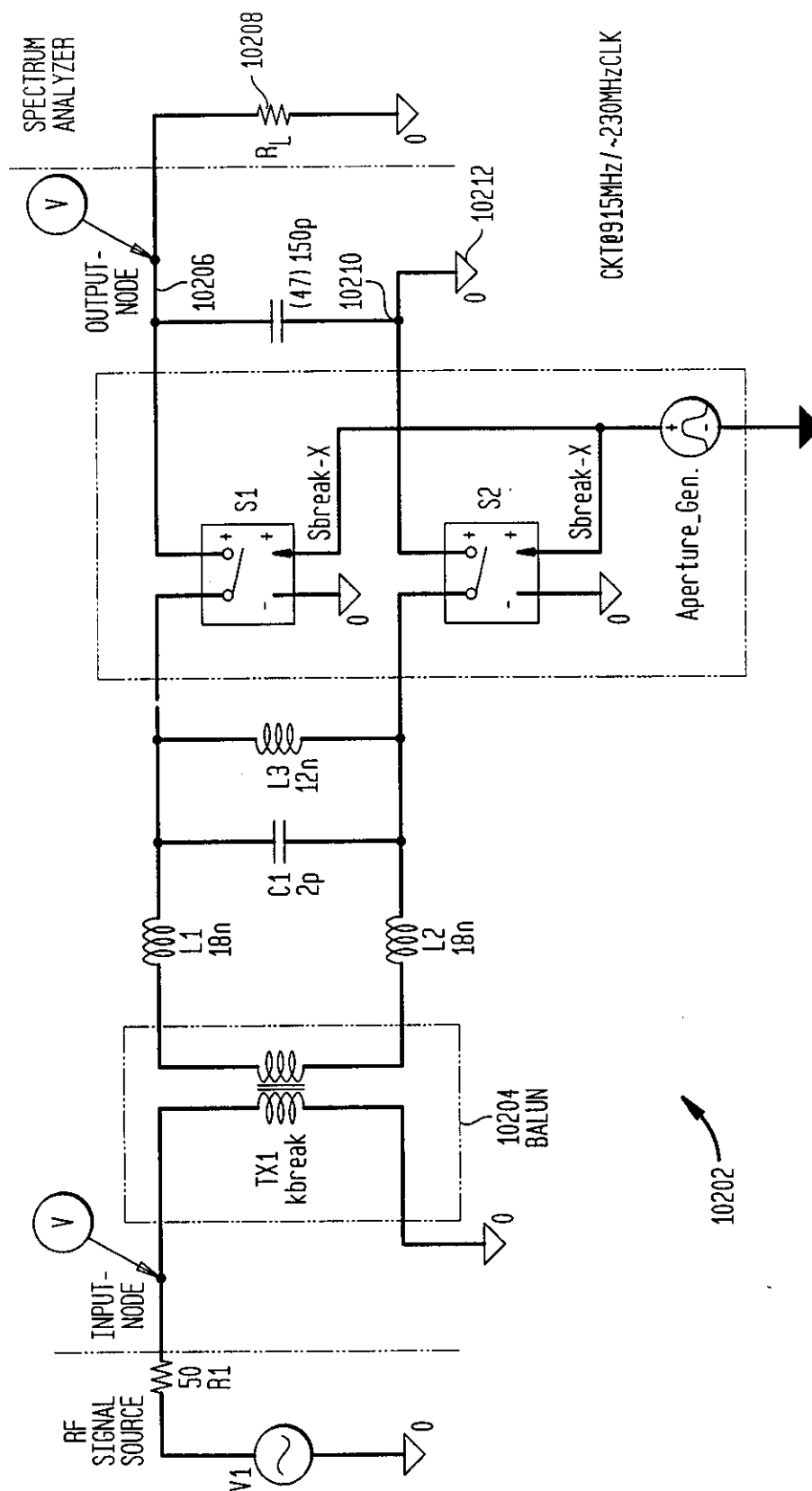
123/283

FIG. 101



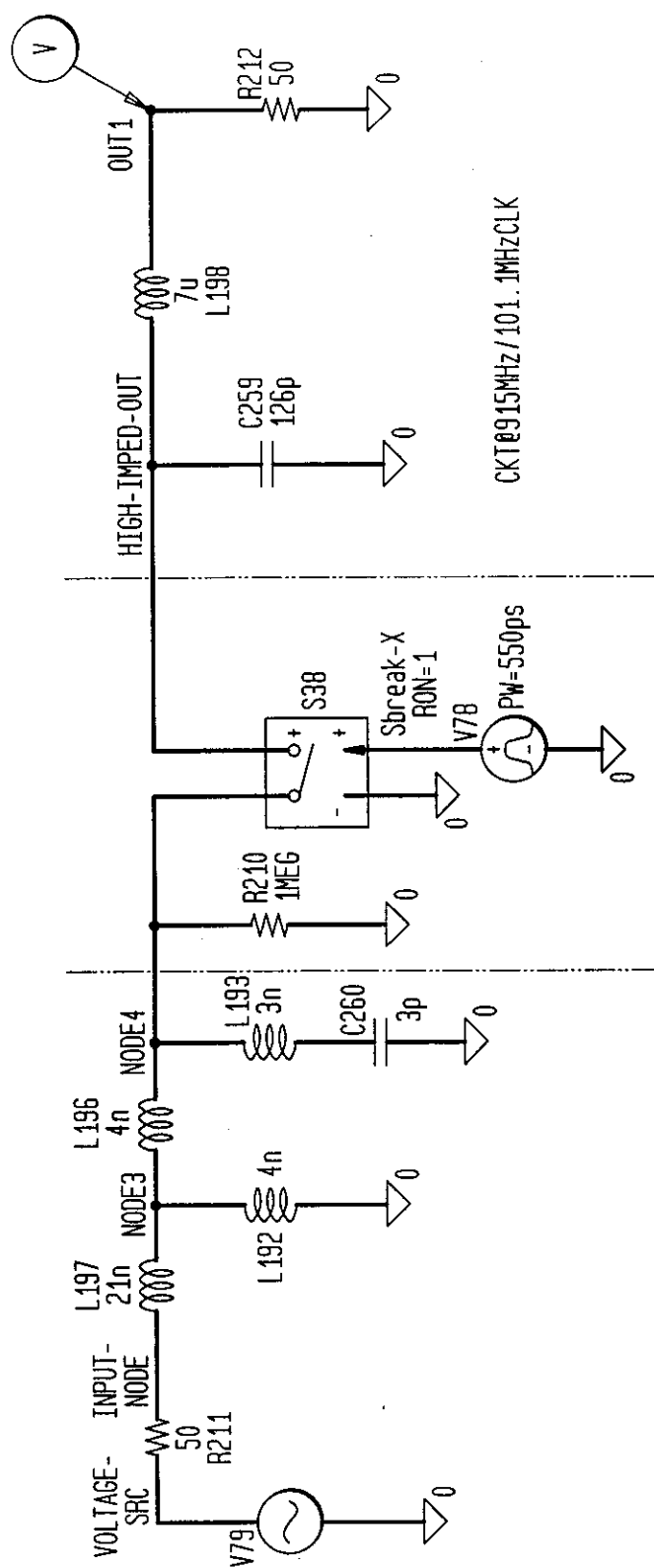
124/283

FIG. 102



125/283

FIG. 103



126/283

FIG. 104

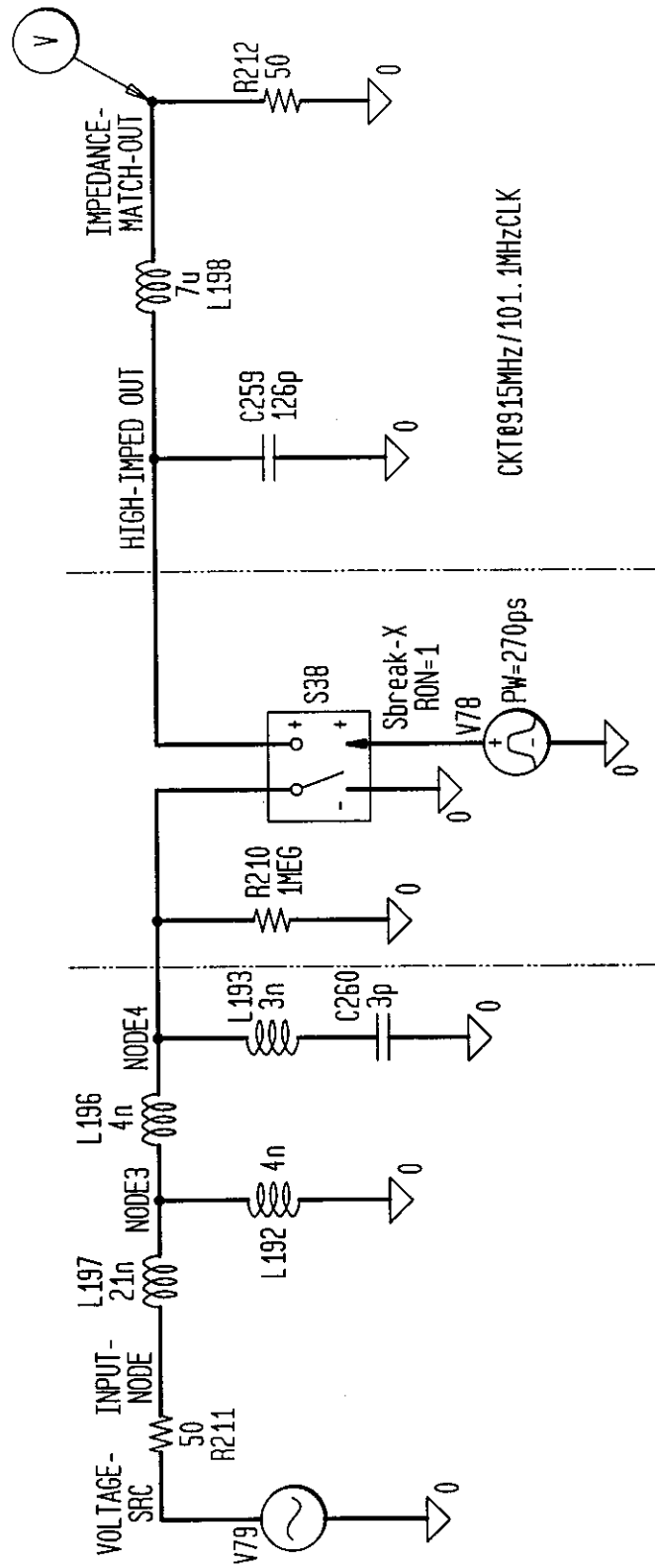
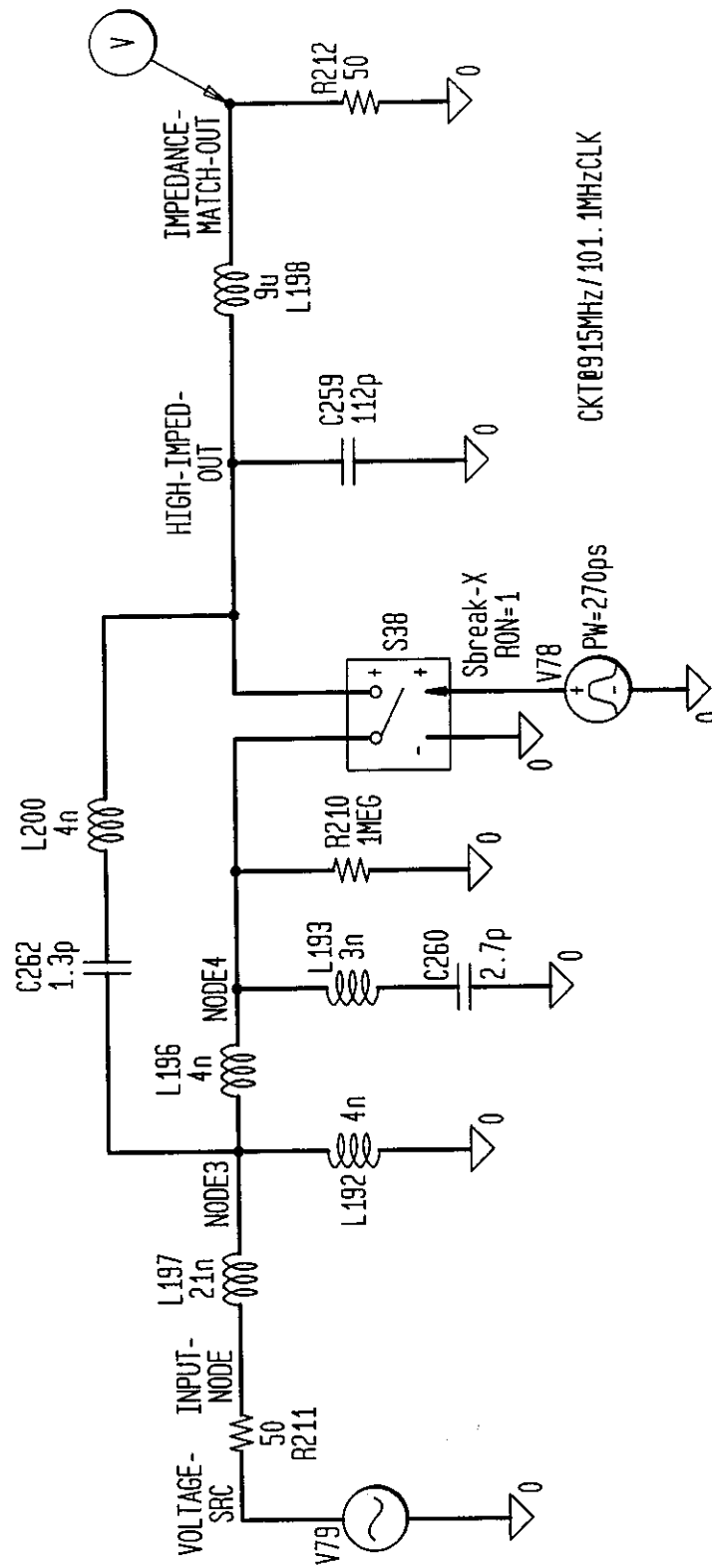


FIG. 105.



128/283

FIG. 106

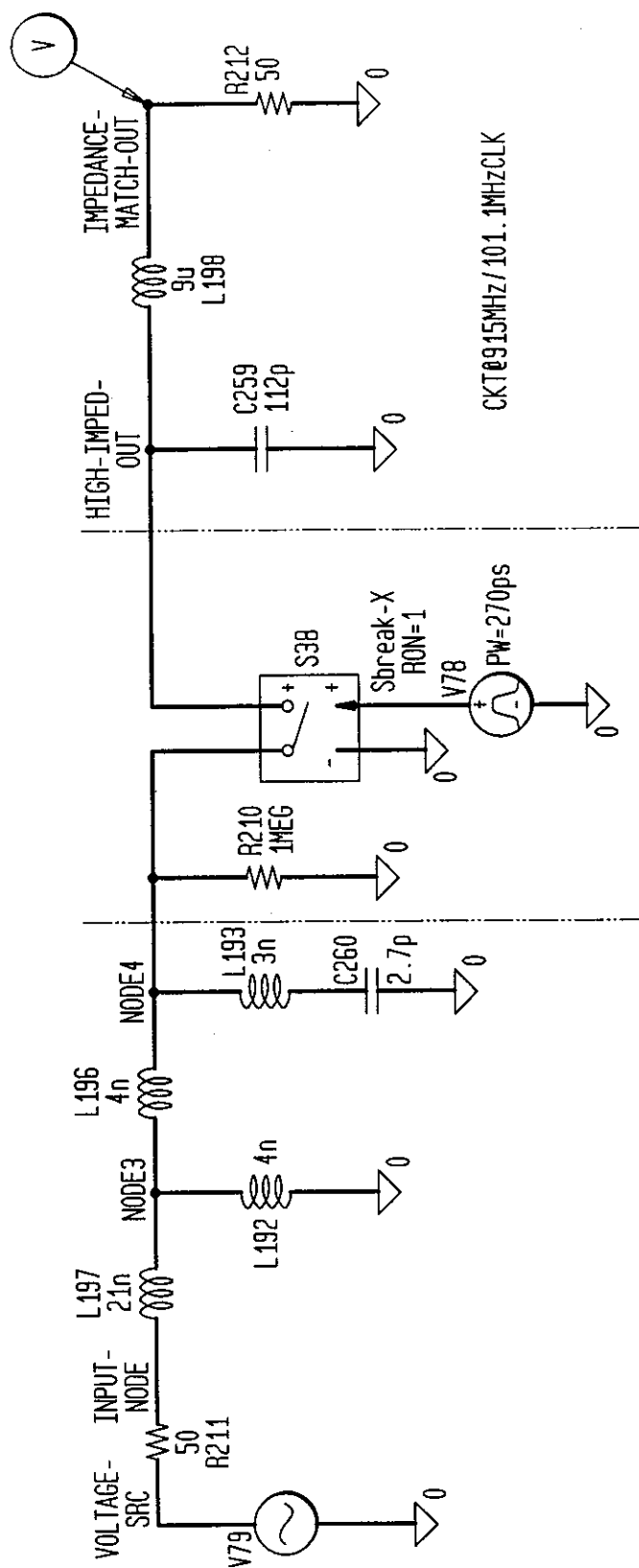
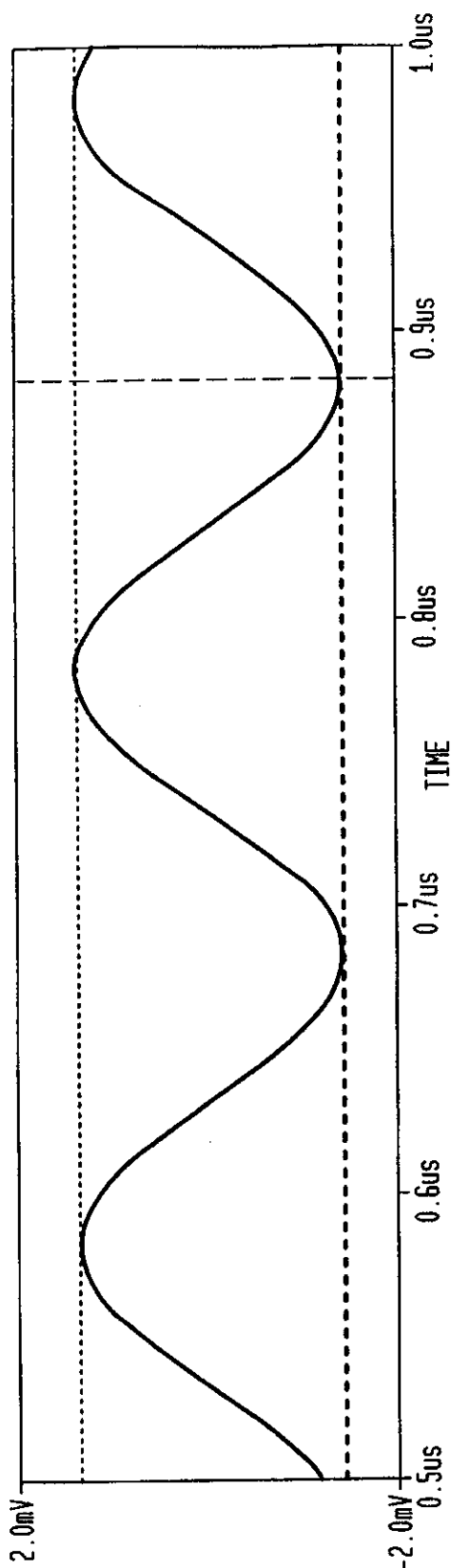
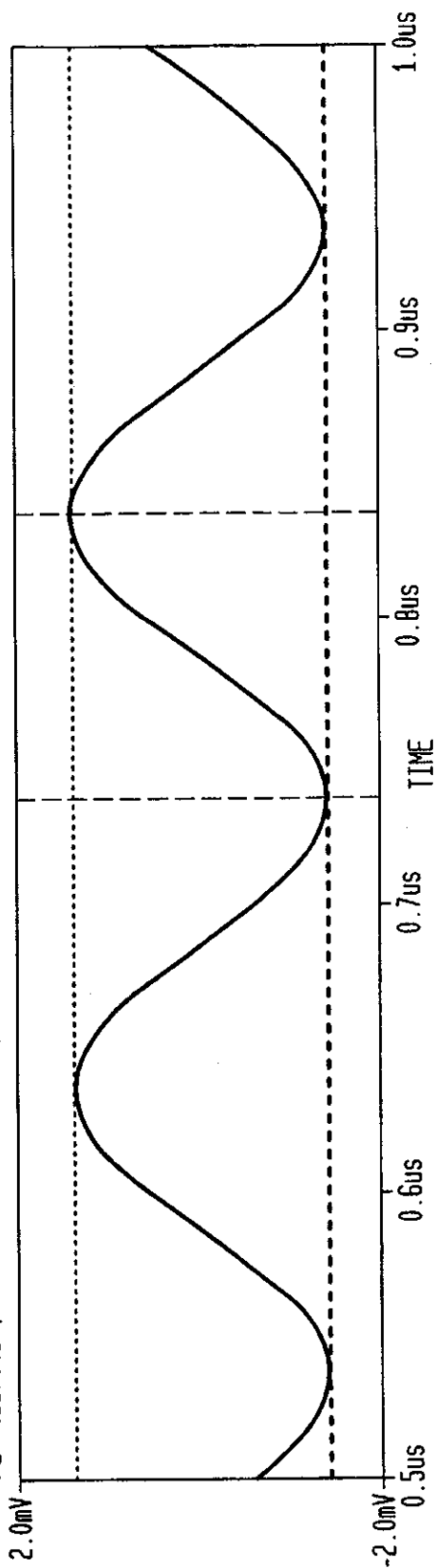


FIG. 107A



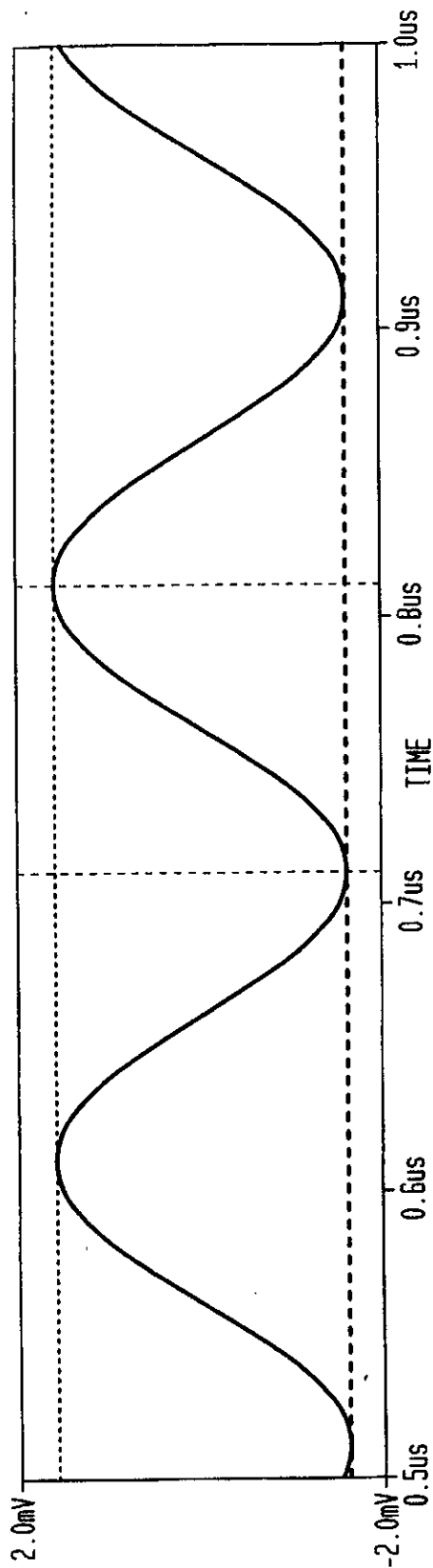
□ V(out1)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 107B



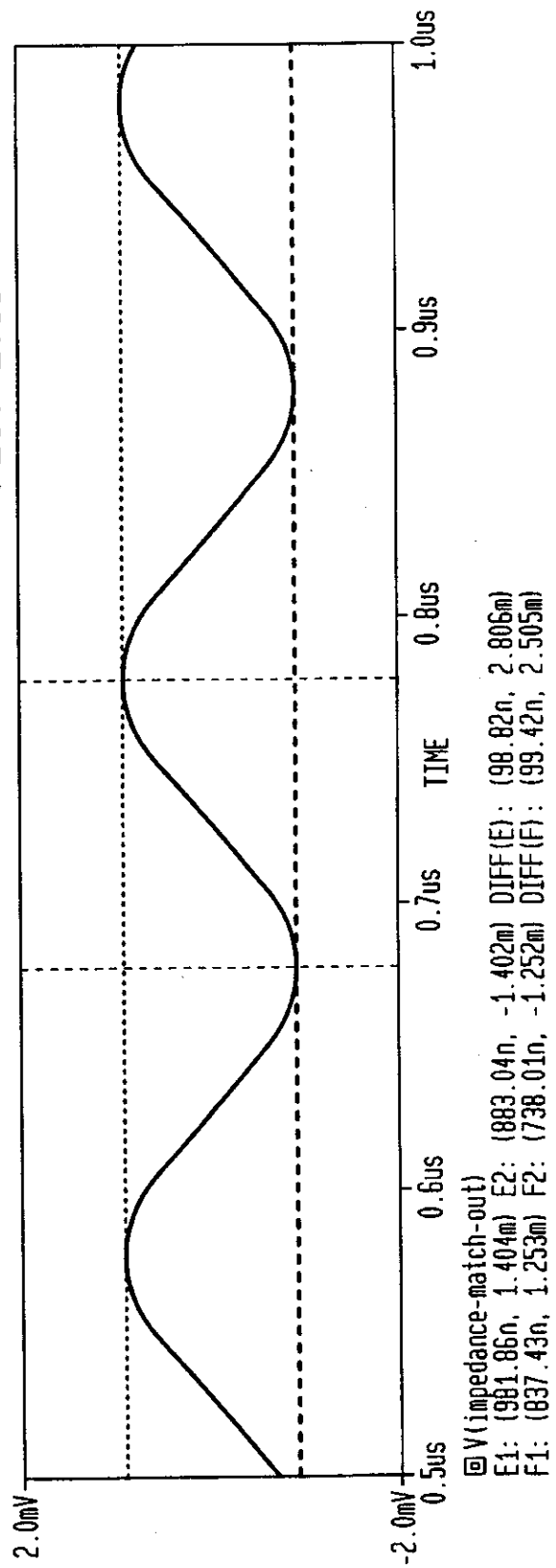
□ V(impedance-match-out)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 108A



□ V(impedance-match-out)
A1: (810.53n, 1.642m) A2: (710.52n, -1.621m) DIFF(A): (100.01n, 3.263m)
B1: (777.78n, 942.32u) B2: (677.18n, -942.51u) DIFF(B): (100.60n, 1.885m)

FIG. 108B



□ V(impedance-match-out)
E1: (981.86n, 1.404m) E2: (883.04n, -1.402m) DIFF(E): (98.82n, 2.806m)
F1: (837.43n, 1.253m) F2: (738.01n, -1.252m) DIFF(F): (99.42n, 2.505m)

FIG. 109A

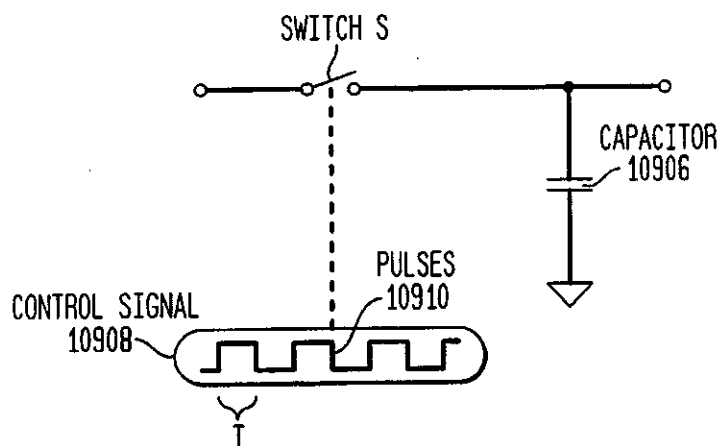


FIG. 109B

$q = C \cdot V$	EQ. 10
$V = A \cdot \sin(t)$	EQ. 11
$q(t) = C \cdot A \cdot \sin(t)$	EQ. 12
$\Delta q(t) = C \cdot A \cdot \sin(t) - C \cdot A \cdot \sin(t-T)$	EQ. 13
$\Delta q(t) = C \cdot A \cdot (\sin(t) - \sin(t-T))$	EQ. 14
$\sin(\alpha) - \sin(\beta) = 2 \cdot \sin\left(\frac{\alpha - \beta}{2}\right) \cdot \cos\left(\frac{\alpha + \beta}{2}\right)$	EQ. 15
$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left[\frac{t - (t-T)}{2}\right] \cdot \cos\left[\frac{t + (t-T)}{2}\right]$	EQ. 16
$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left(\frac{1}{2} \cdot T\right) \cdot \cos\left(t - \frac{1}{2} \cdot T\right)$	EQ. 17
$q(t) = \int C \cdot A \cdot (\sin(t) - \sin(t-T)) dt$	EQ. 18
$q(t) = -\cos(t) \cdot C \cdot A + \cos(t-T) \cdot C \cdot A$	EQ. 19
$q(t) = C \cdot A \cdot (\cos(t-T) - \cos(t))$	EQ. 20

132/283

FIG. 109C

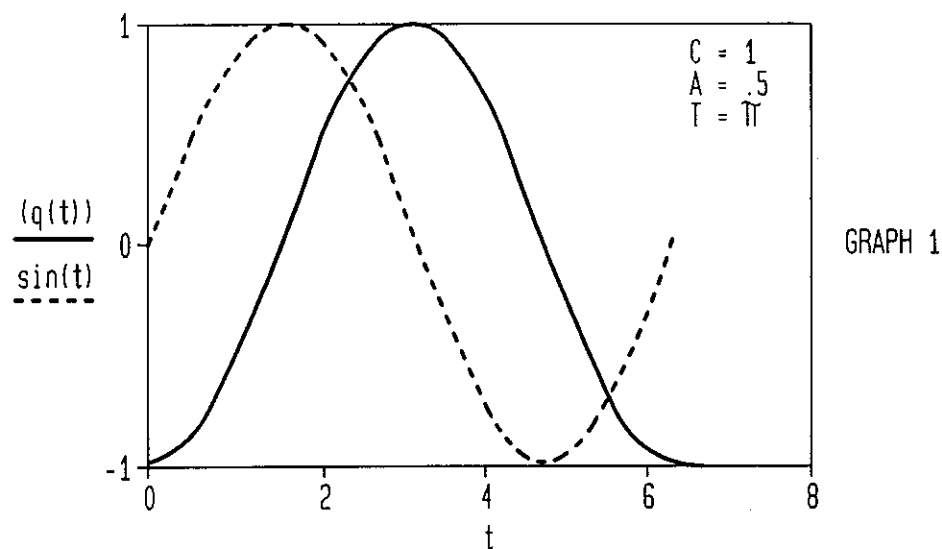


FIG. 109D

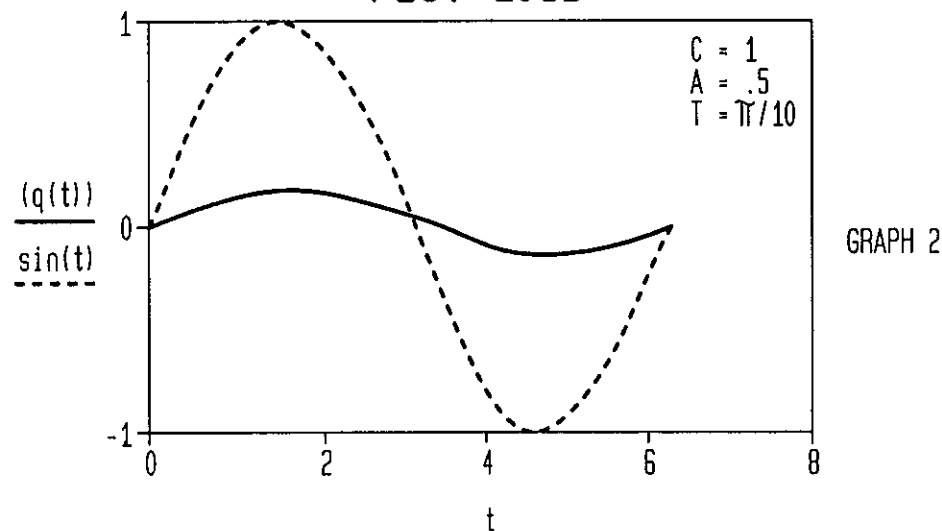


FIG. 109E

POWER-CHARGE RELATIONSHIP

$$q = C \cdot V \quad \text{EQ. 21}$$

$$V = q/C \quad \text{EQ. 22}$$

$$V = J/C \quad \text{EQ. 23}$$

$$J = q^2/C \quad \text{EQ. 24}$$

$$P = J/S \quad \text{EQ. 25}$$

$$P = \frac{q^2}{C \cdot S} \quad \text{EQ. 26}$$

FIG. 109F

INSERTION LOSS

INSERTION LOSS IN dB IS EXPRESSED BY:

$$IL_{dB} = 10 \cdot \log\left(\frac{P_{in}}{P_{out}}\right) \text{ or } -$$

$$IL_{dB} = 10 \cdot \log\left[\frac{\left(\frac{V_{in}^2}{R_{in}}\right)}{\left(\frac{V_{out}^2}{R_{out}}\right)}\right]$$

FIG. 110A

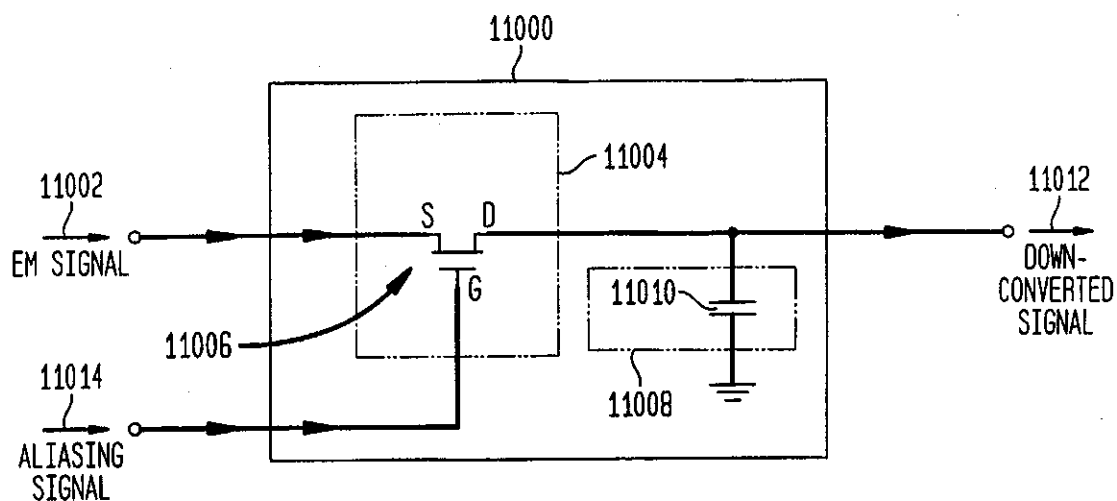
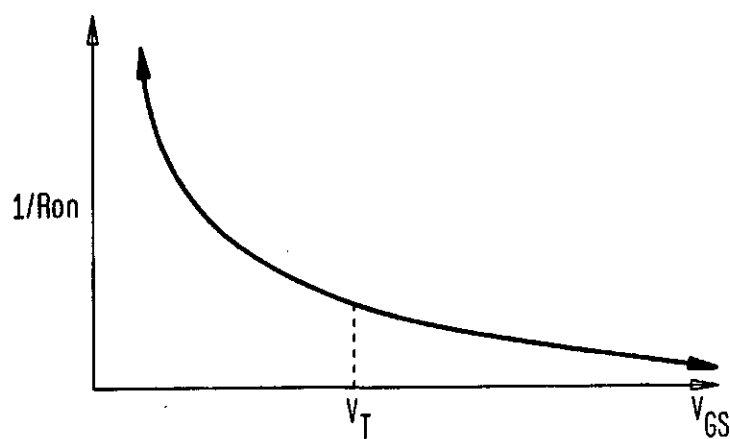
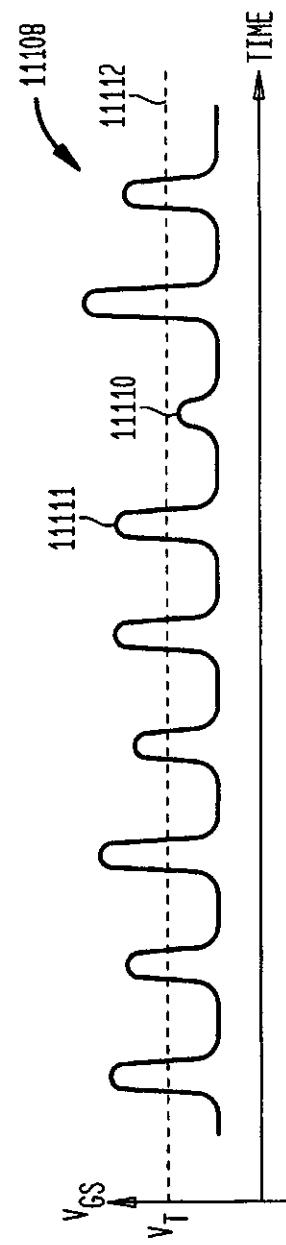
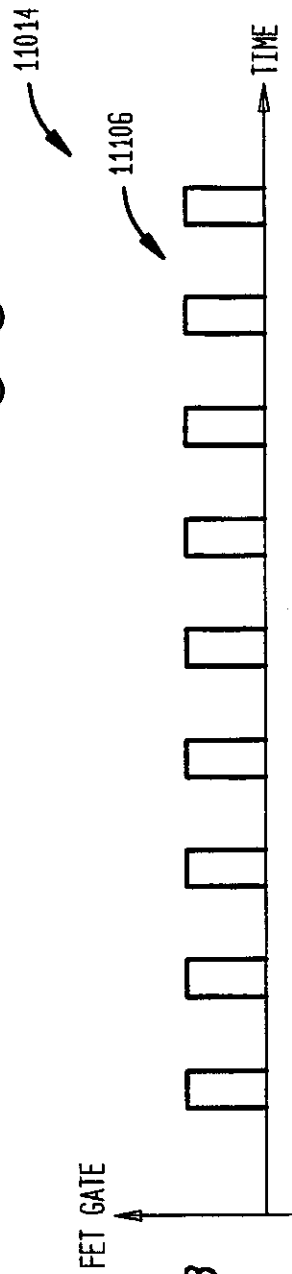
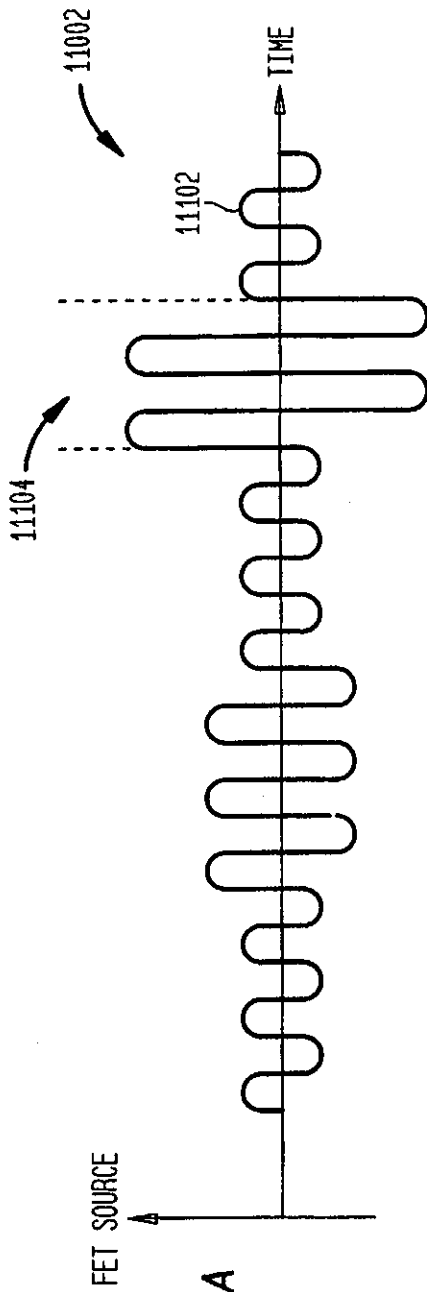


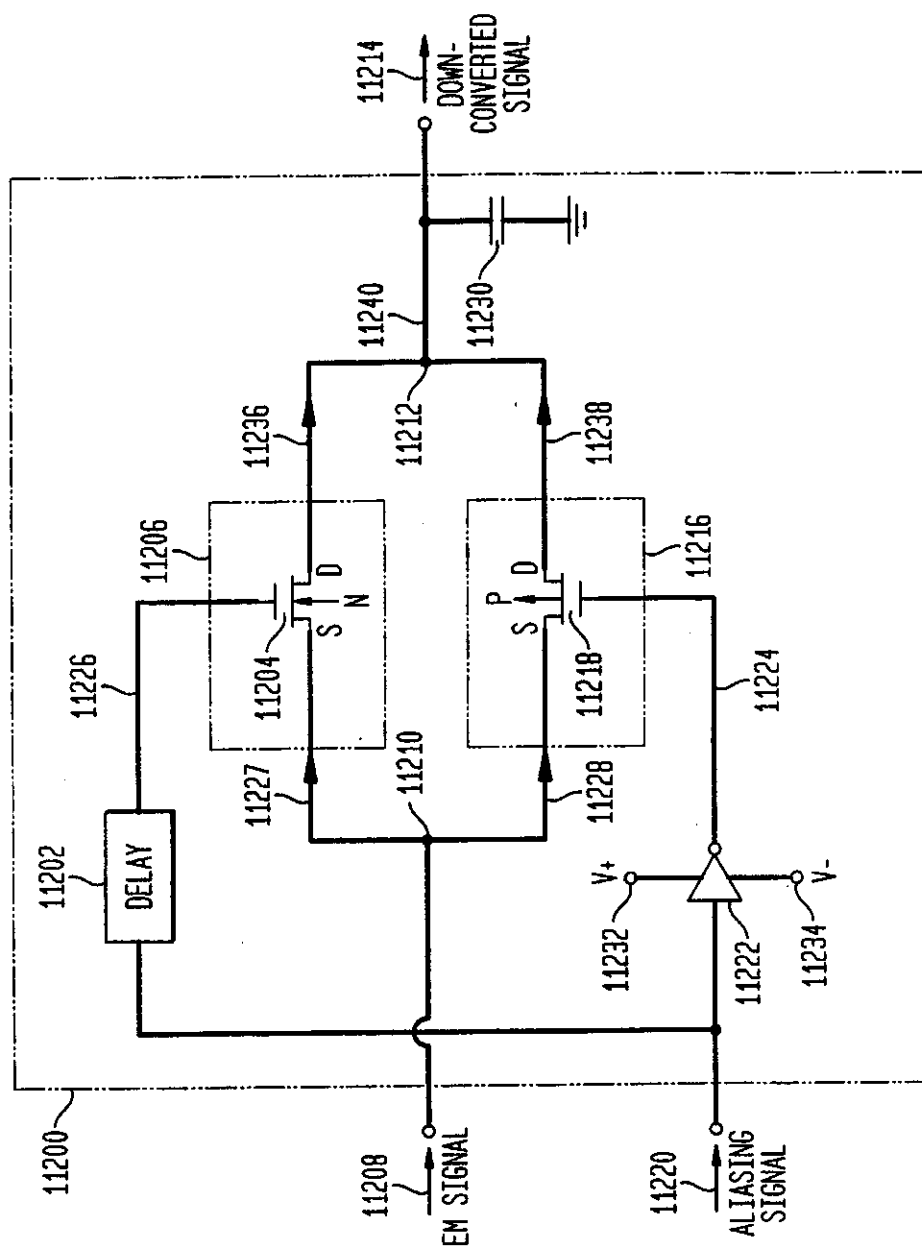
FIG. 110B





135/283

FIG. 112



136/283

FIG. 113A

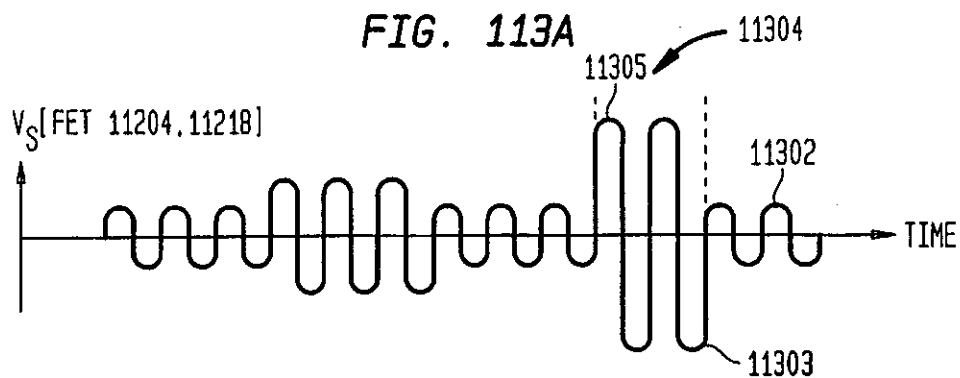


FIG. 113B

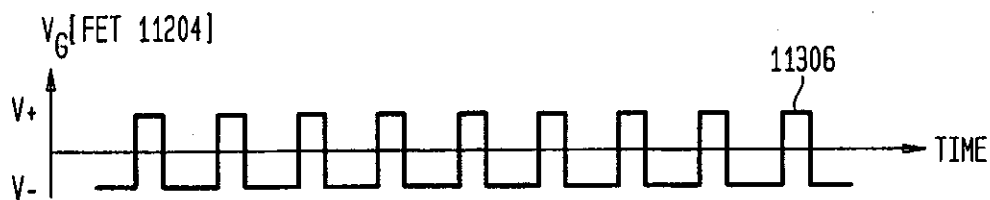


FIG. 113C

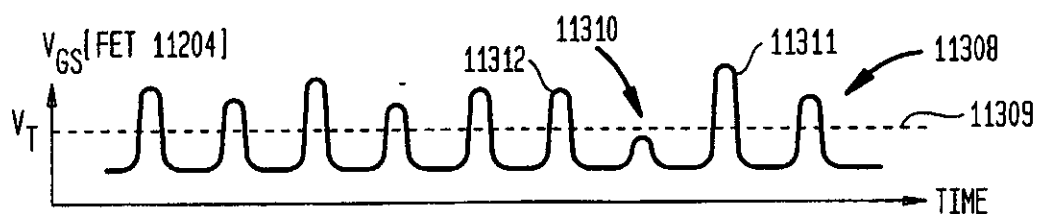


FIG. 113D

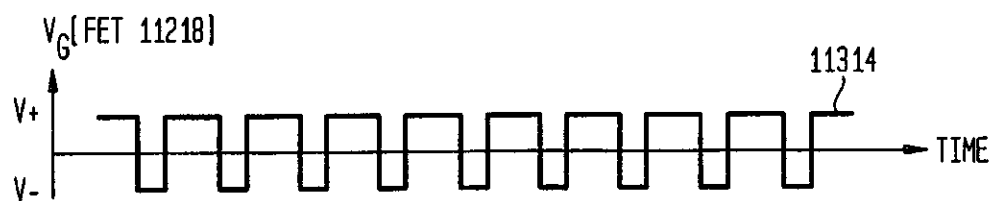
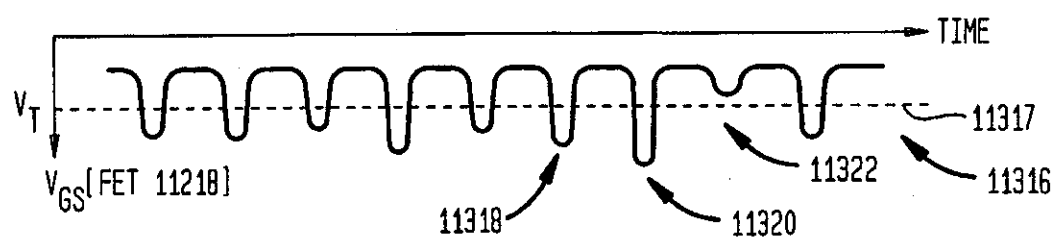
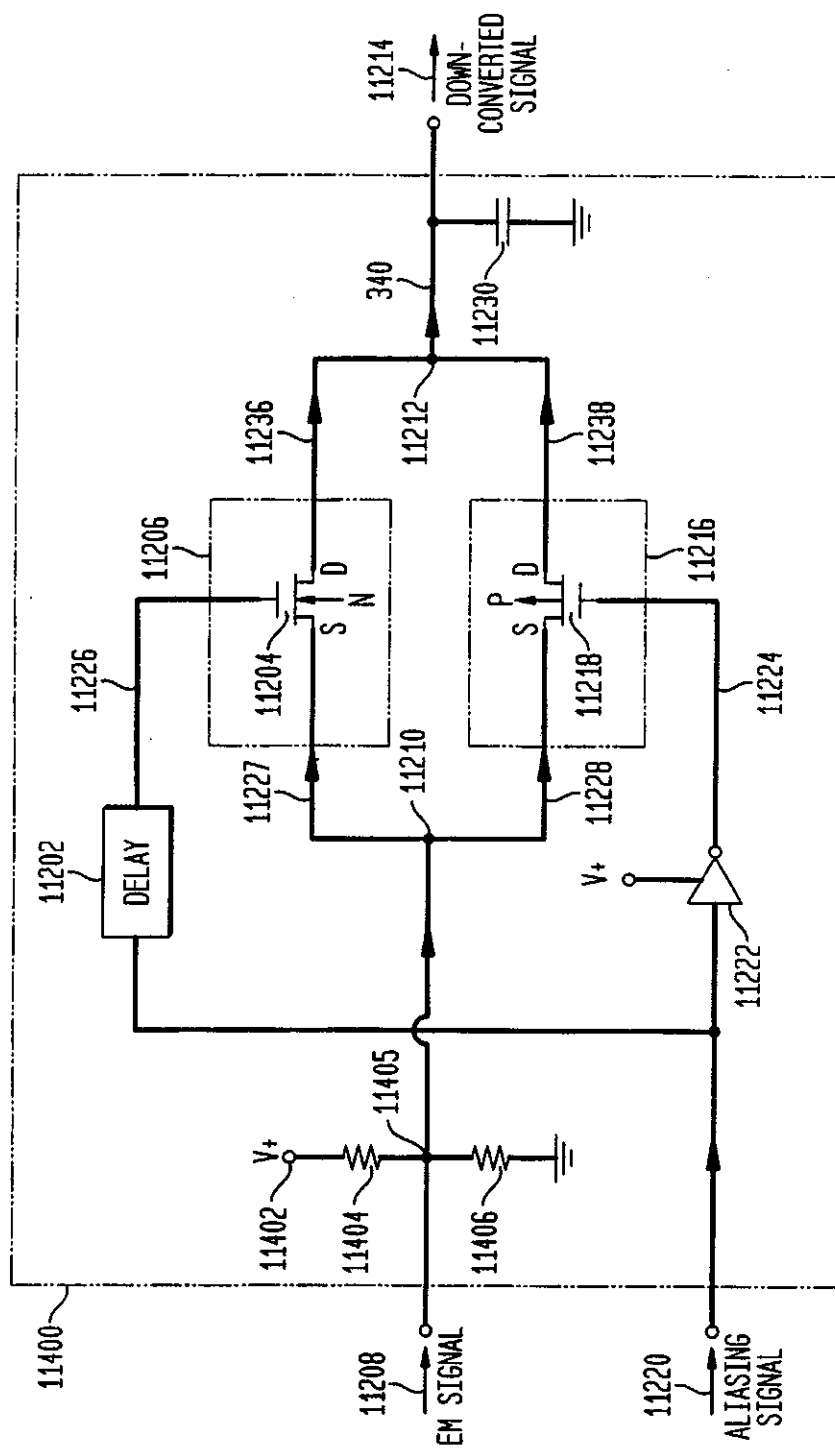


FIG. 113E



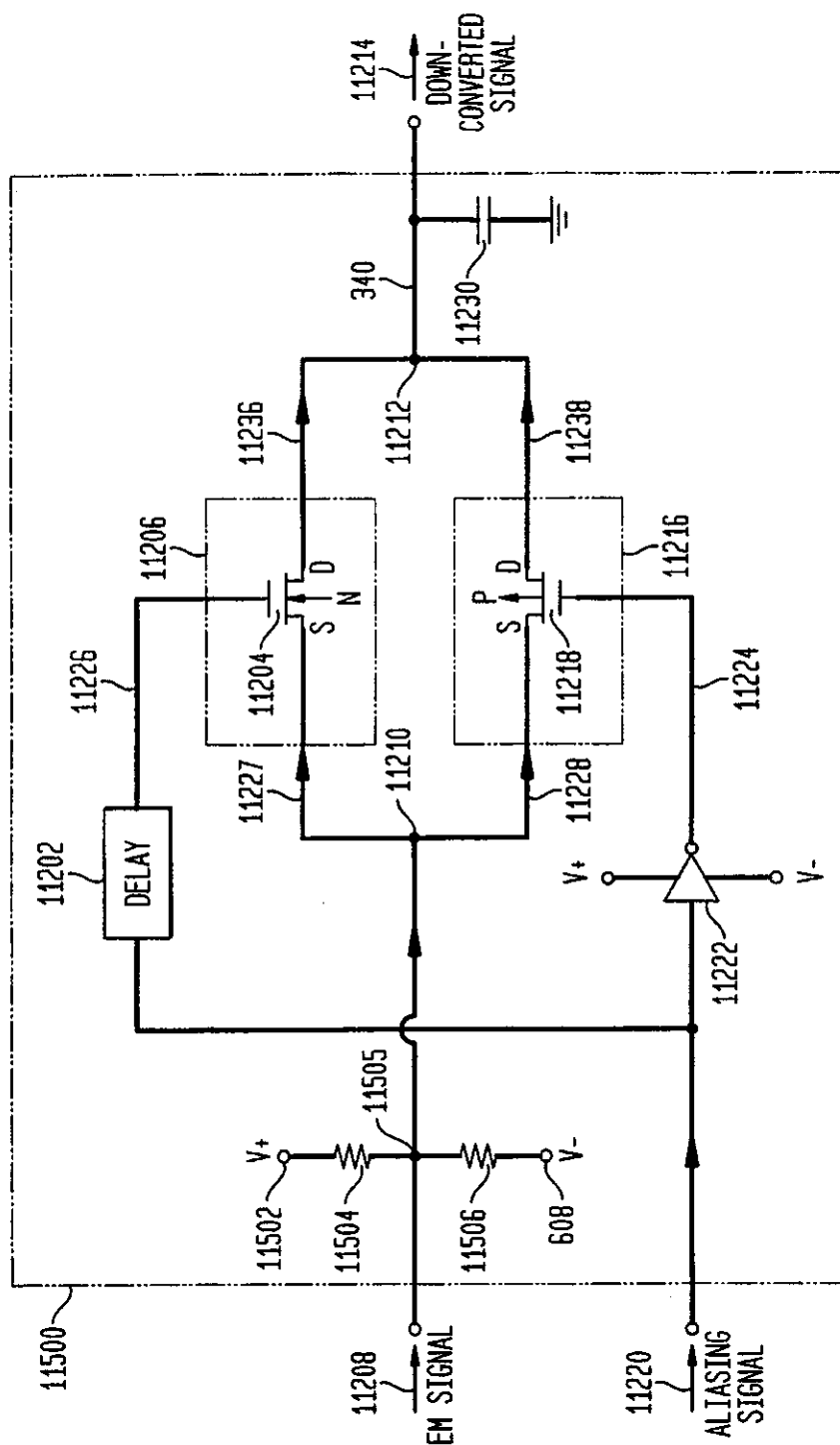
137/283

FIG. 114



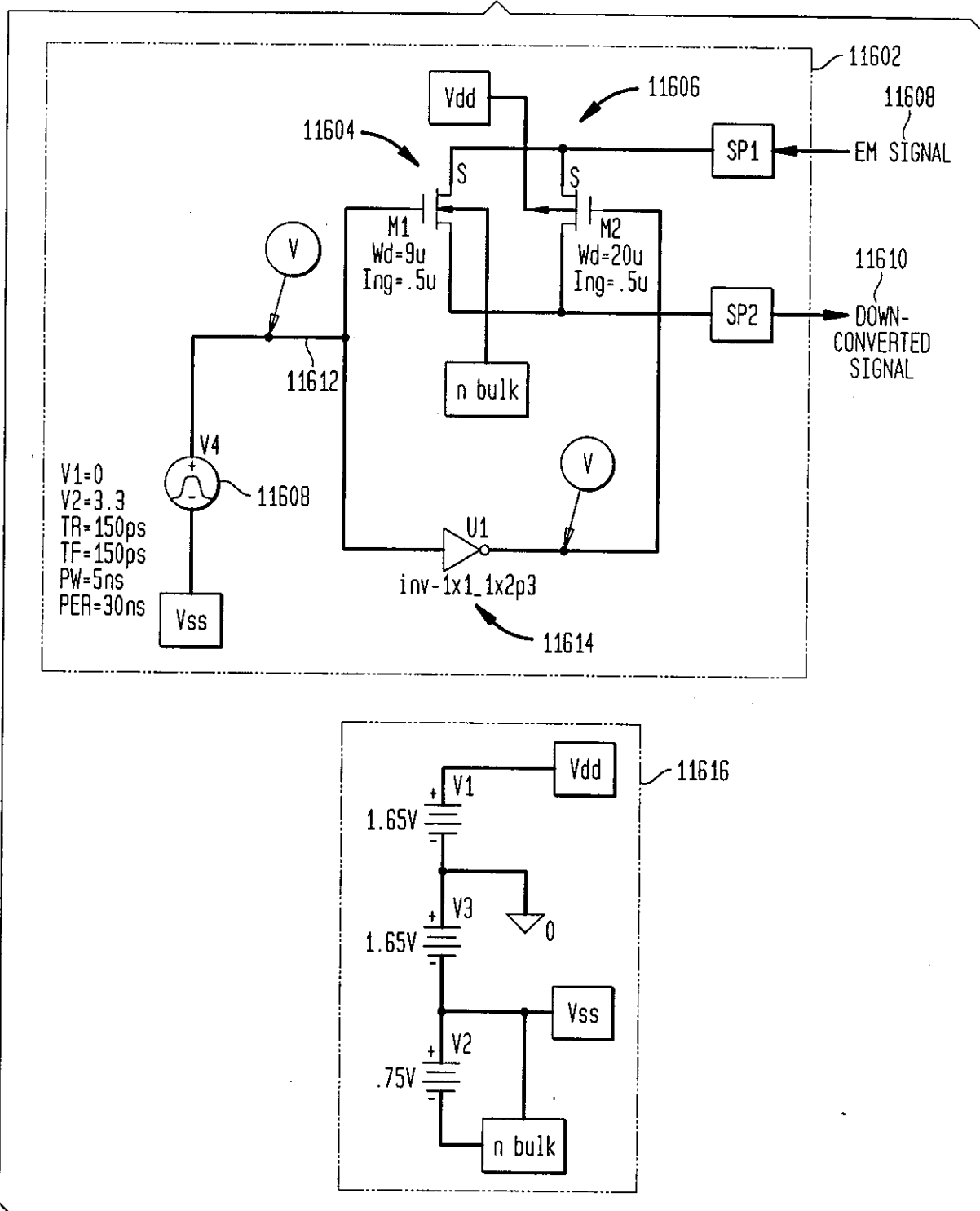
138/283

FIG. 115



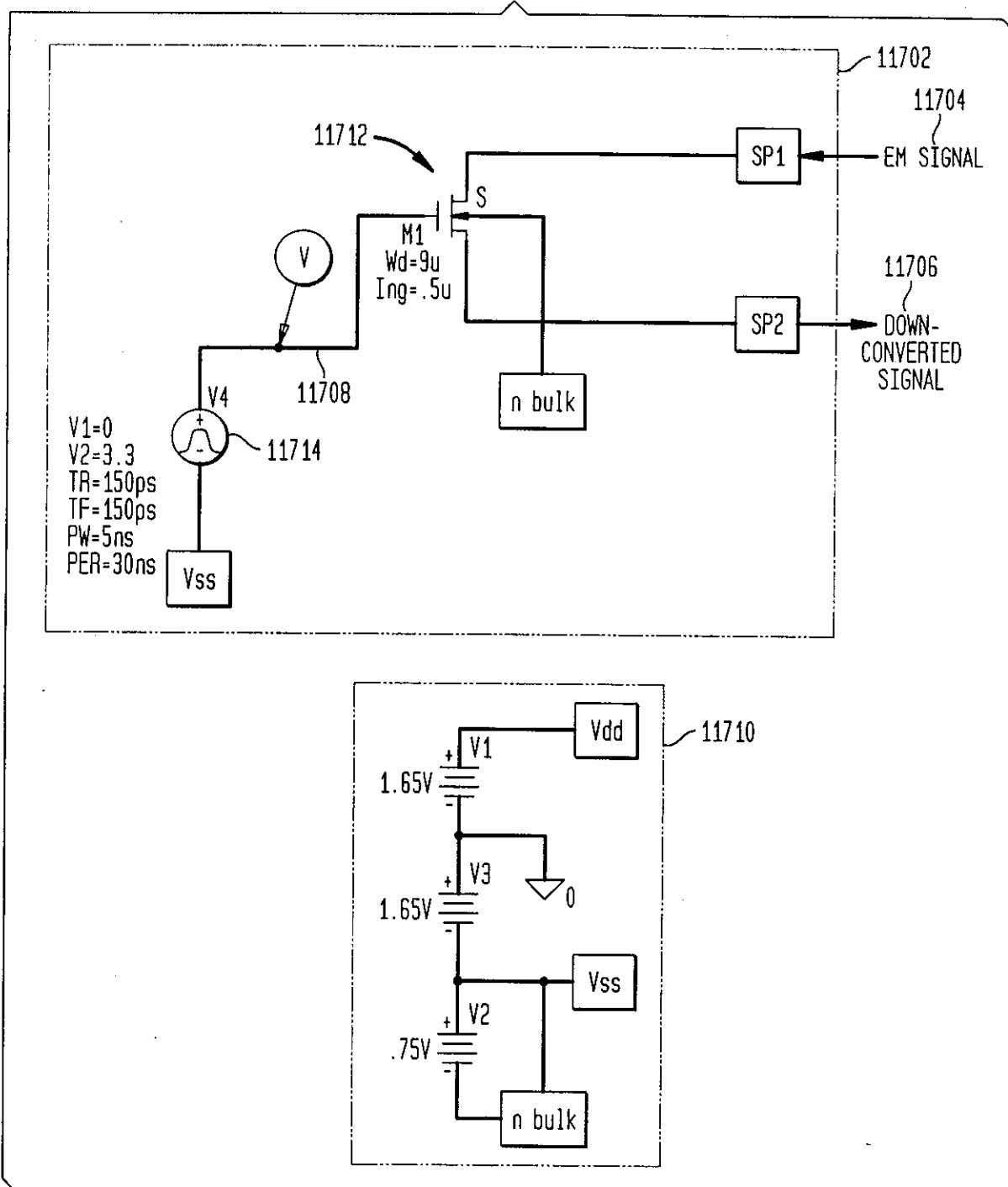
139/283

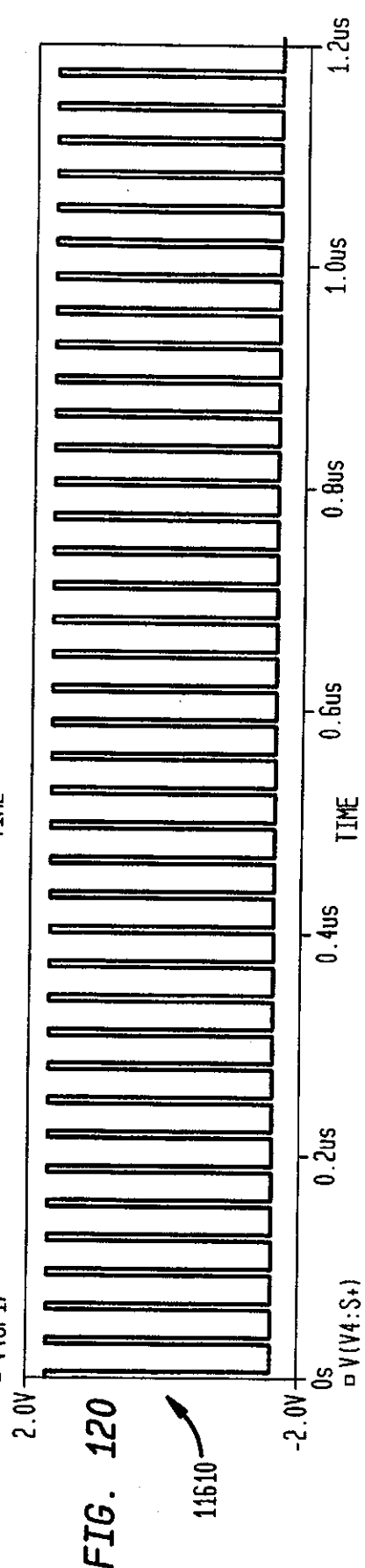
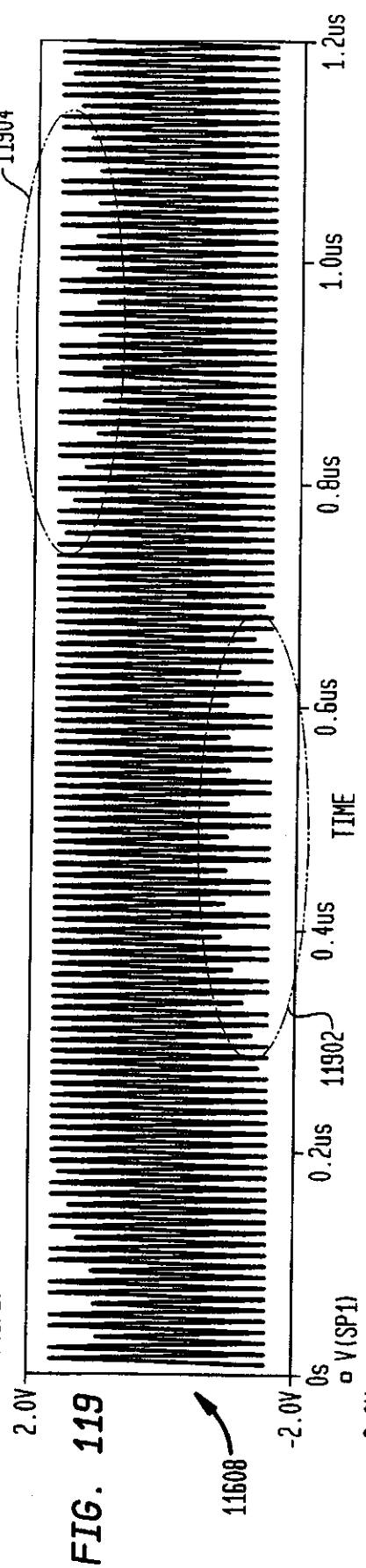
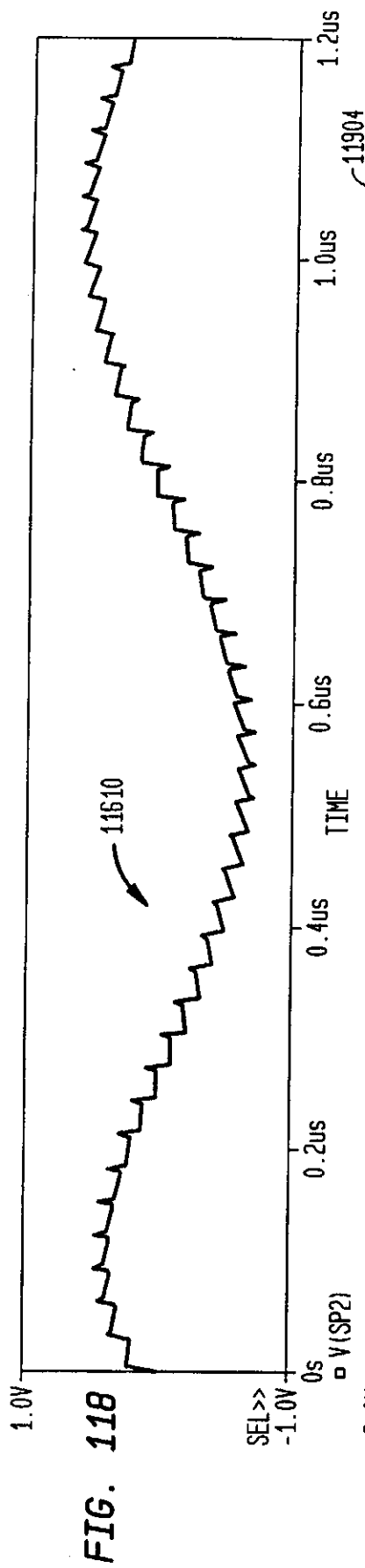
FIG. 116



140/283

FIG. 117





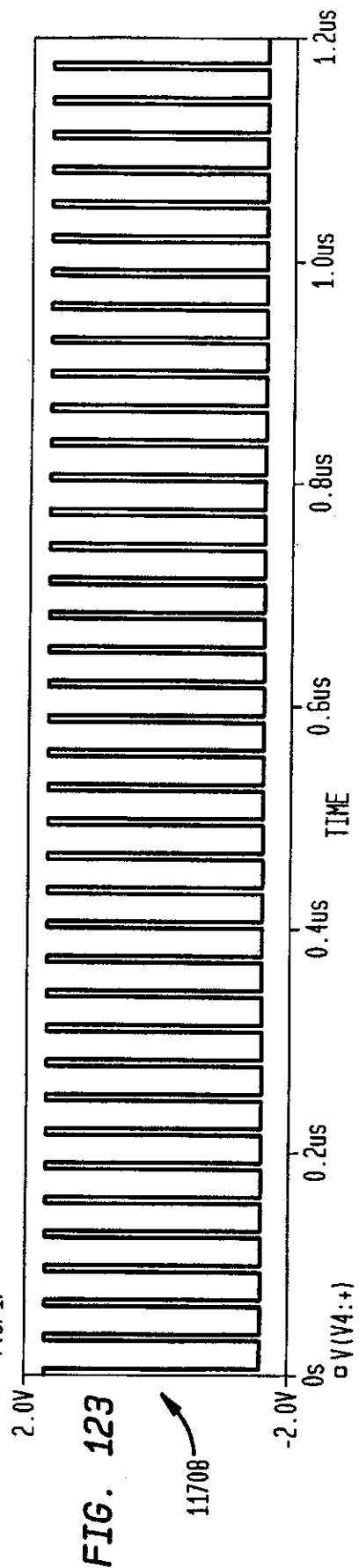
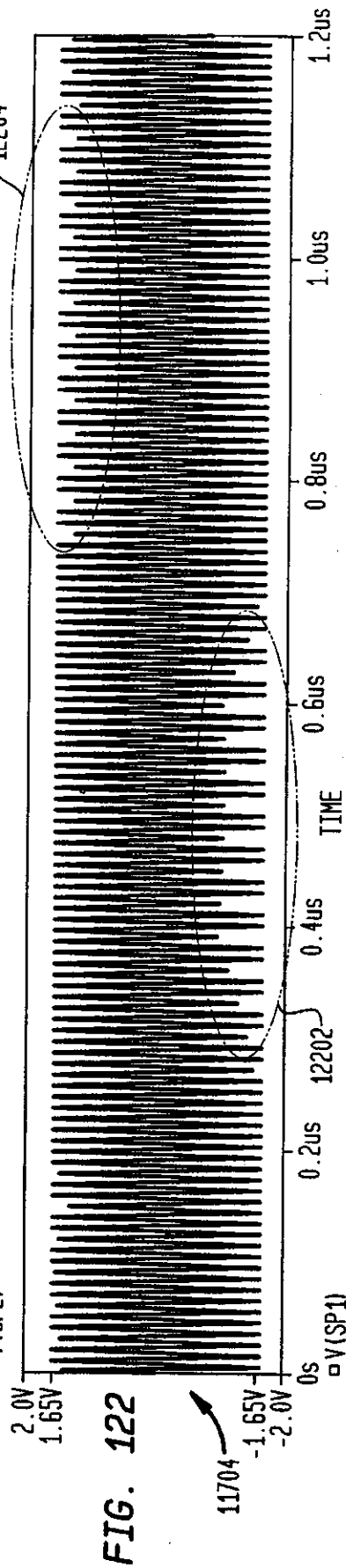
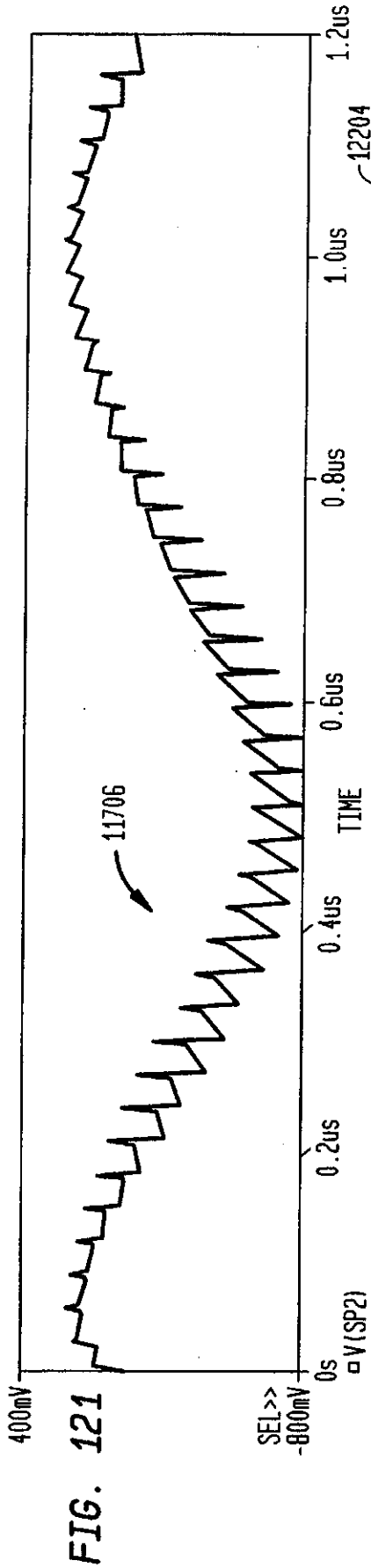


FIG. 124A

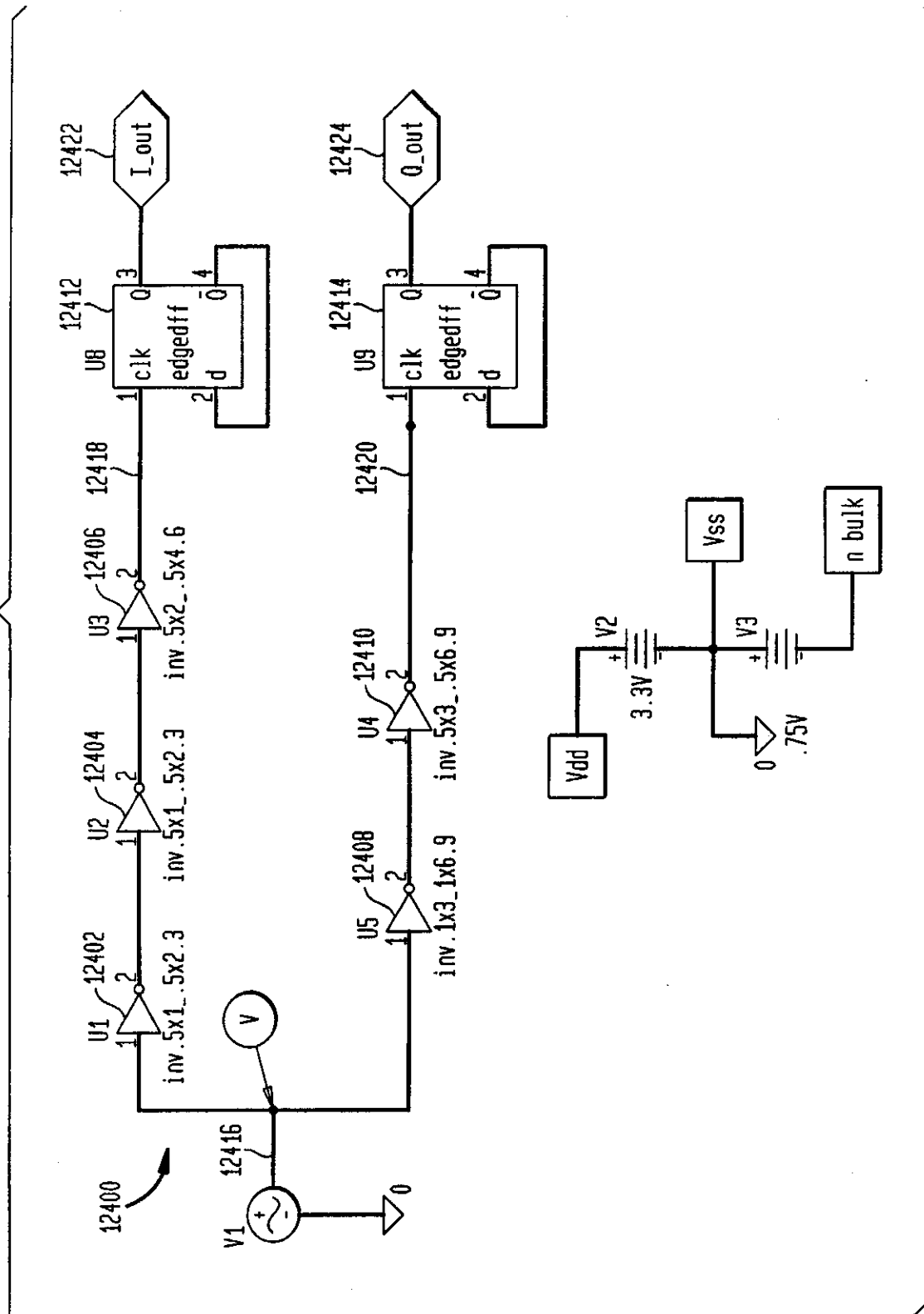
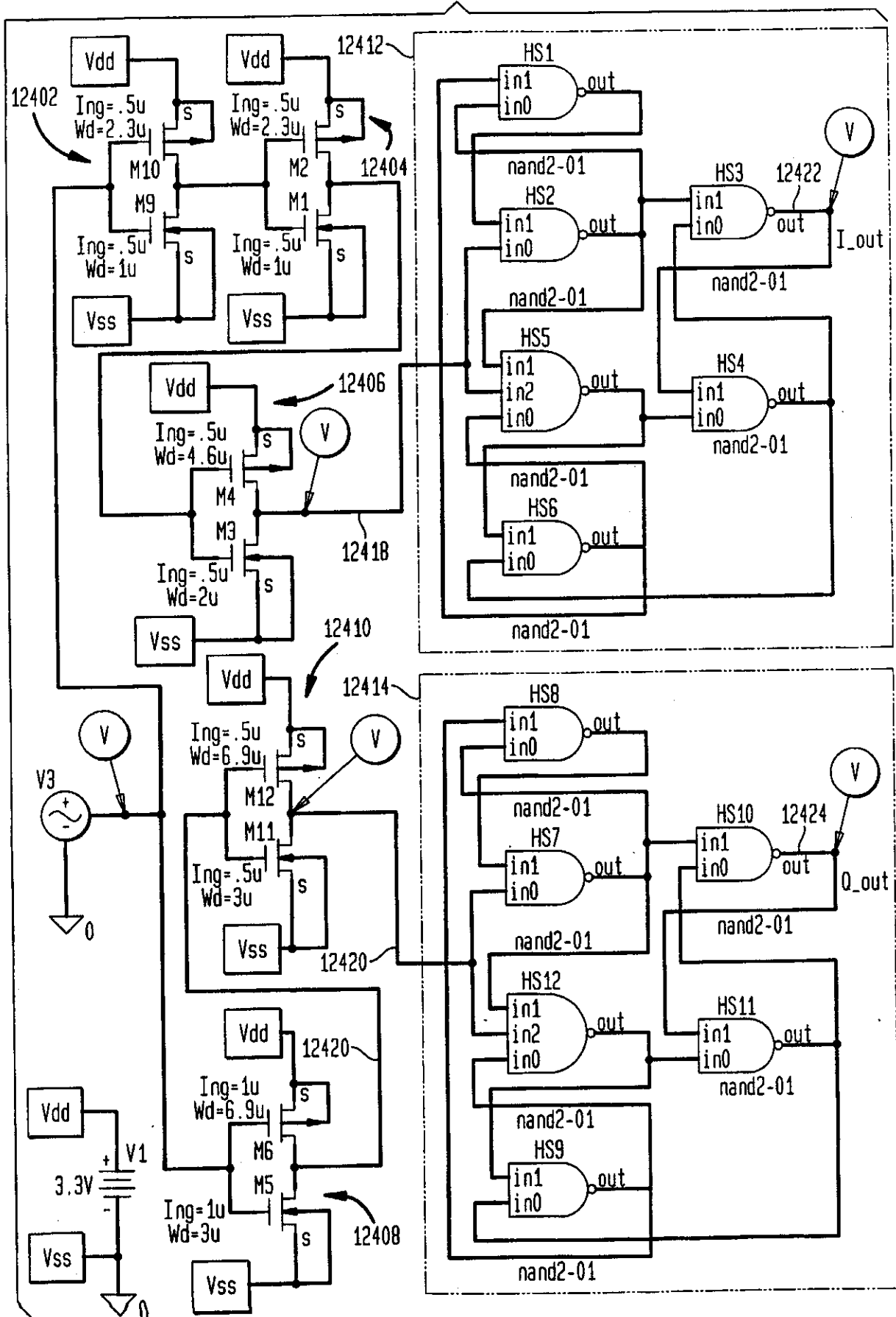


FIG. 124B



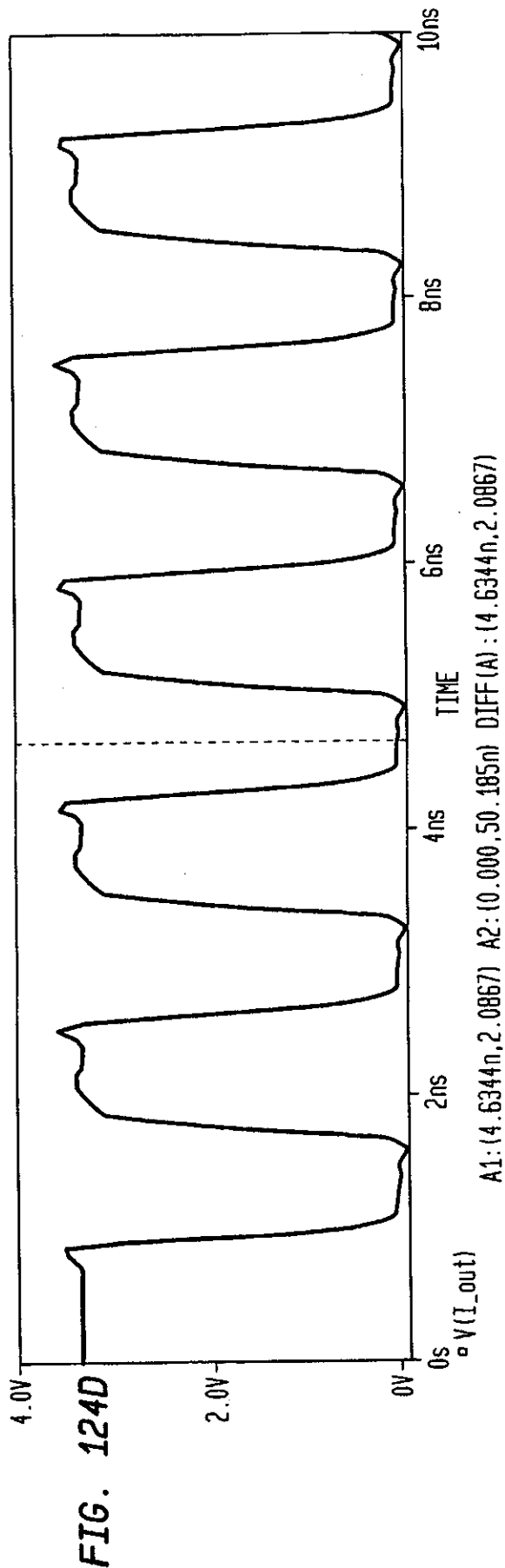
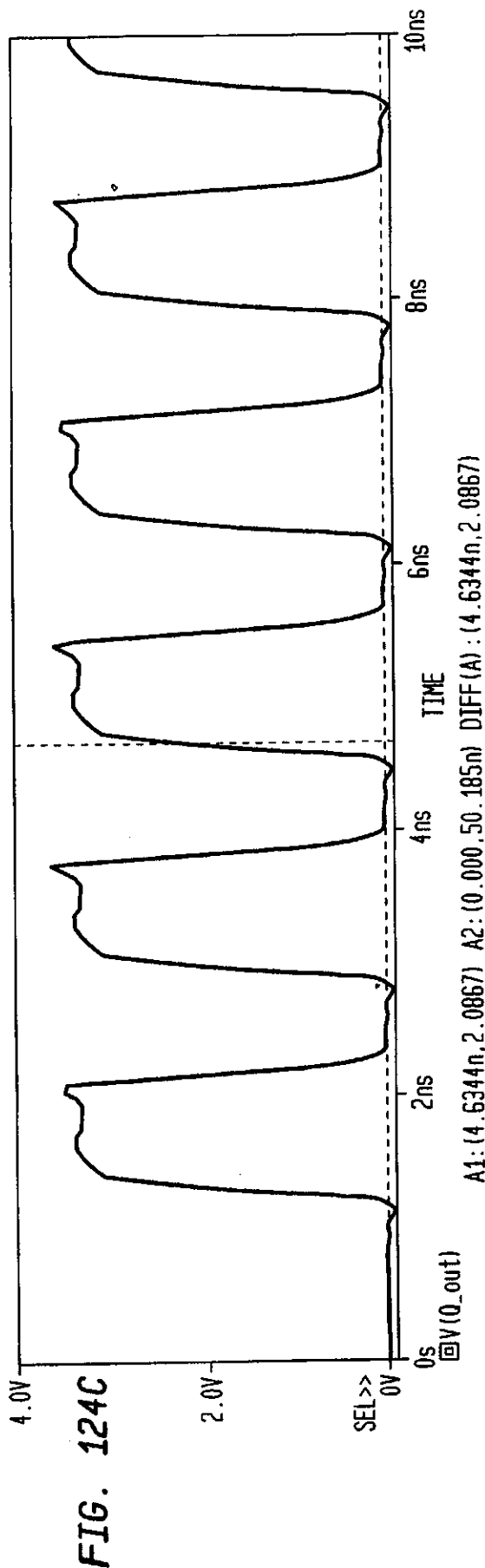


FIG. 124E

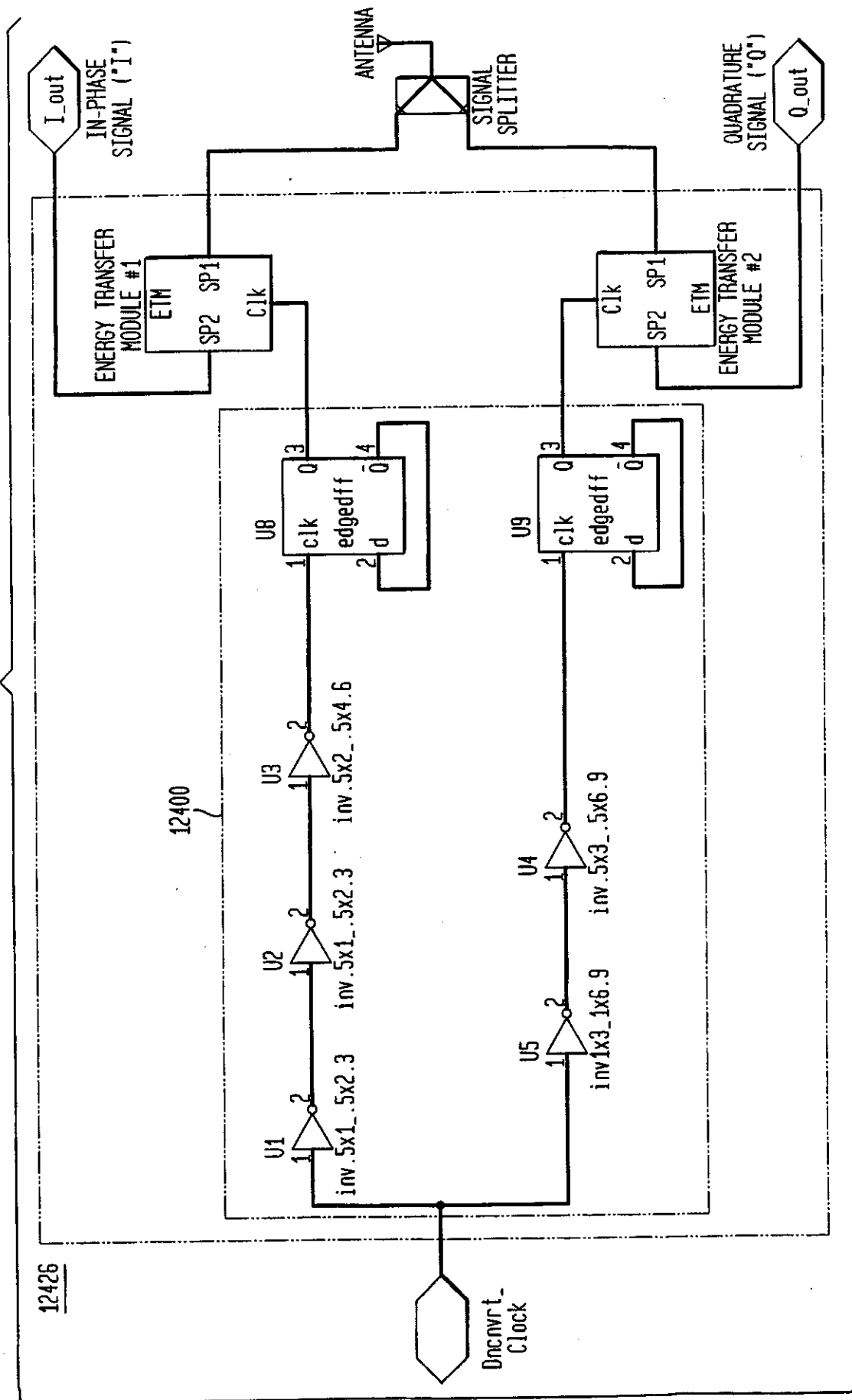


FIG. 124F

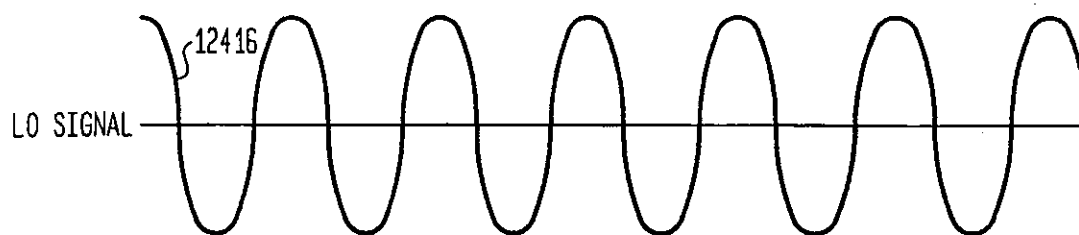


FIG. 124G

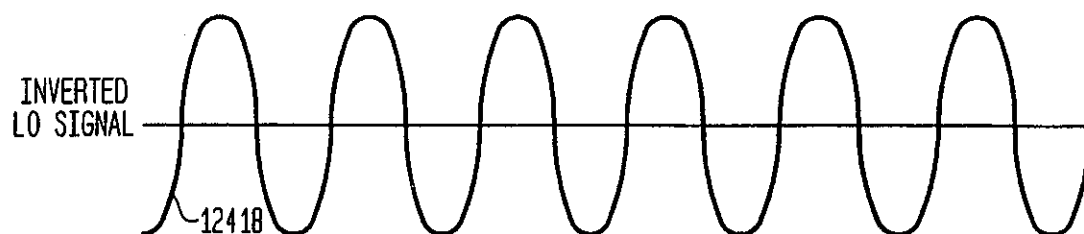


FIG. 124H

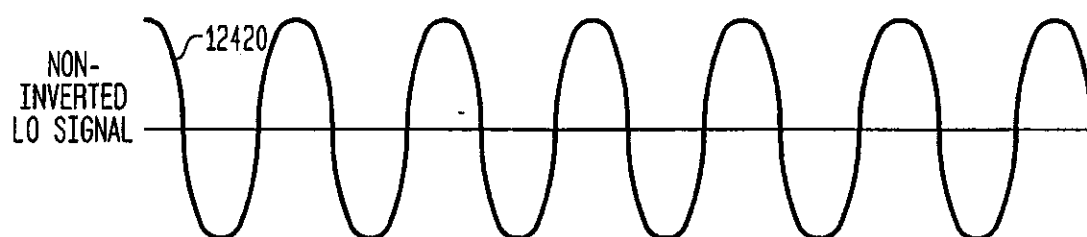


FIG. 124I

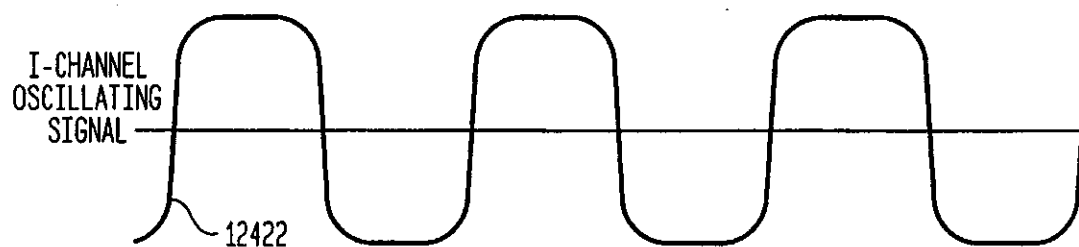


FIG. 124J

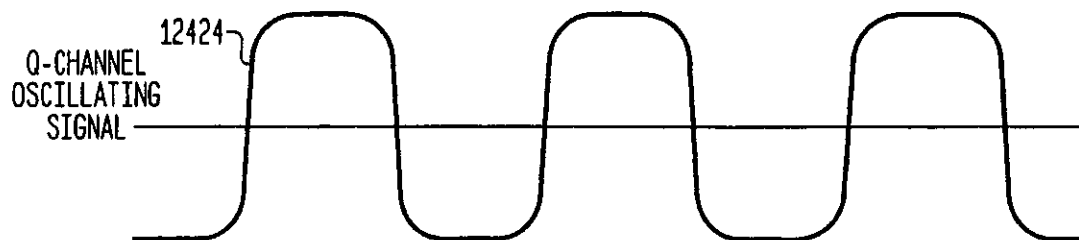


FIG. 125

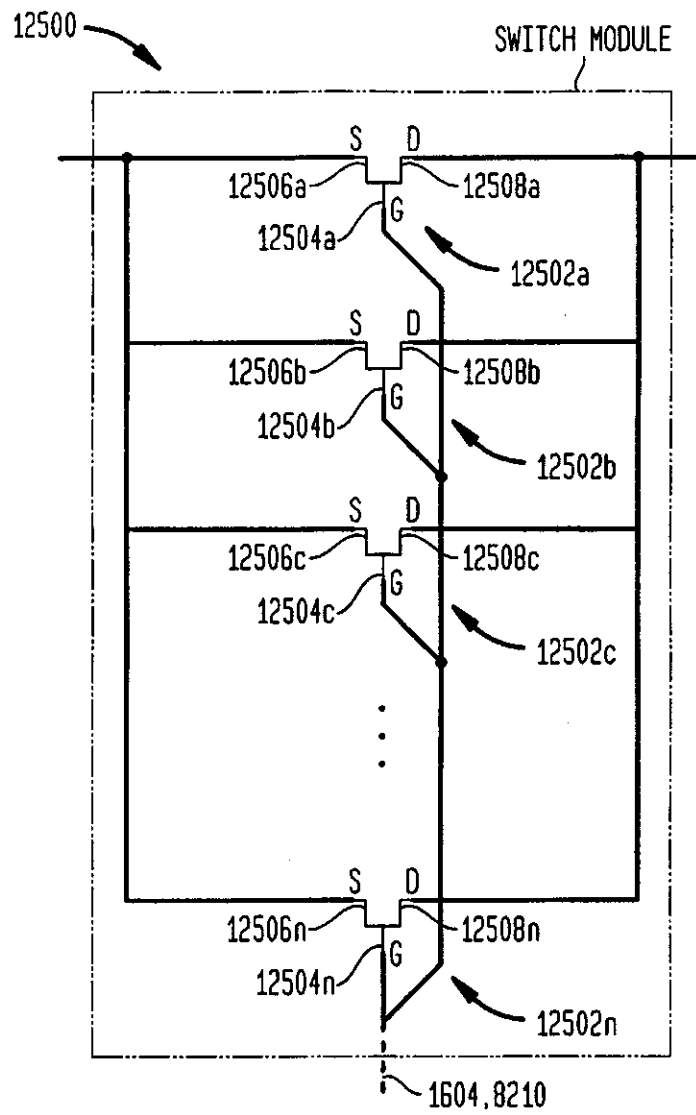
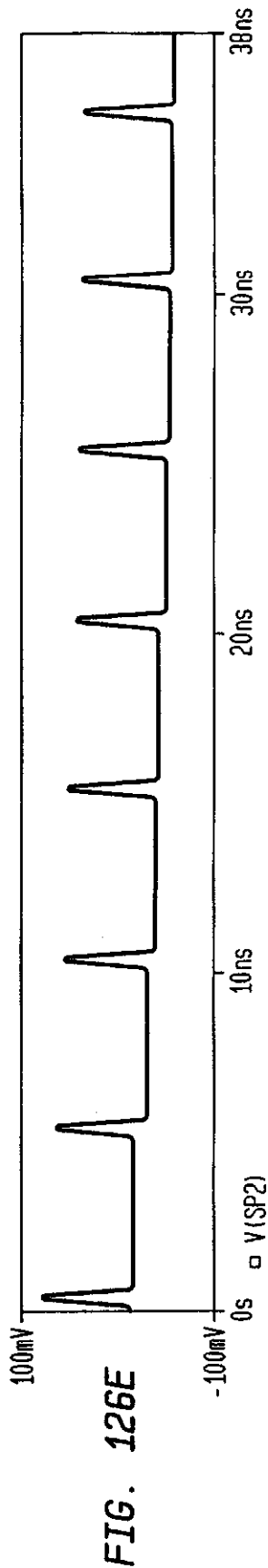
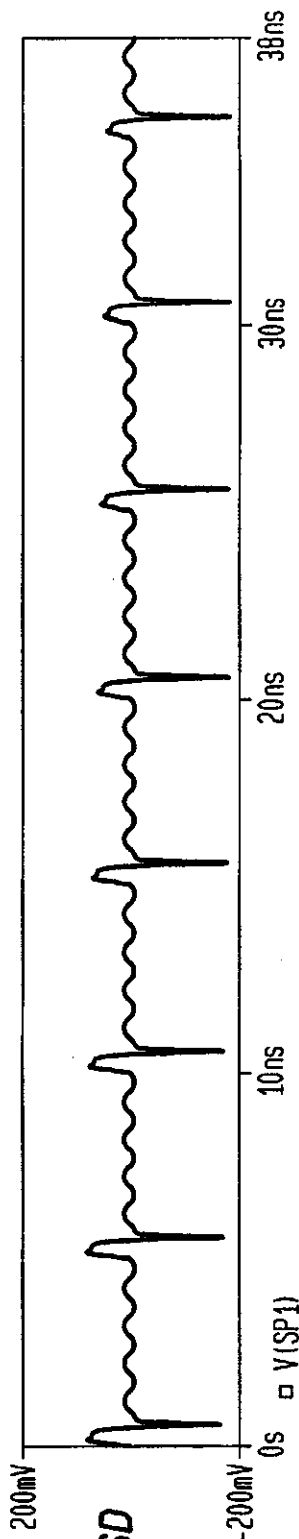
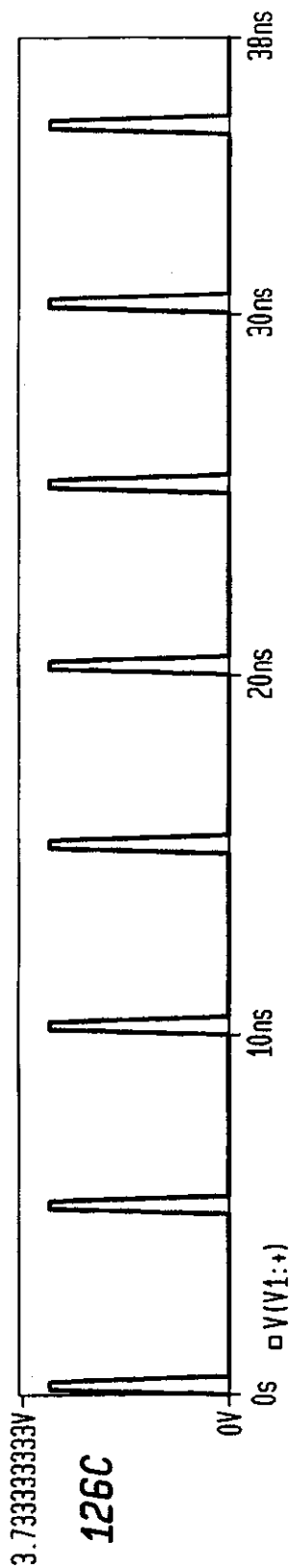
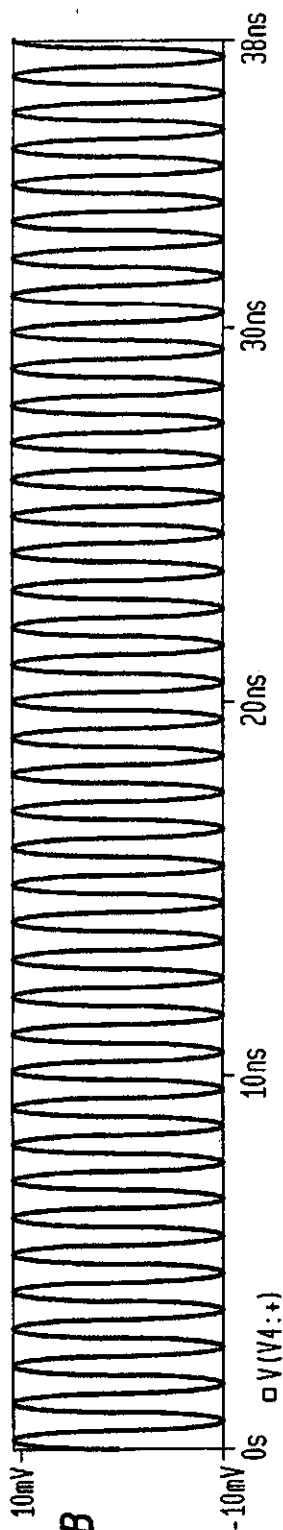
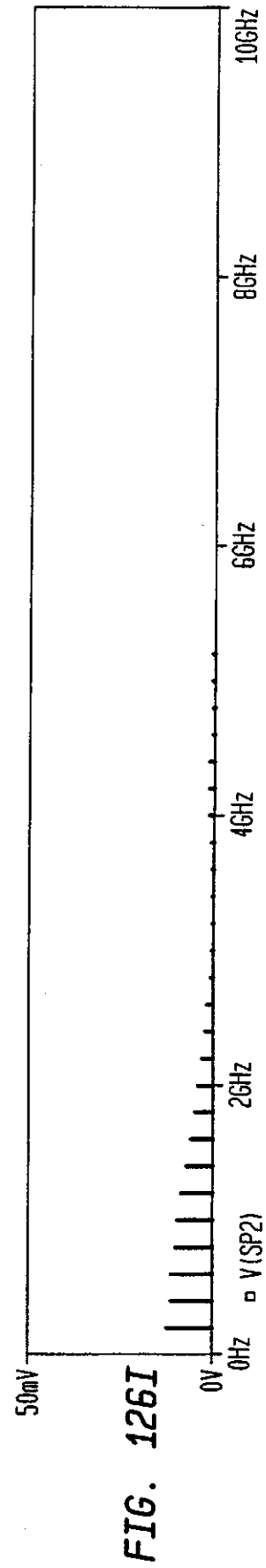
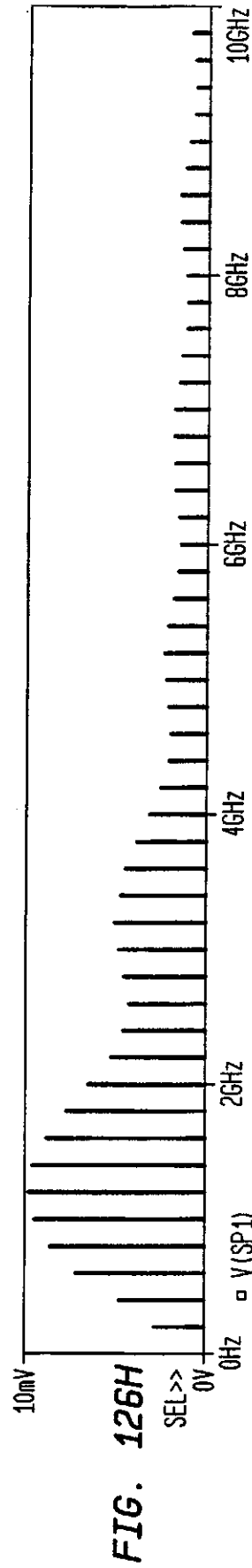
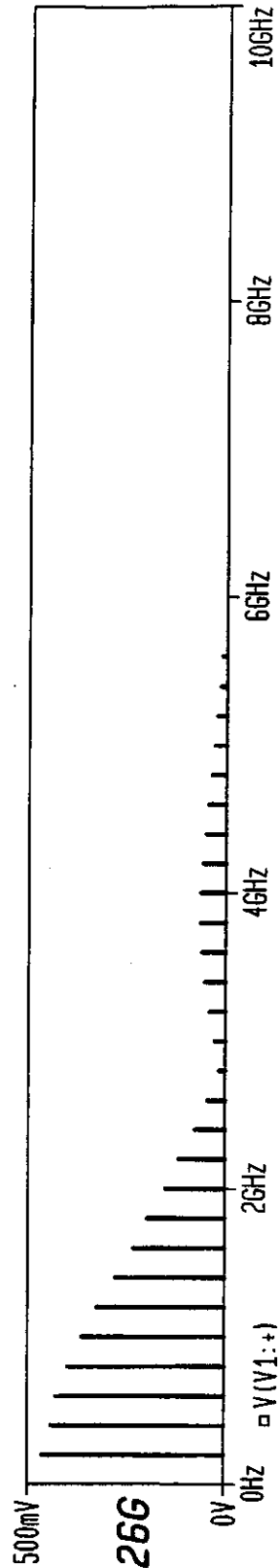
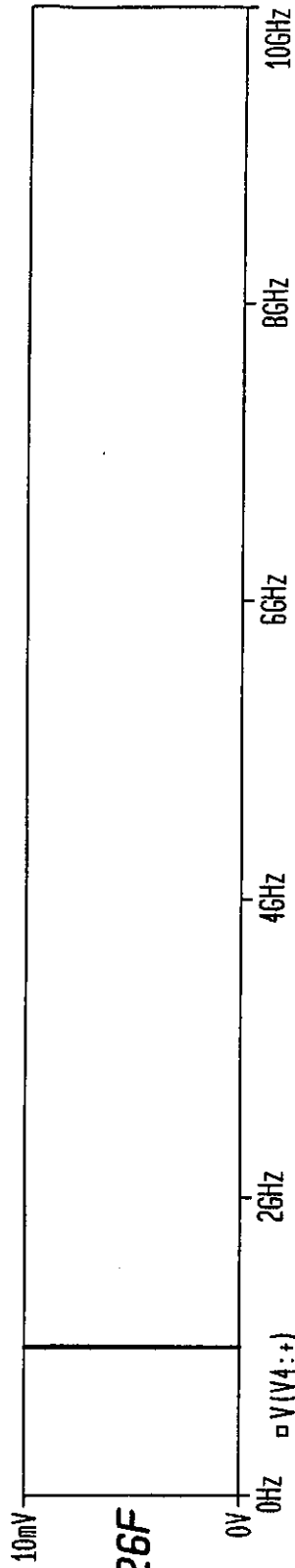
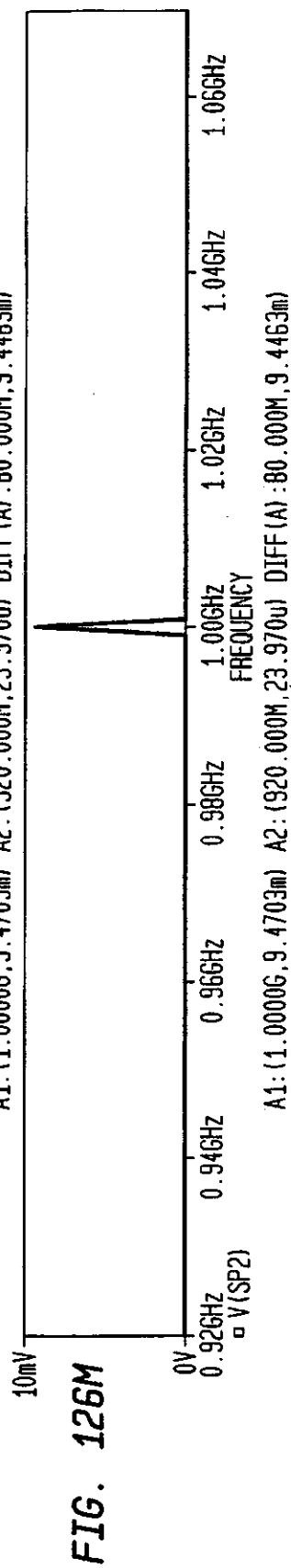
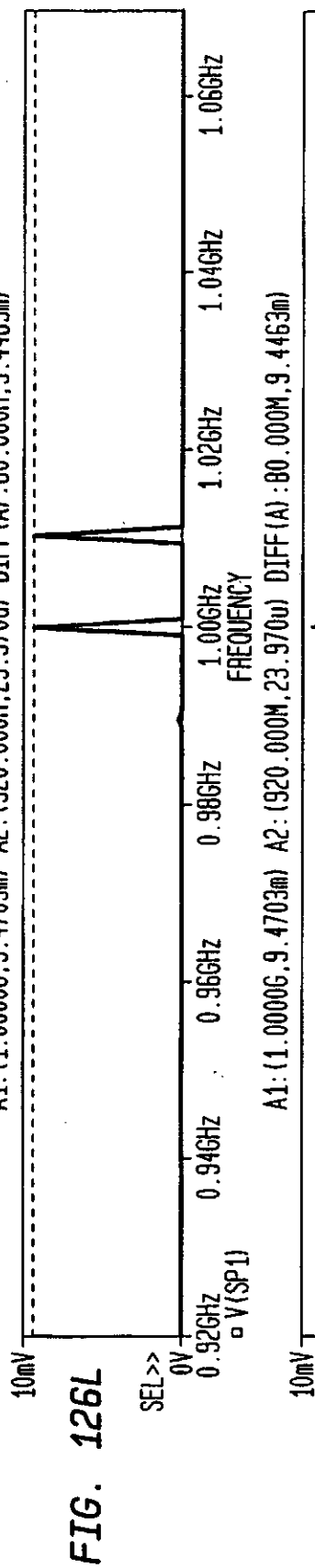
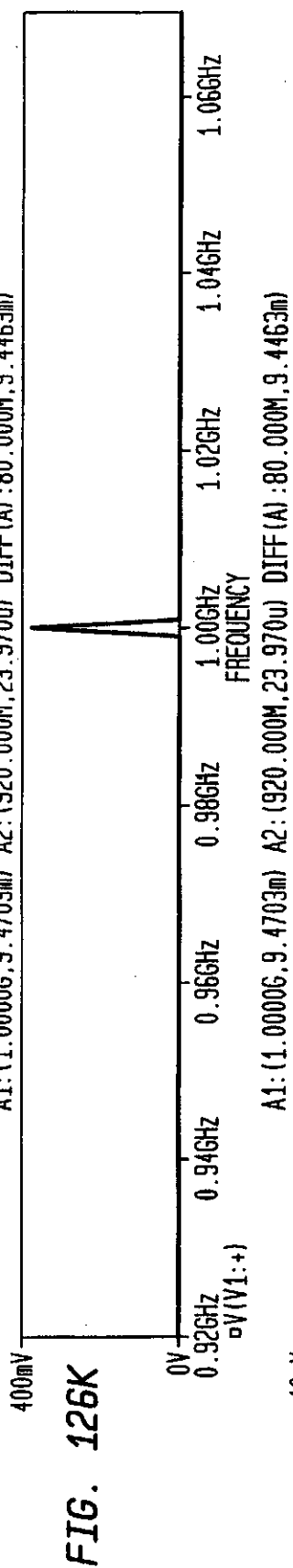
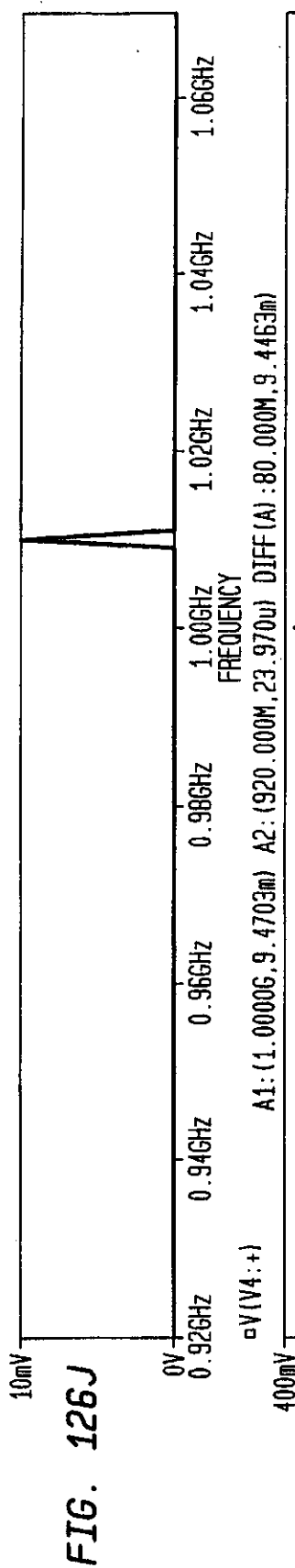


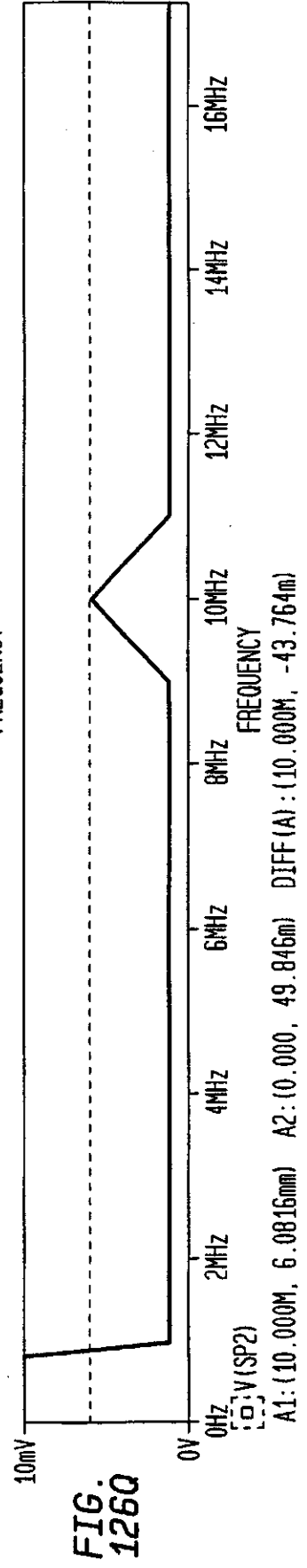
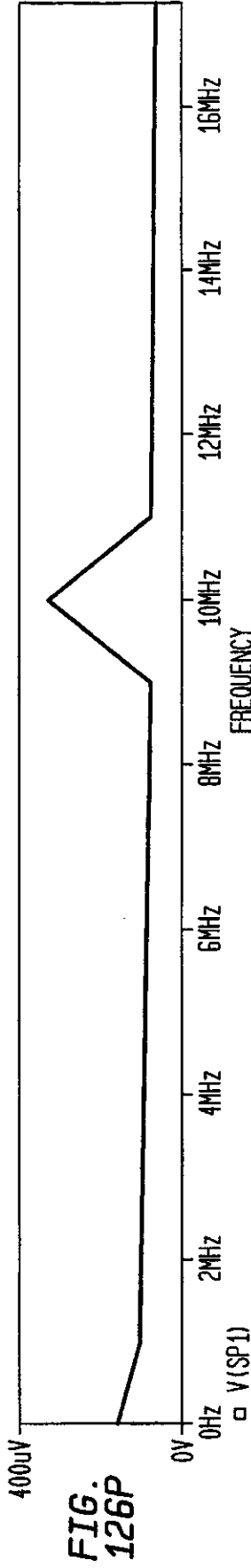
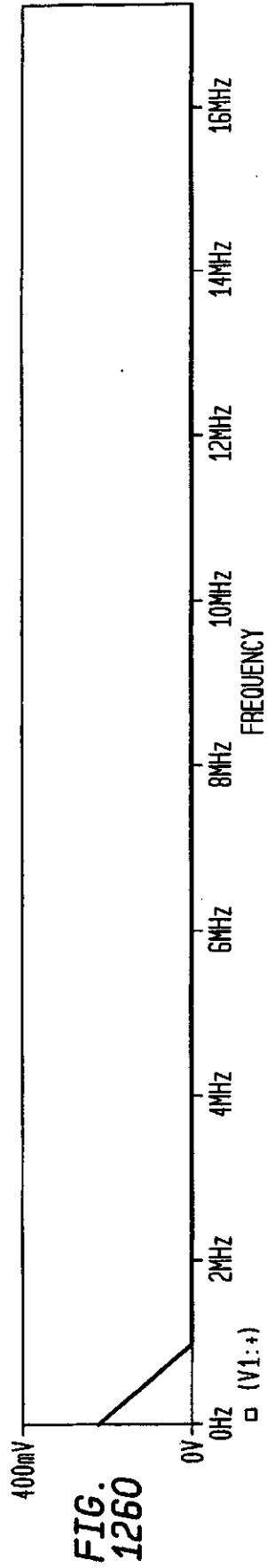
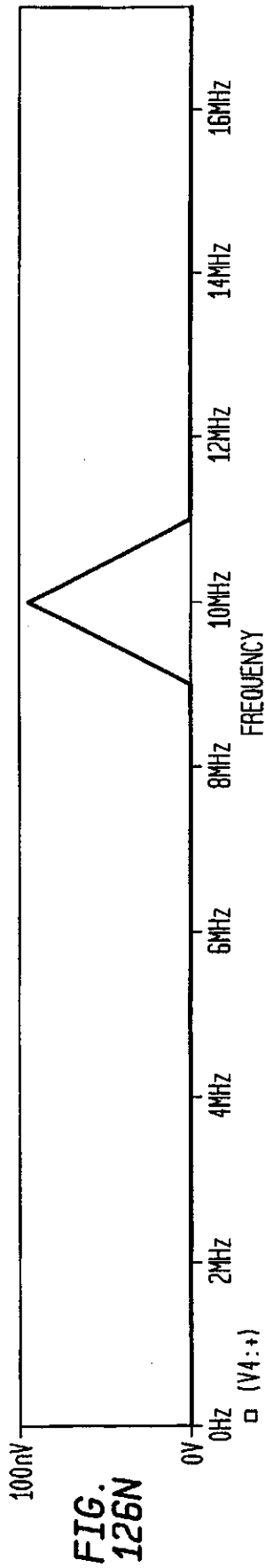
FIG. 126A





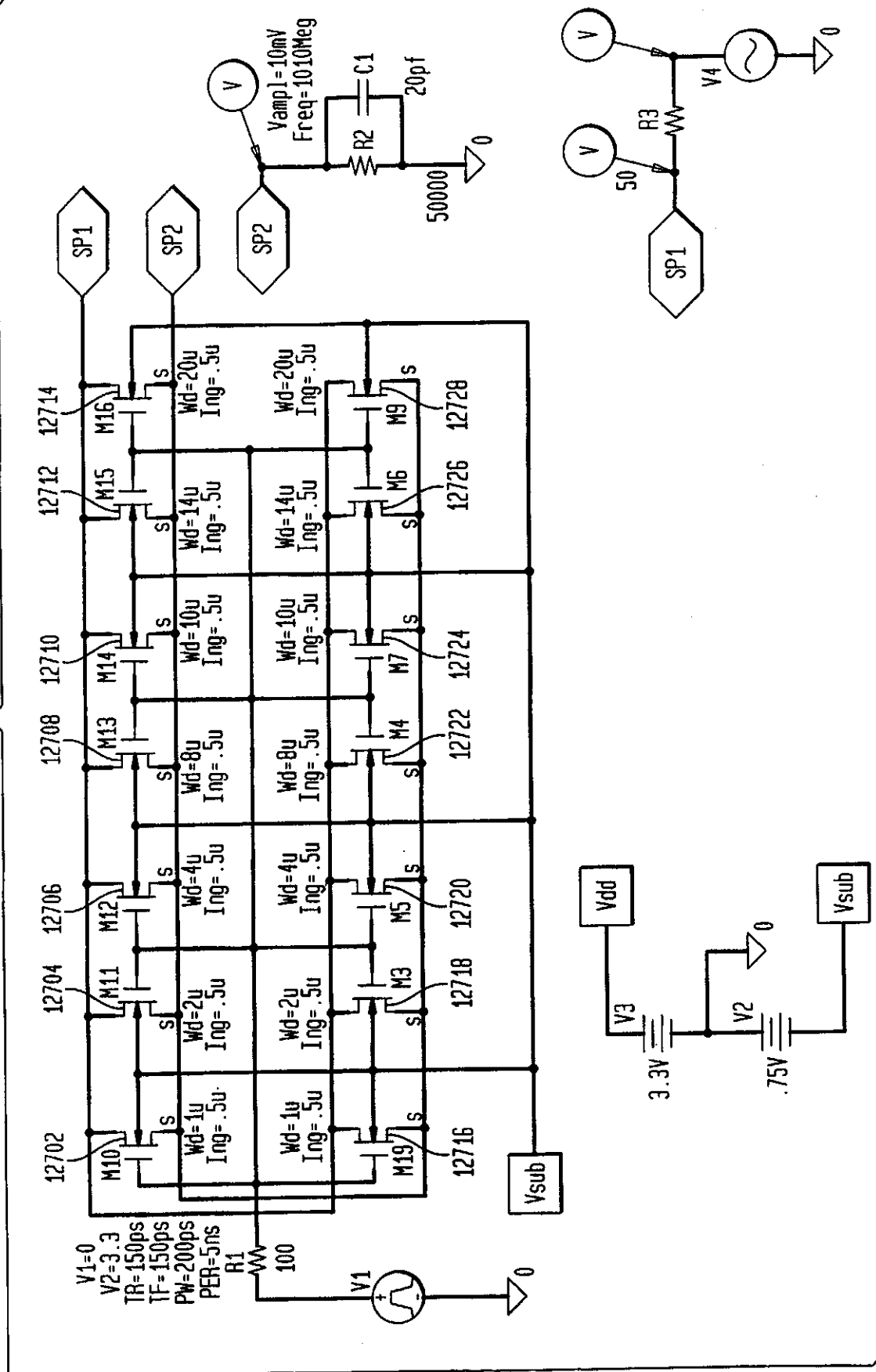






154/283

FIG. 127A



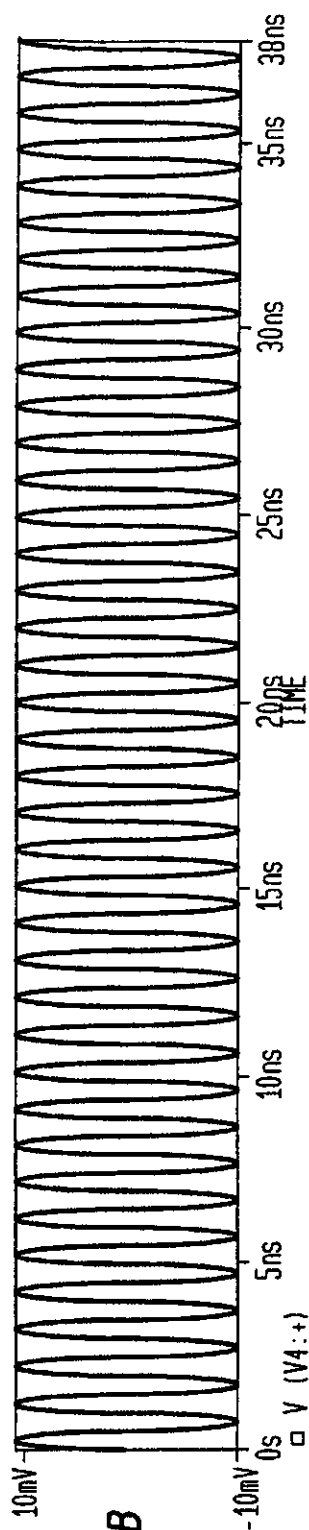


FIG. 127B

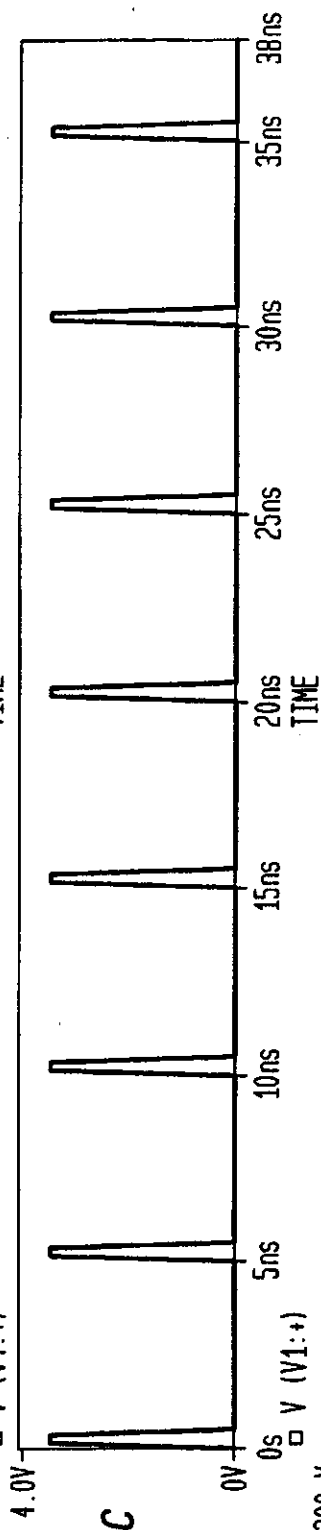


FIG. 127C

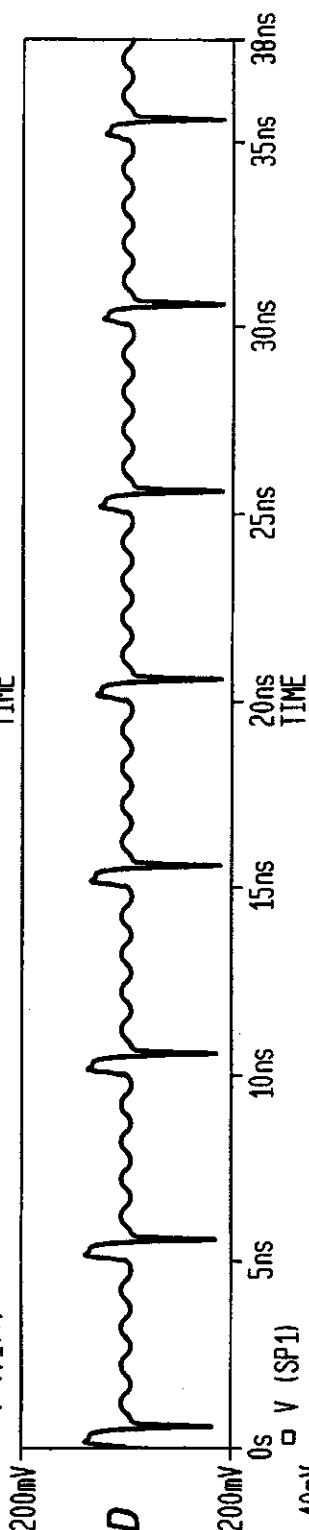


FIG. 127D

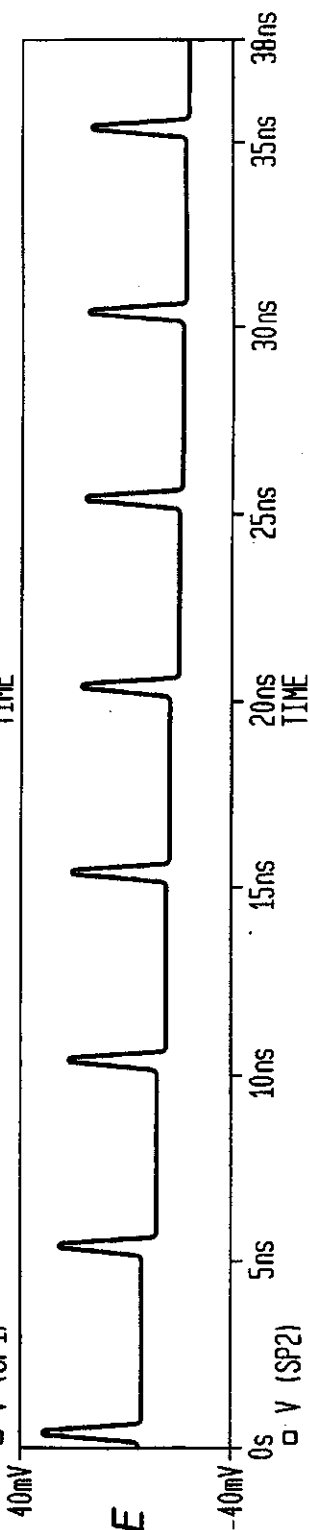


FIG. 127E

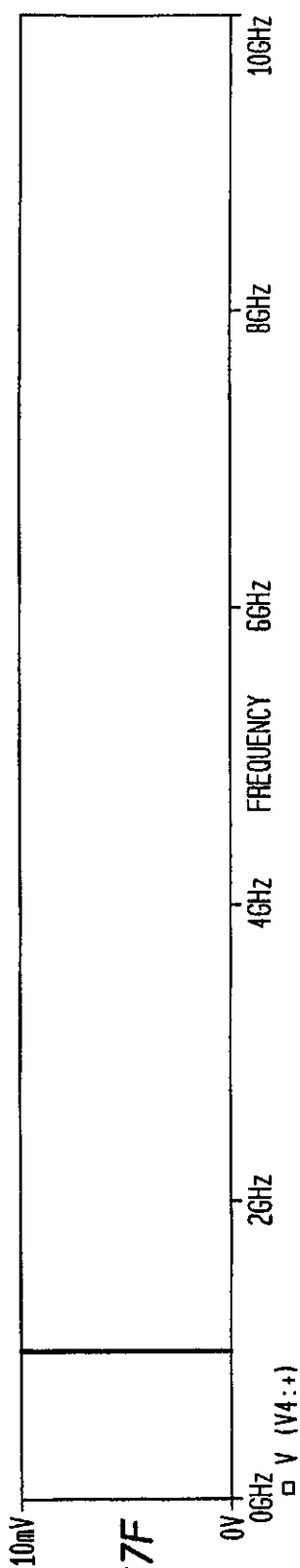


FIG. 127F

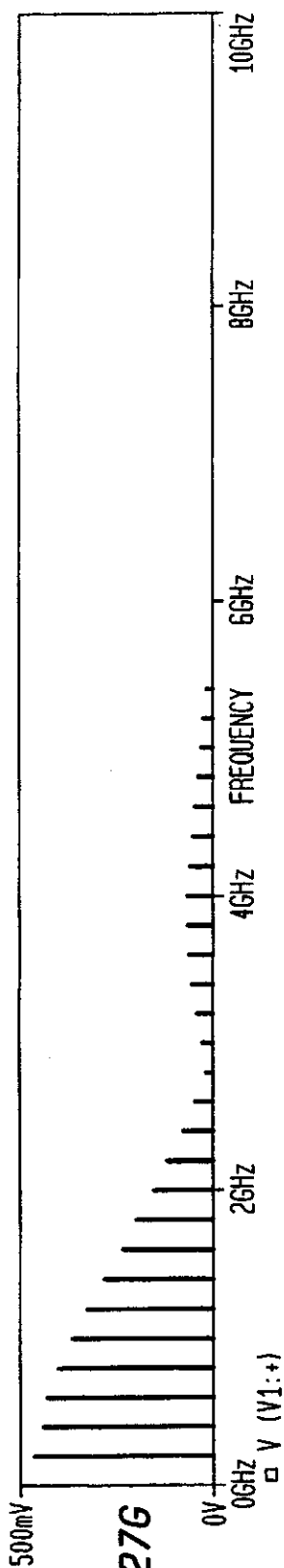


FIG. 127G

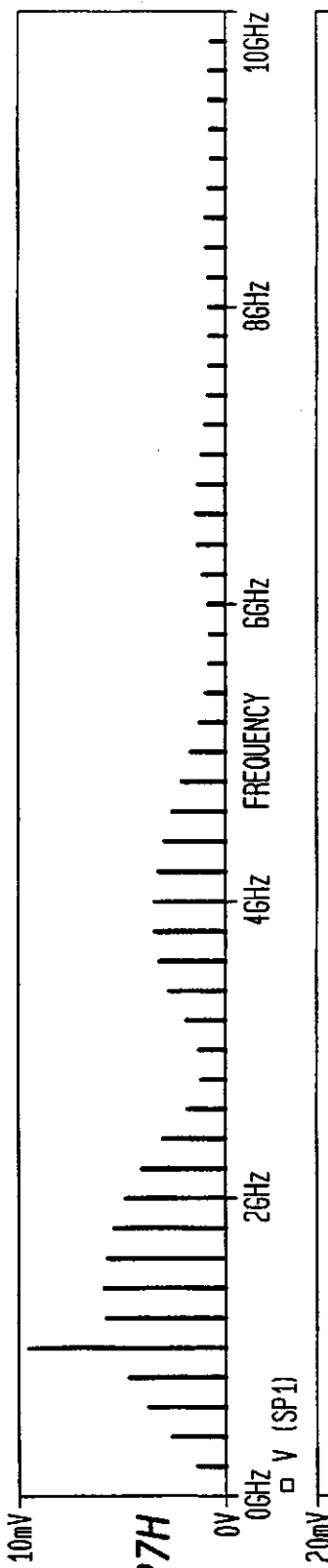


FIG. 127H

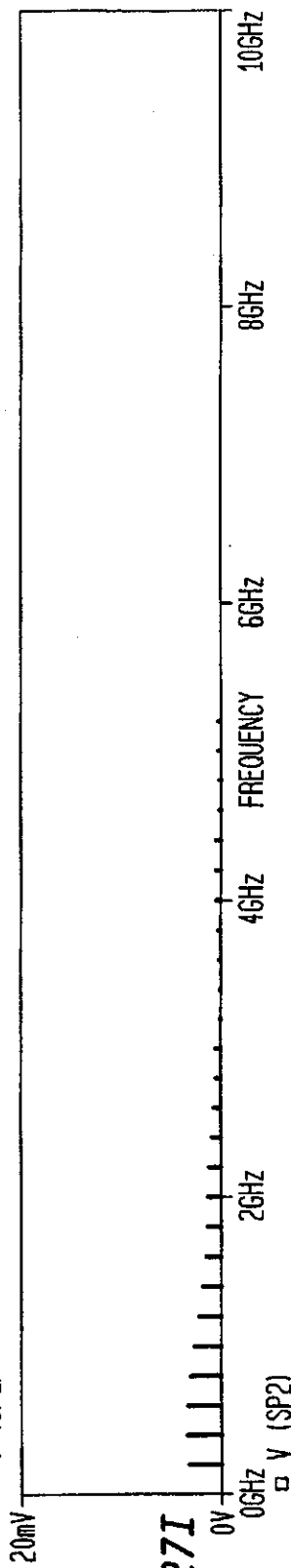
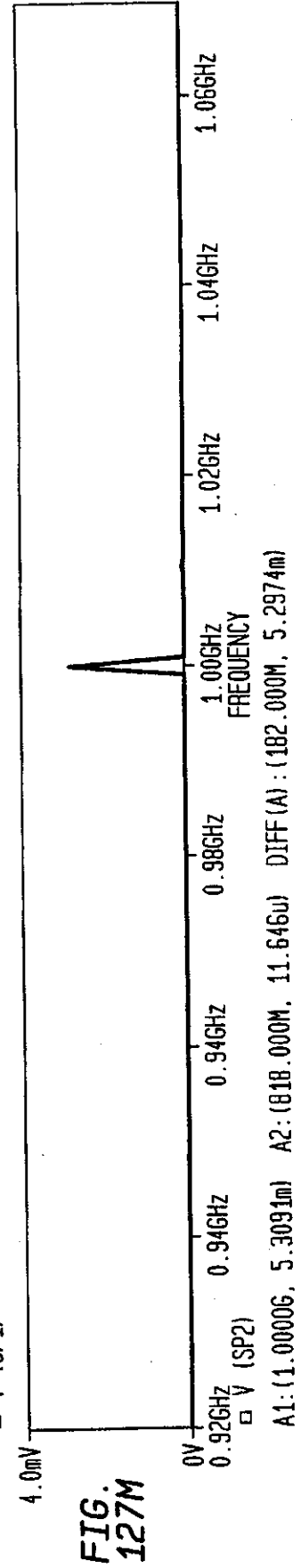
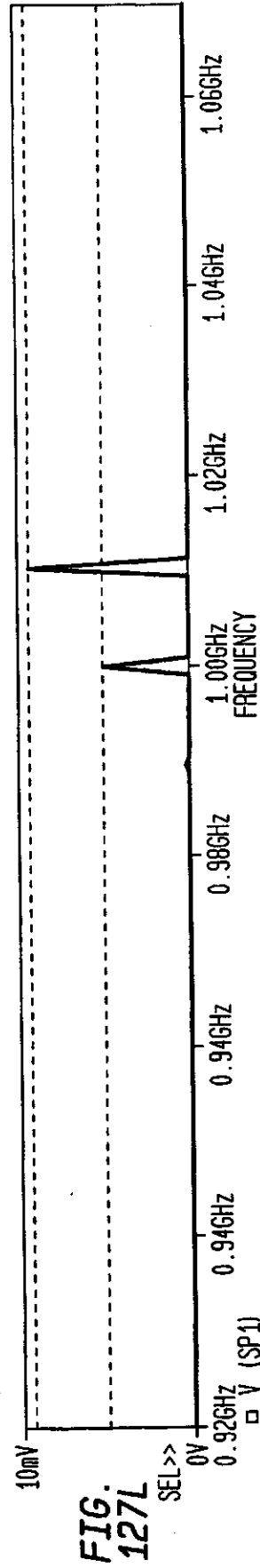
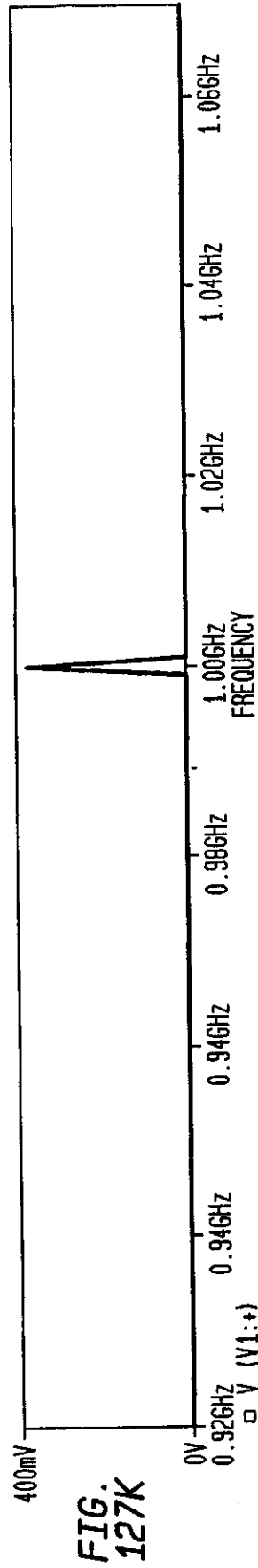
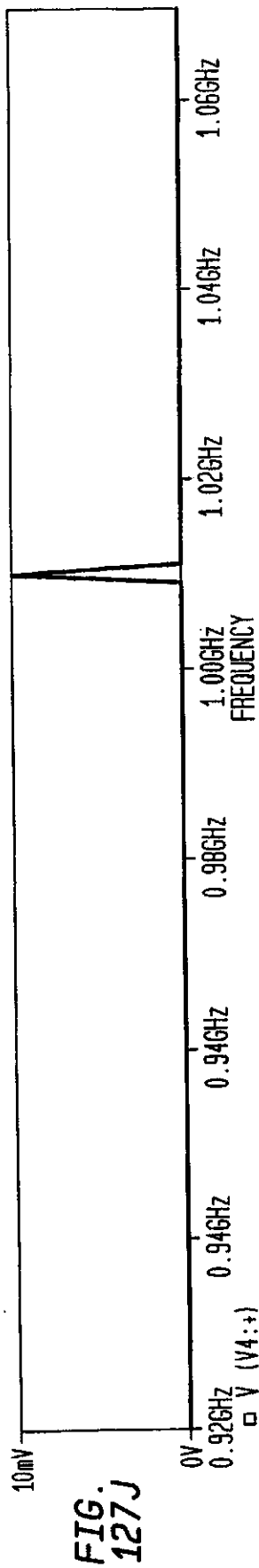


FIG. 127I



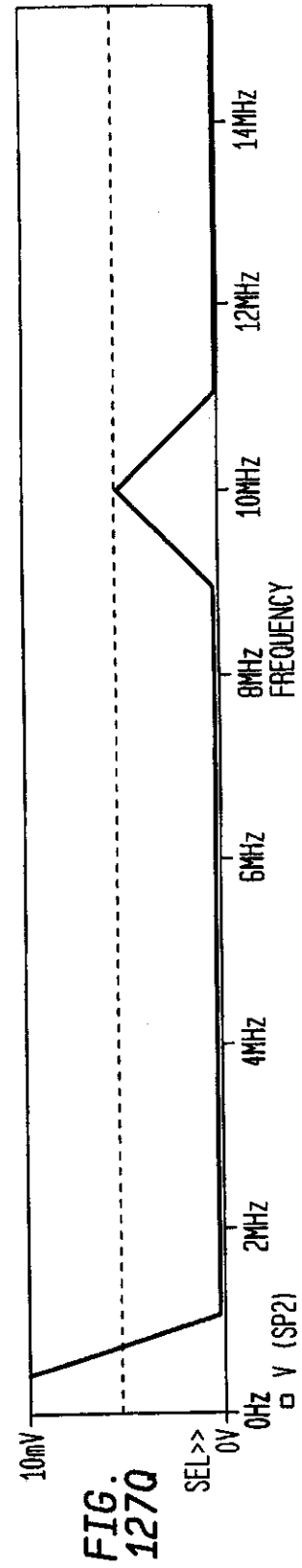
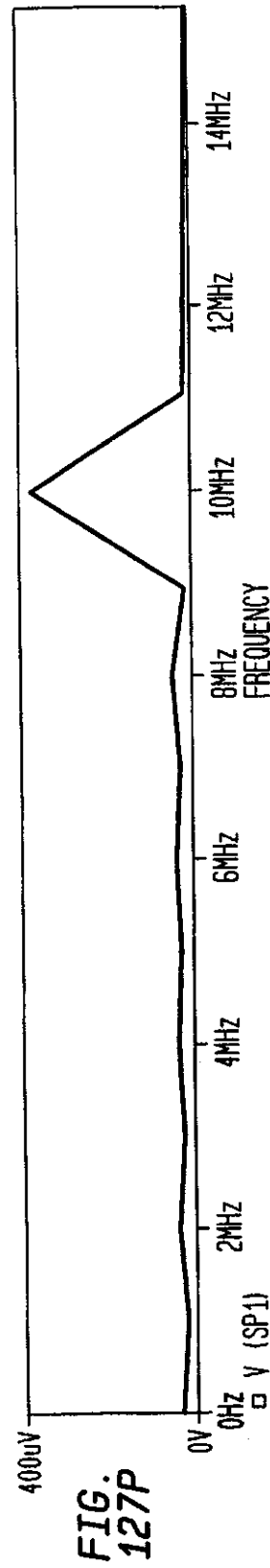
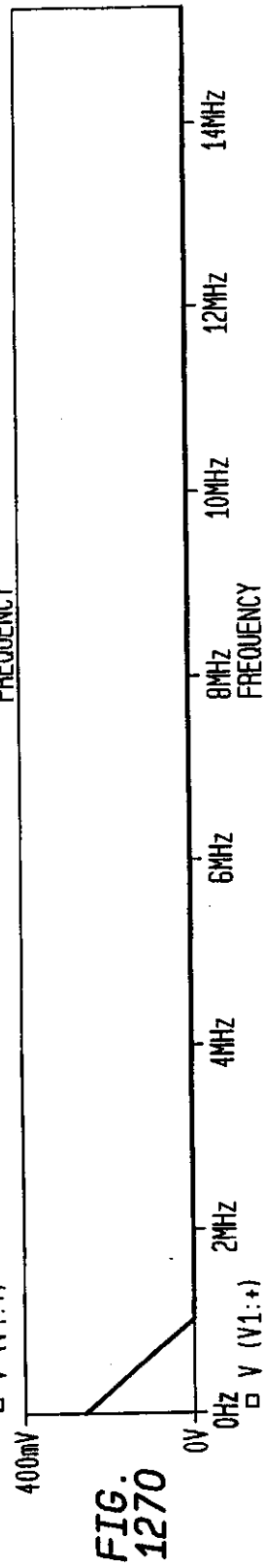
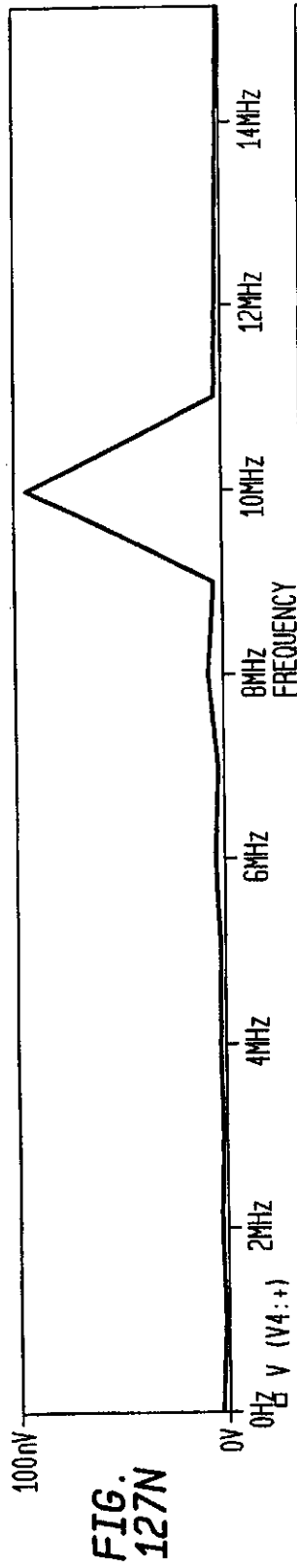


FIG. 128A

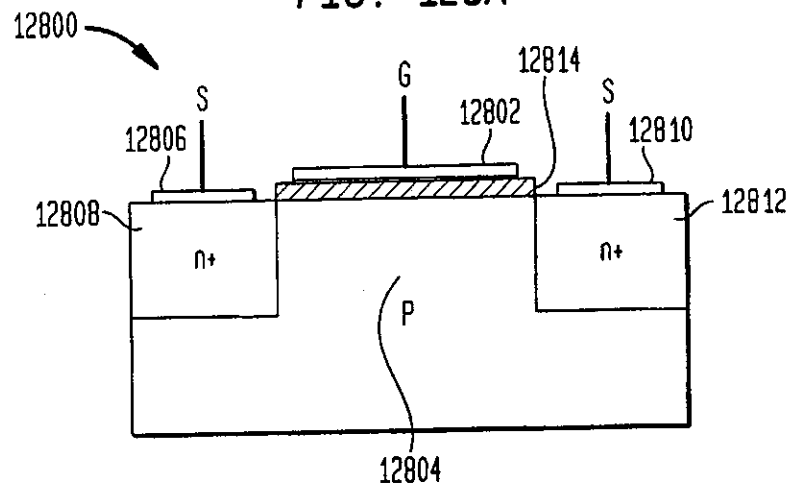


FIG. 128B

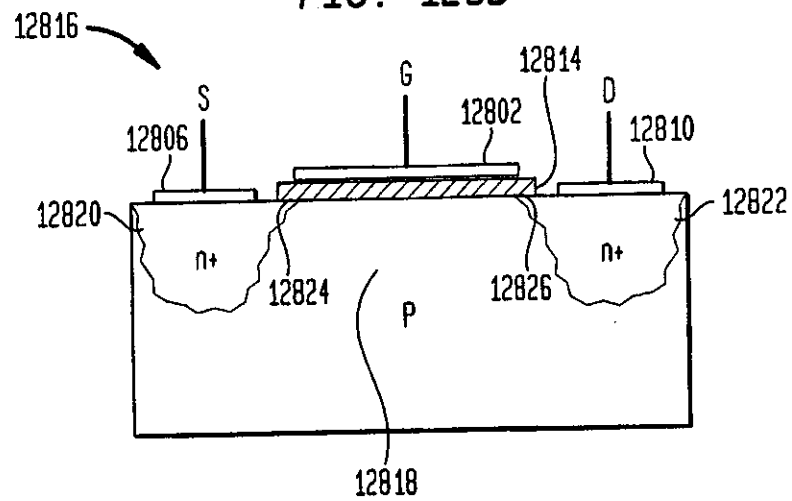
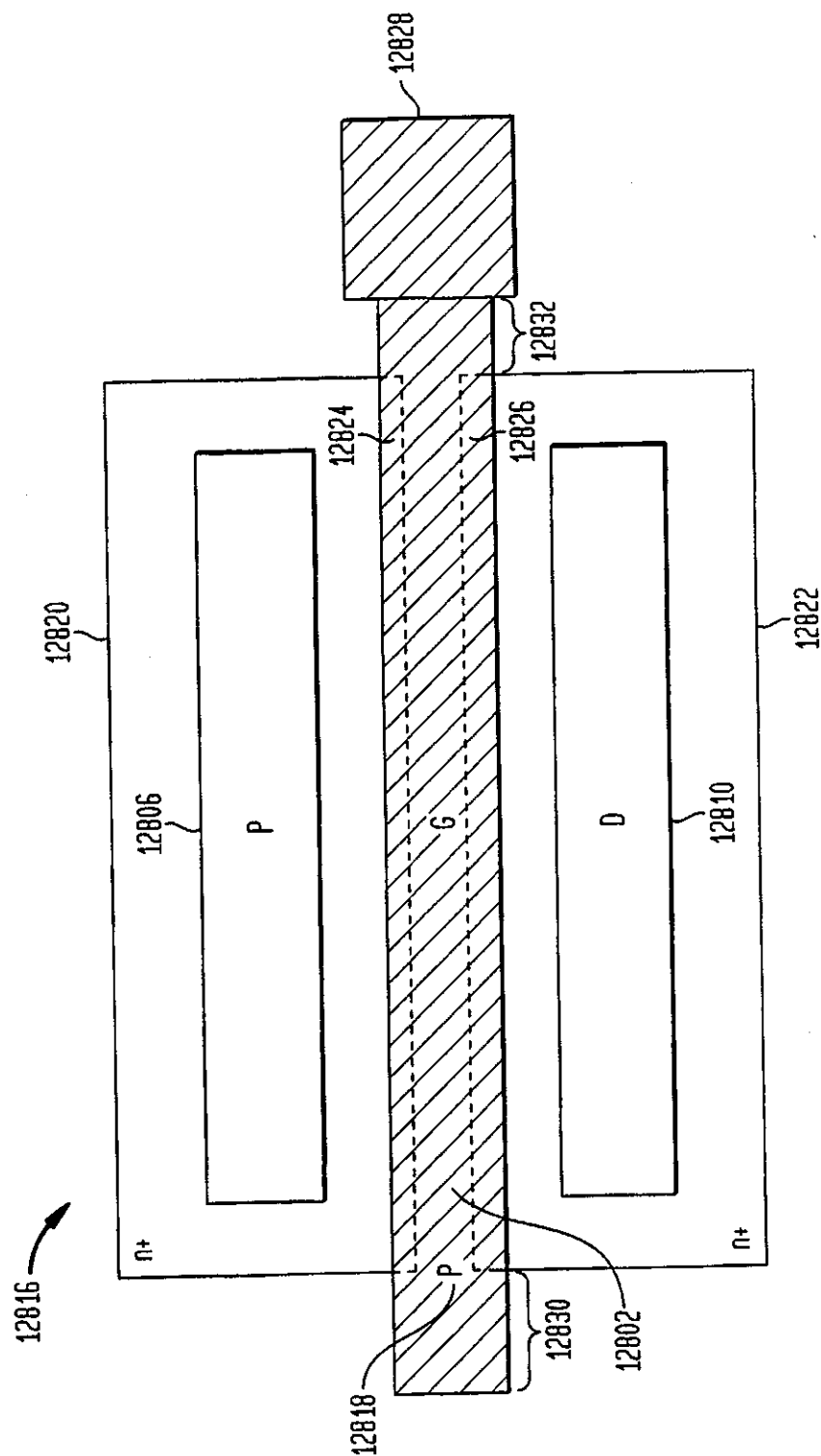
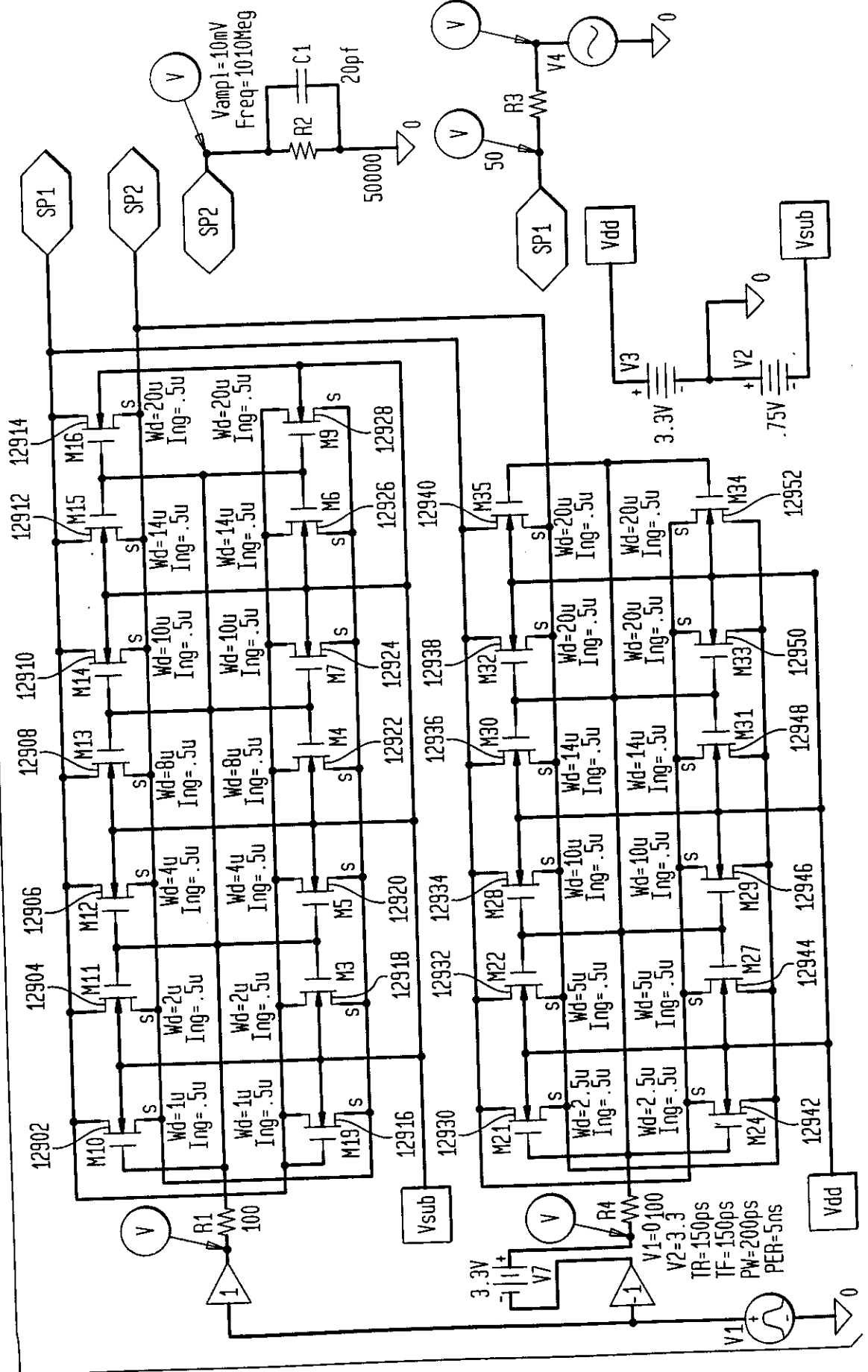


FIG. 128C



161/283

FIG. 129A



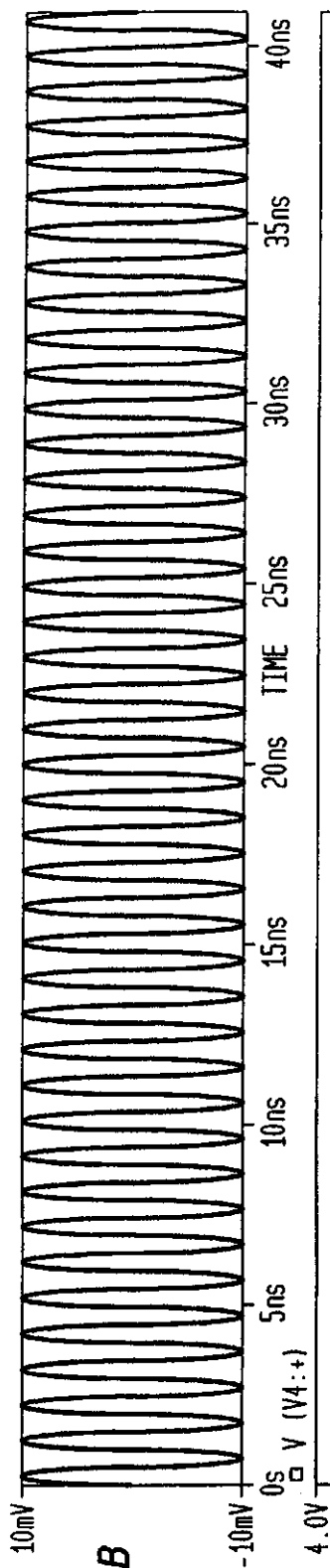


FIG. 129B

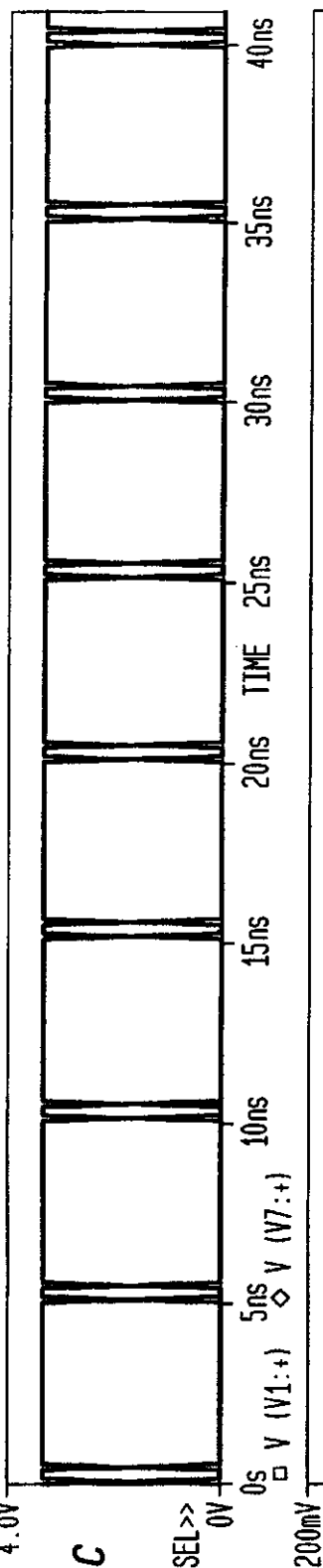


FIG. 129C

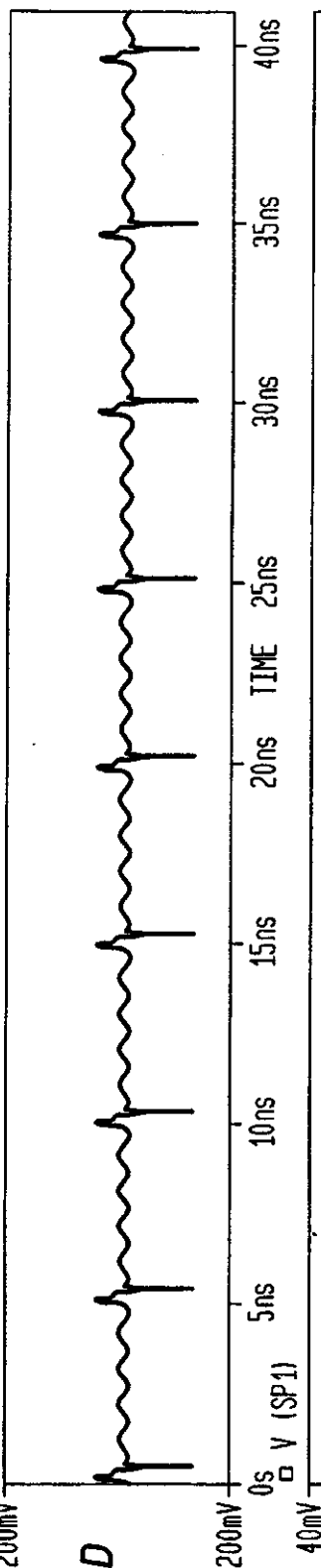


FIG. 129D

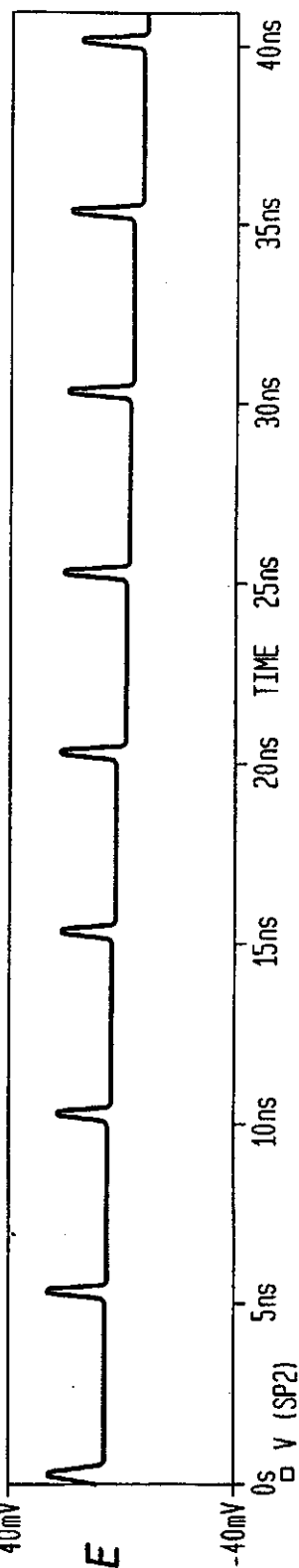
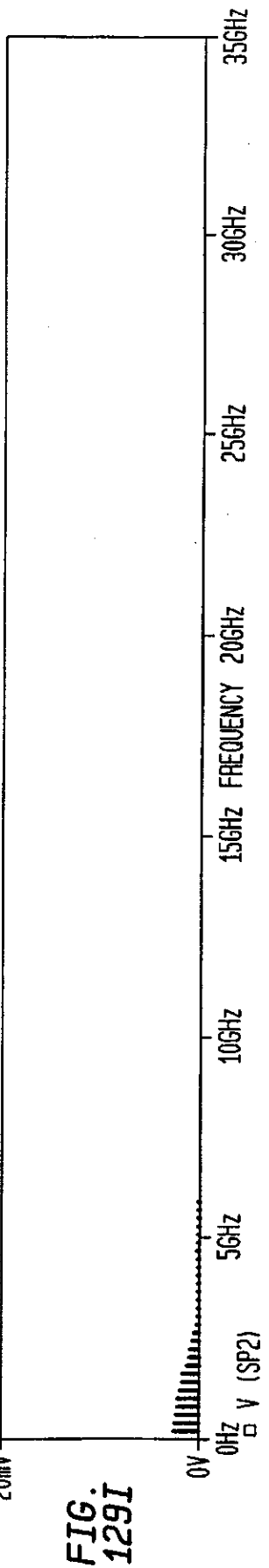
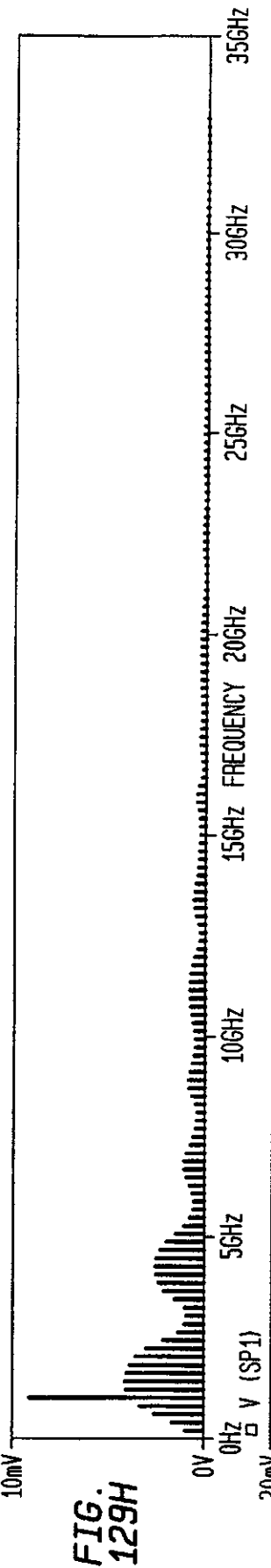
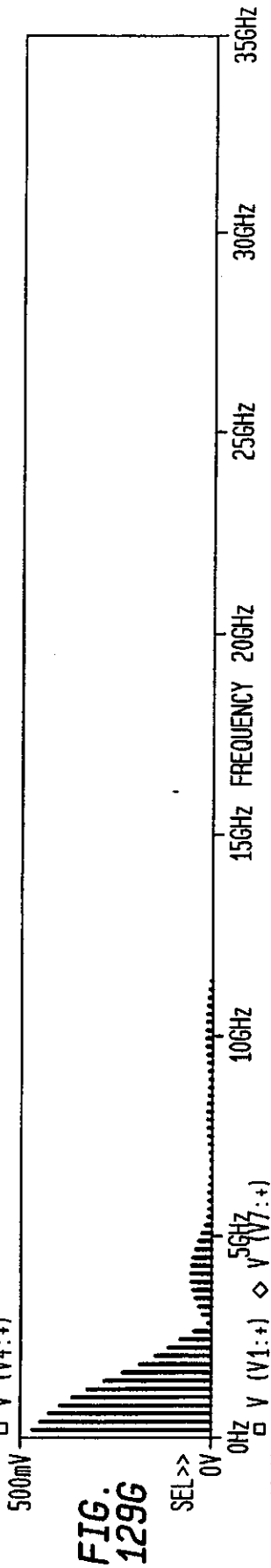
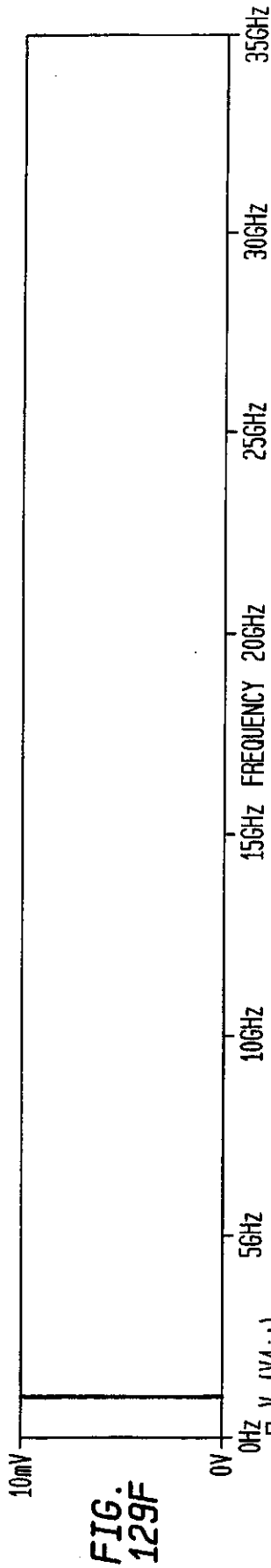
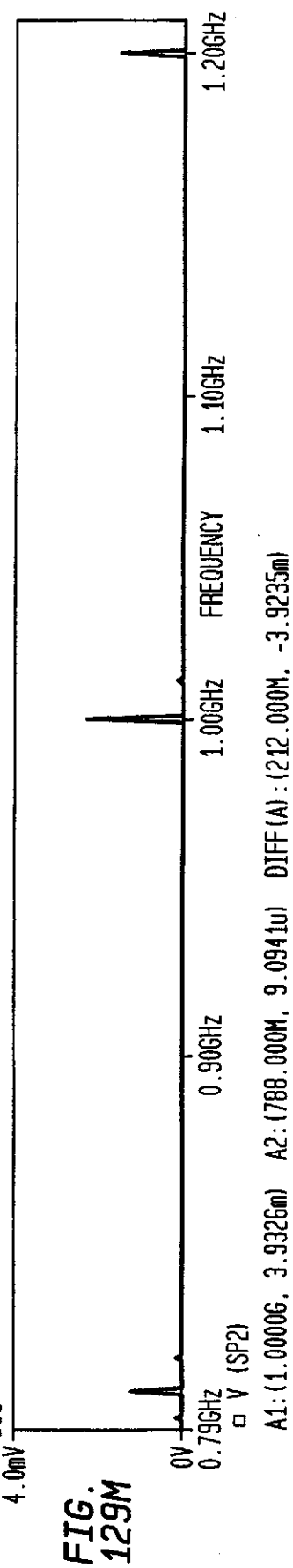
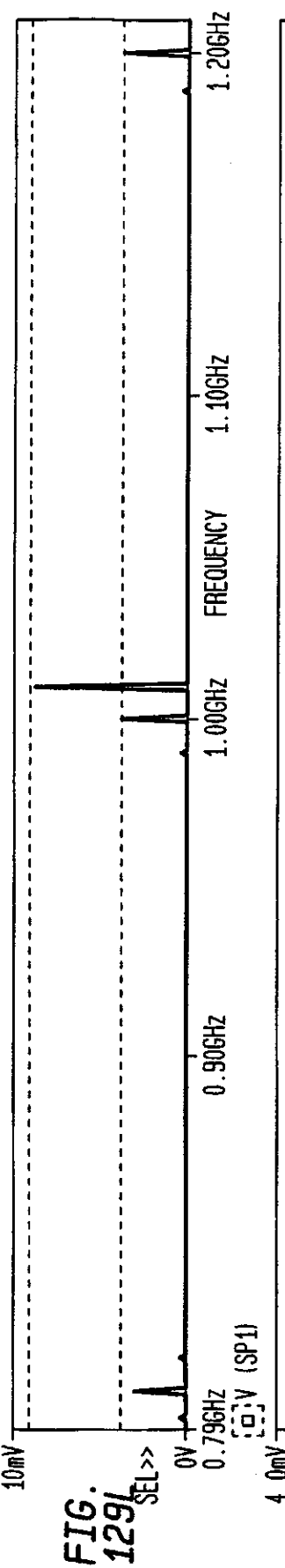
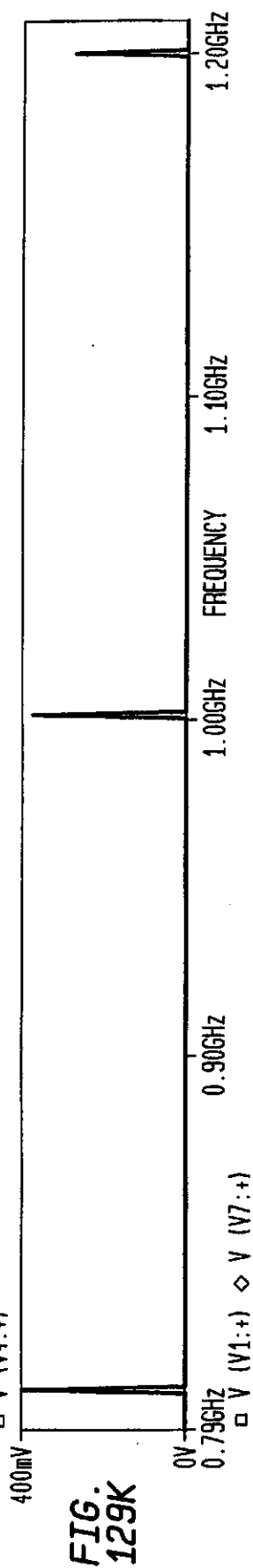
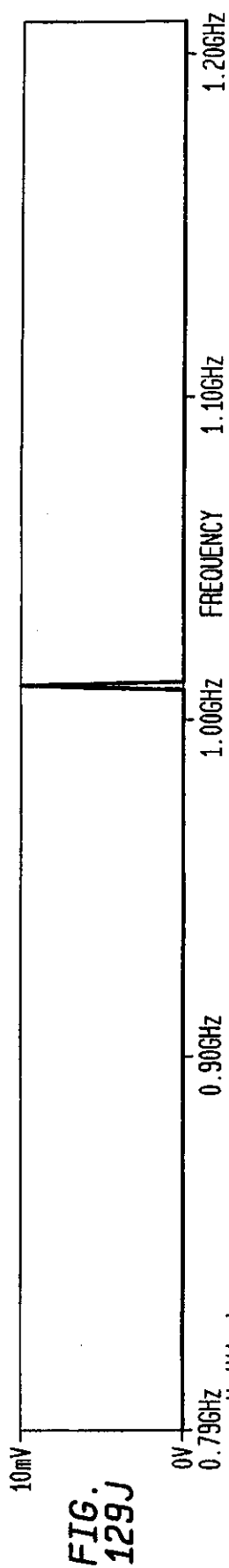


FIG. 129E

163/283



164/283



165/283

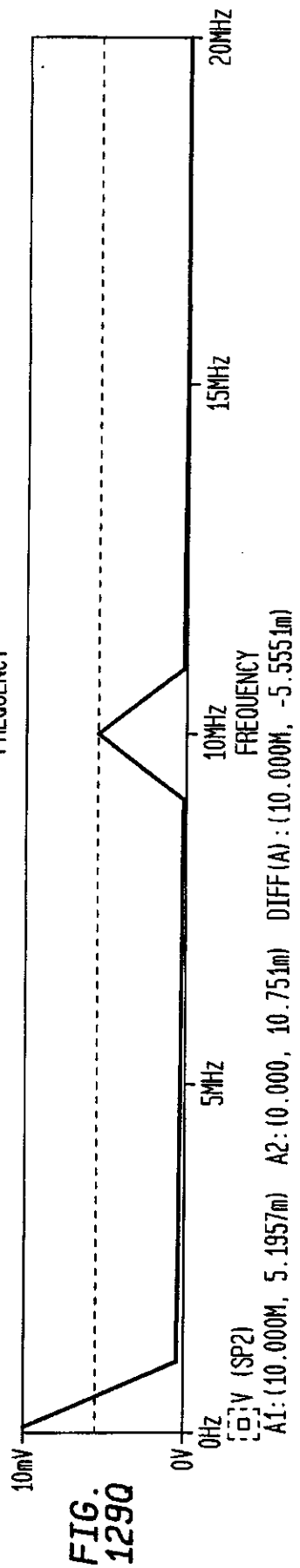
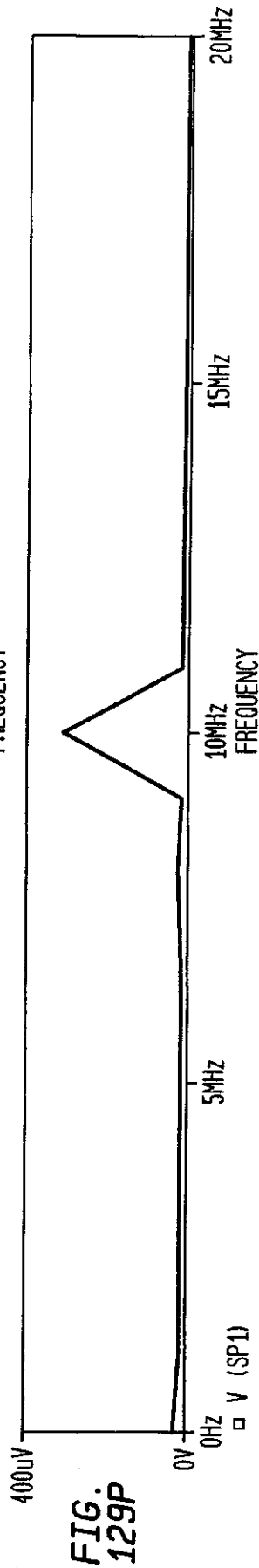
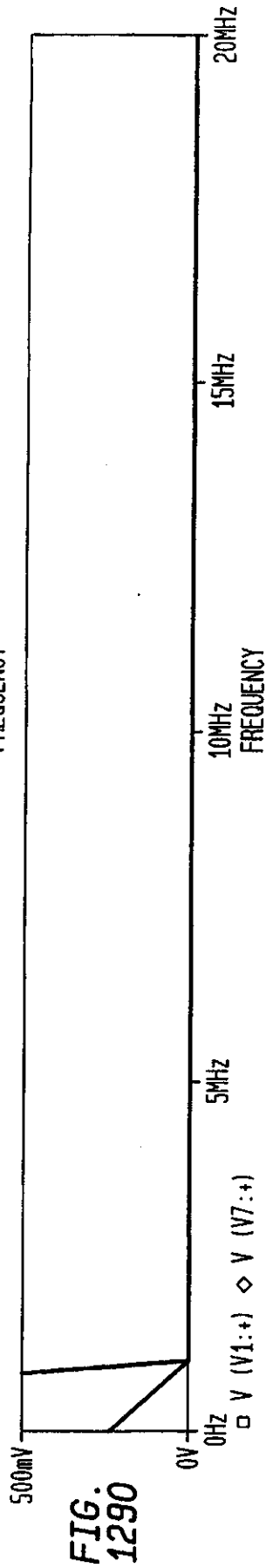
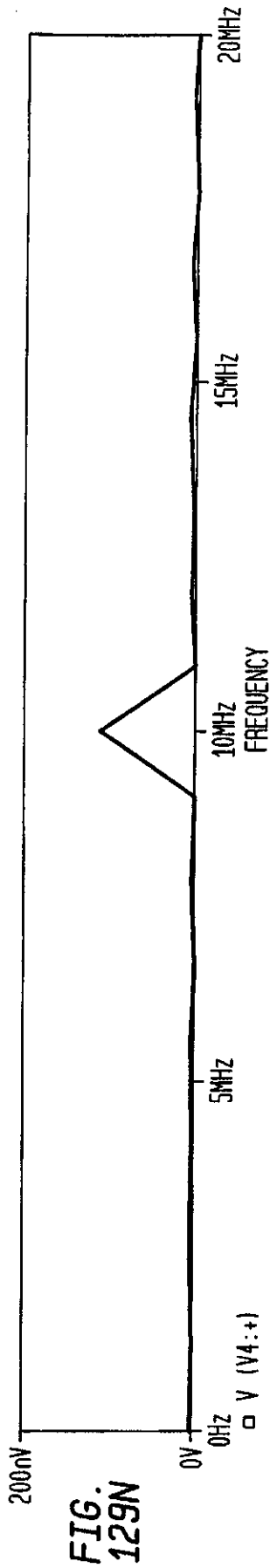


FIG. 130

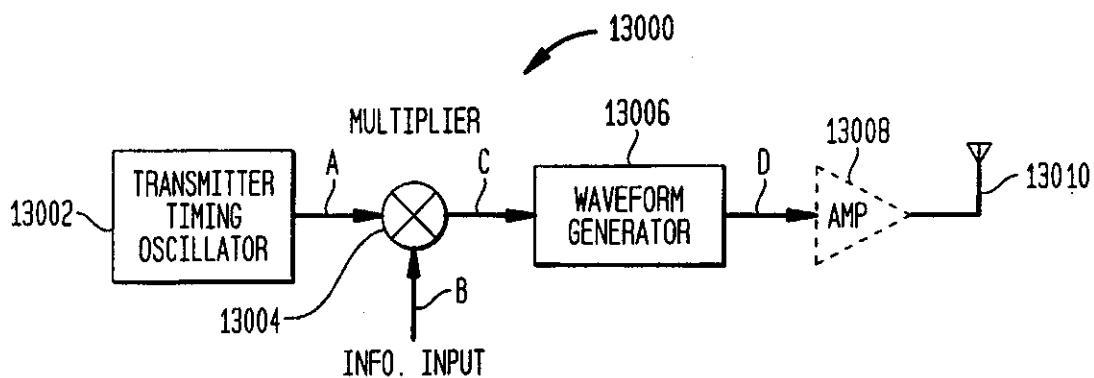


FIG. 131

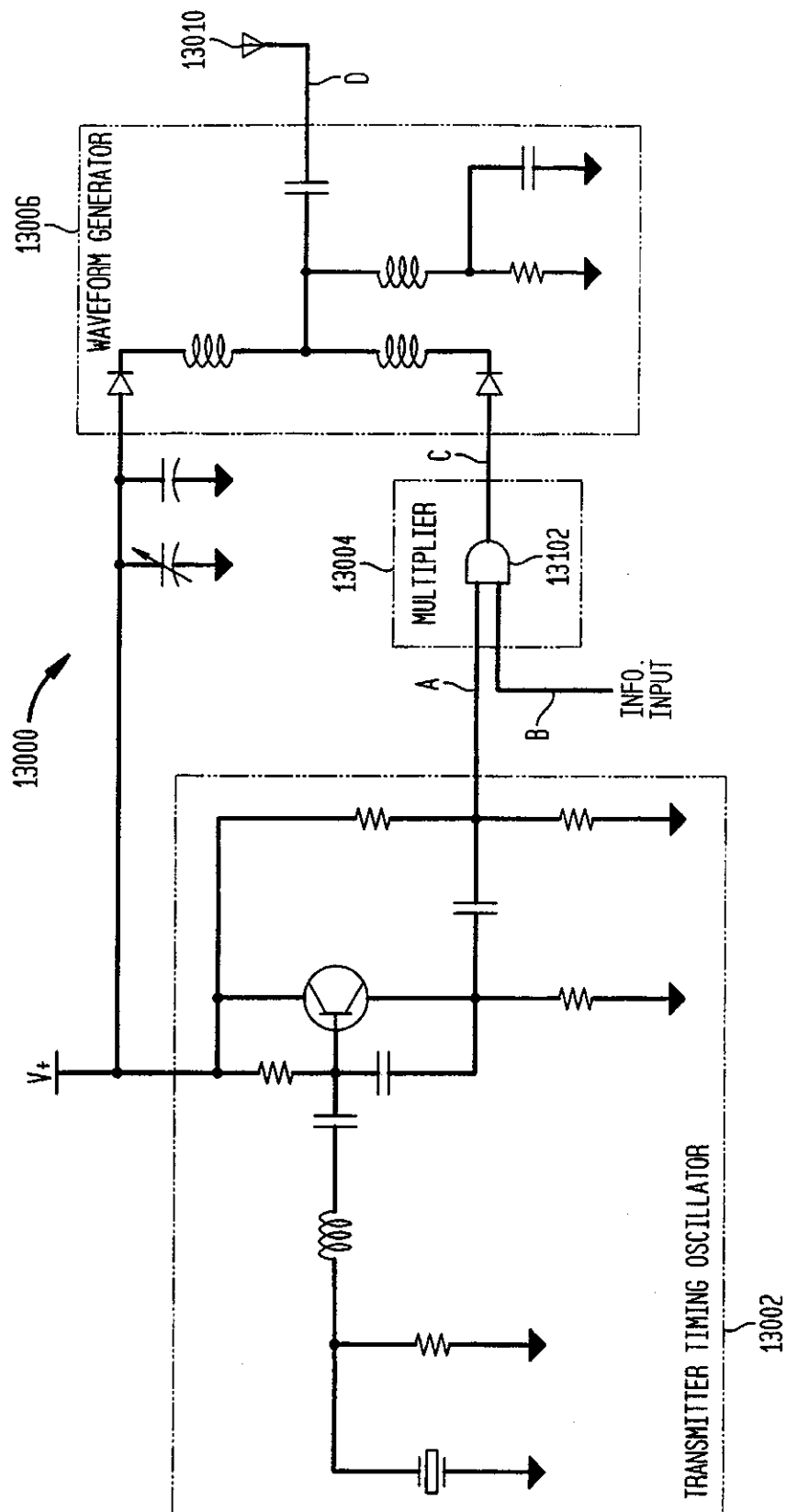


FIG. 132A

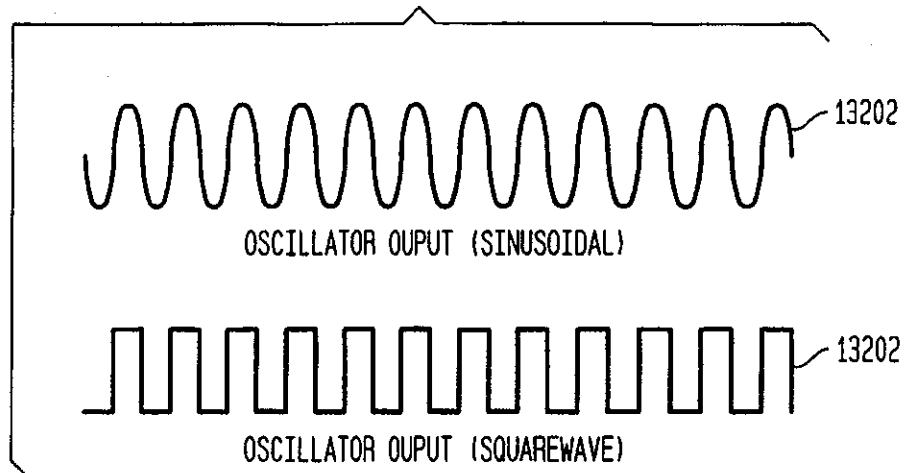


FIG. 132B

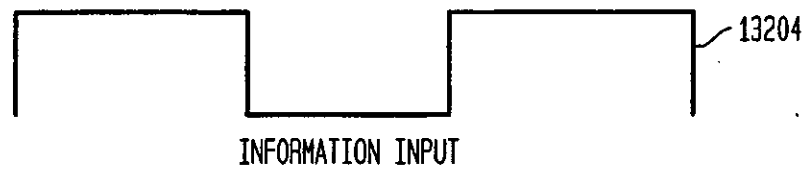


FIG. 132C

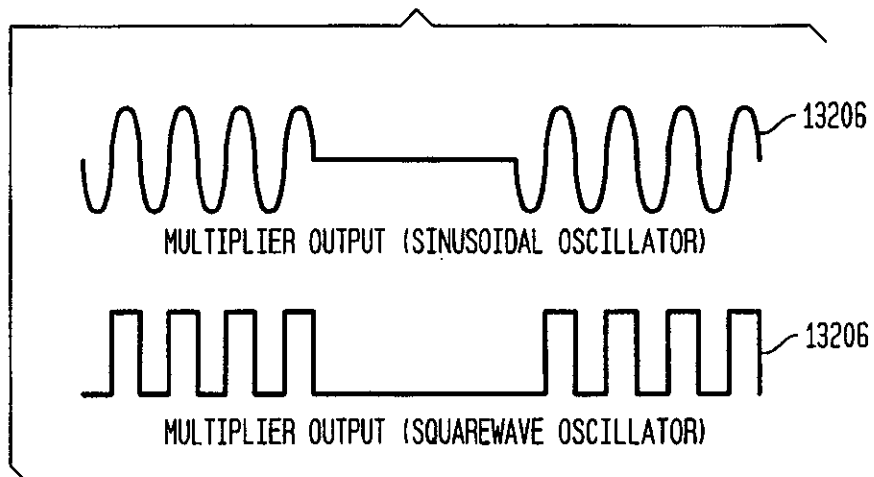


FIG. 132D

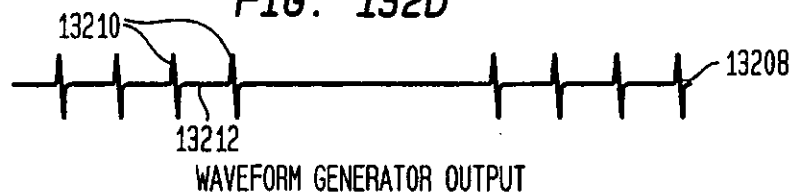
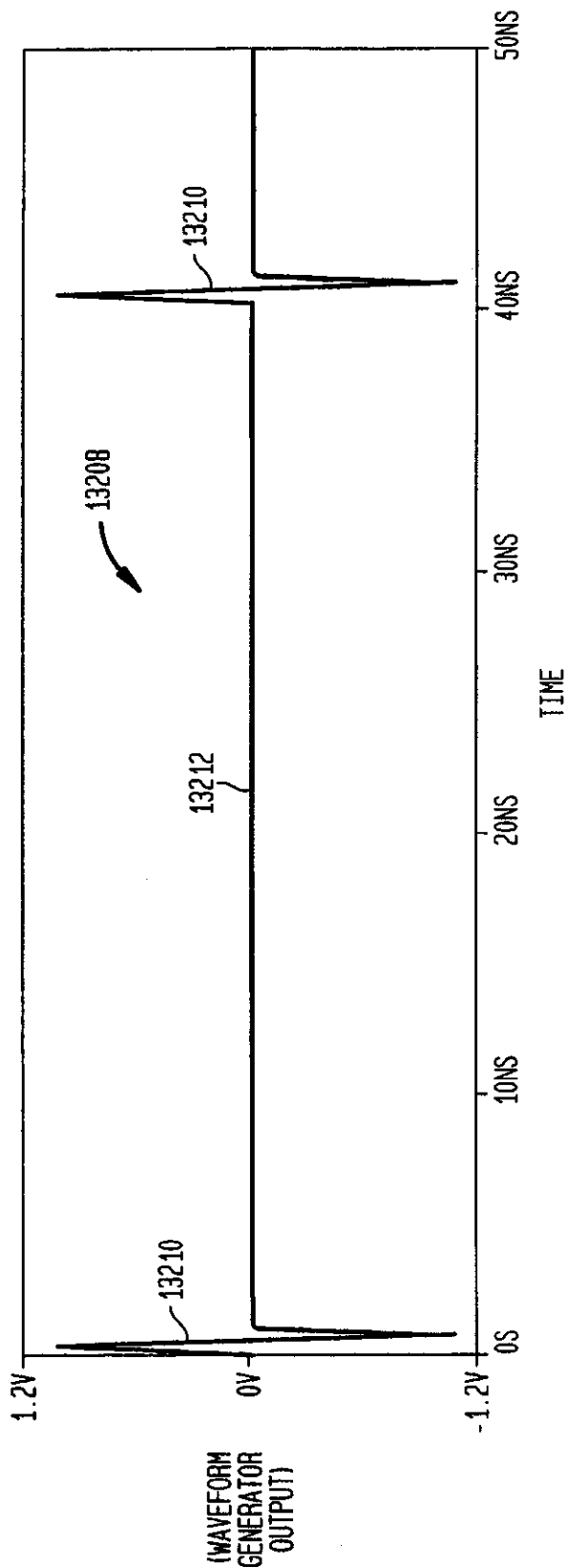


FIG. 133



170/283

FIG. 134

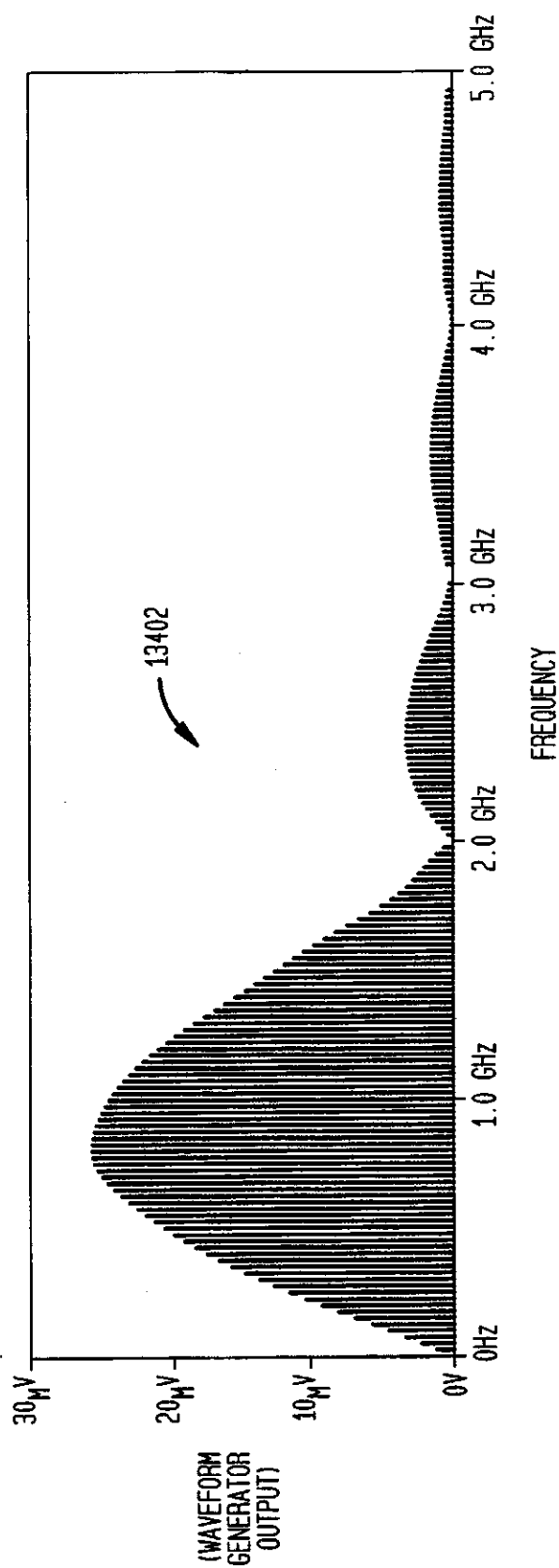
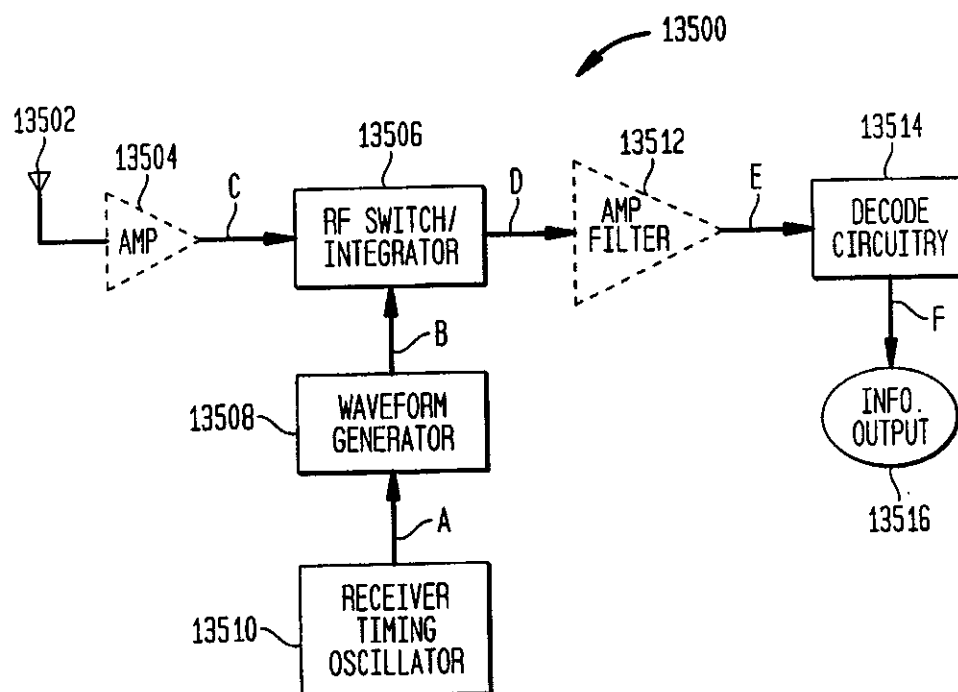


FIG. 135



172/283

FIG. 136A



FIG. 136B

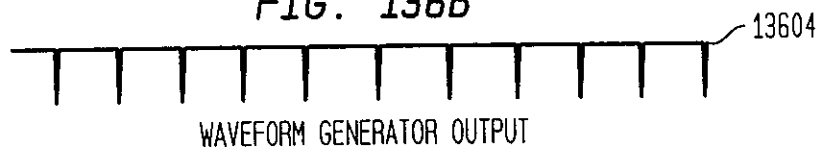


FIG. 136C

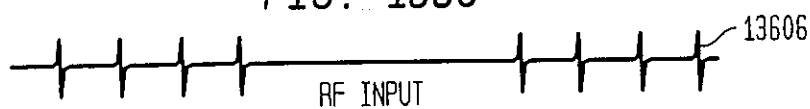


FIG. 136D

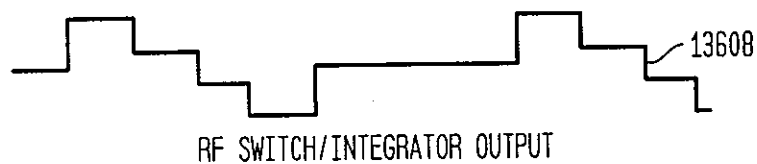


FIG. 136E

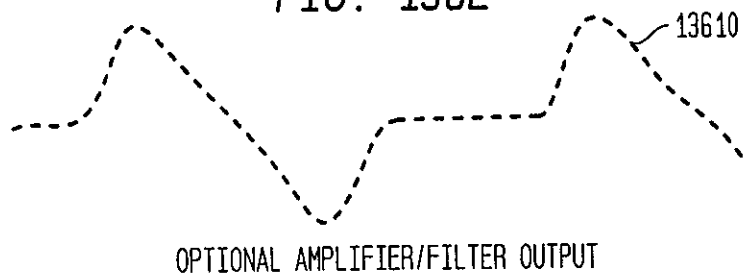


FIG. 136G

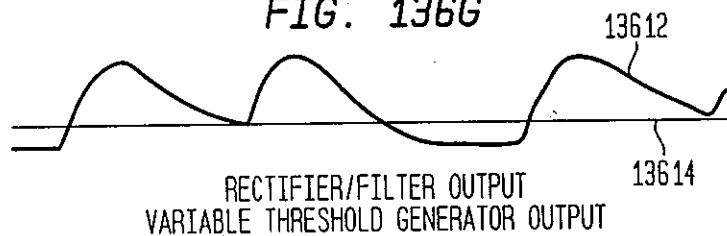


FIG. 136F

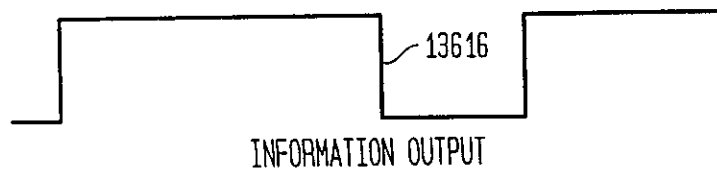


FIG. 137

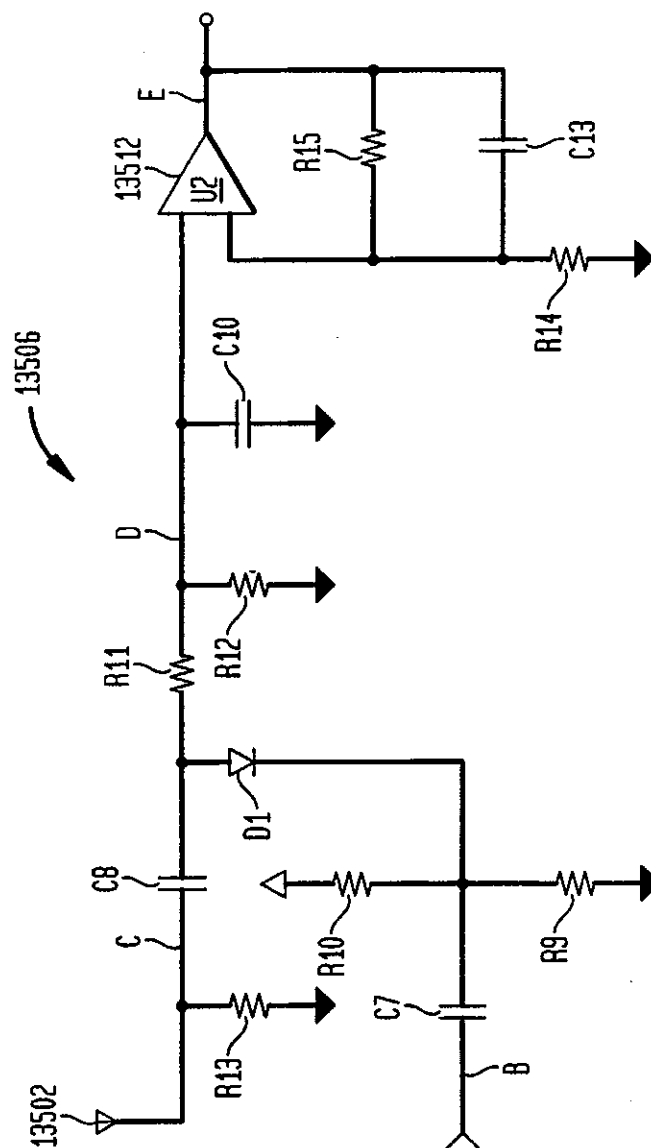


FIG. 138

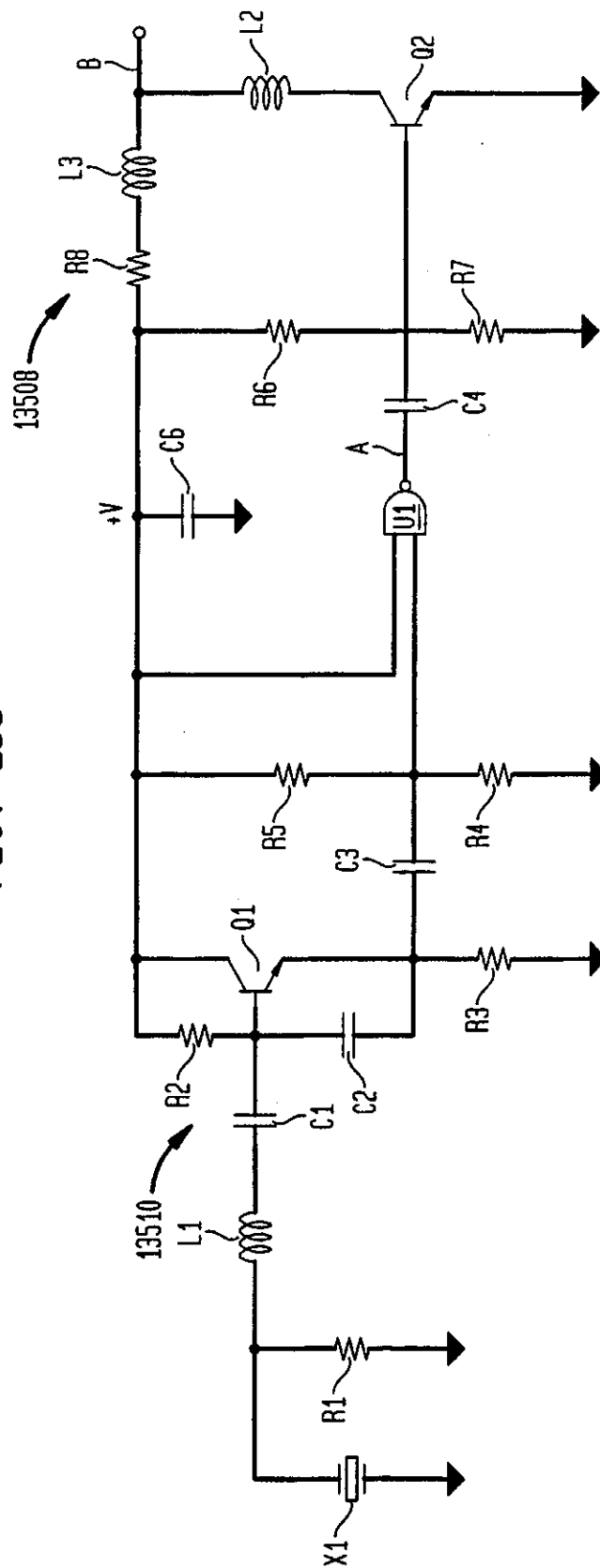
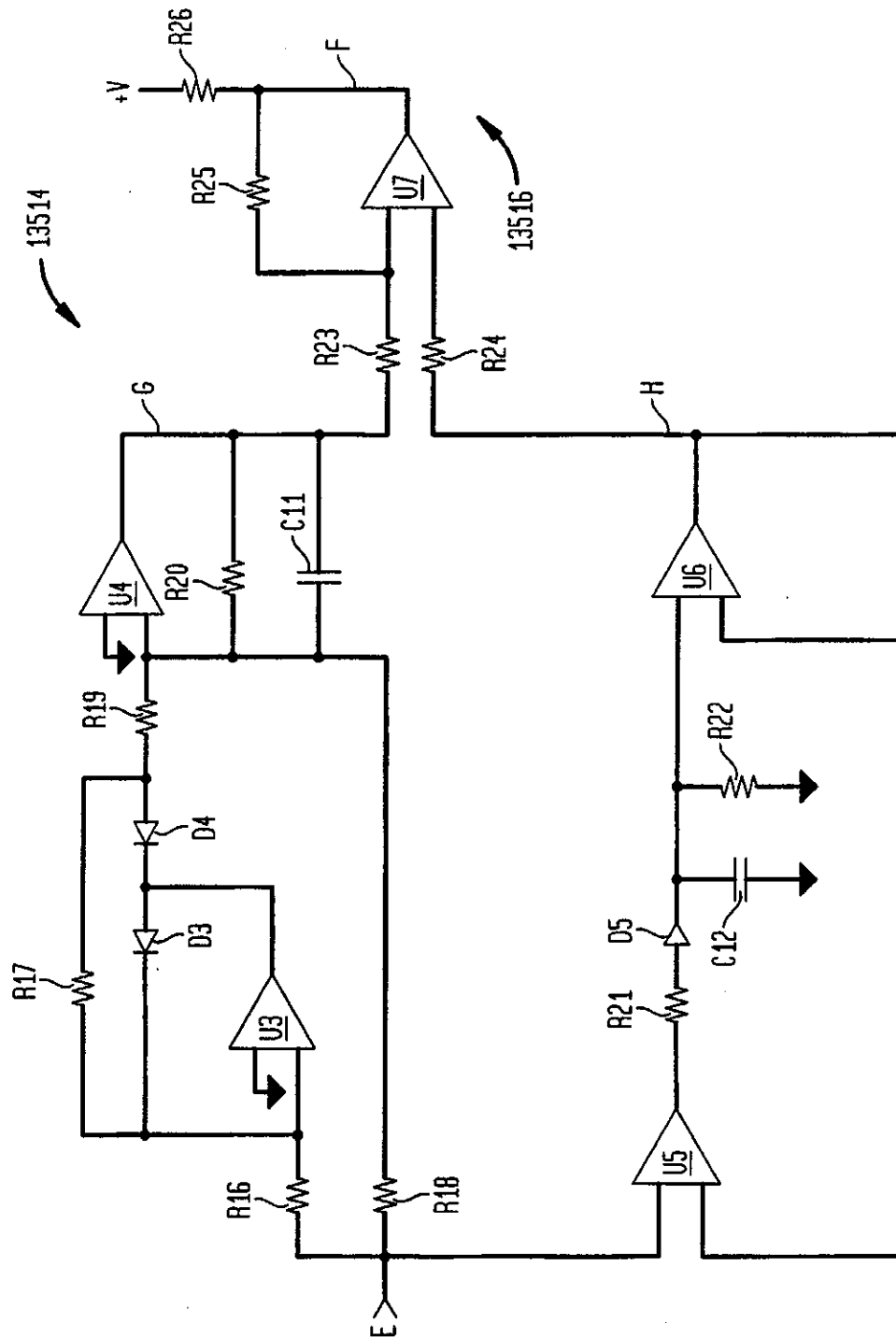
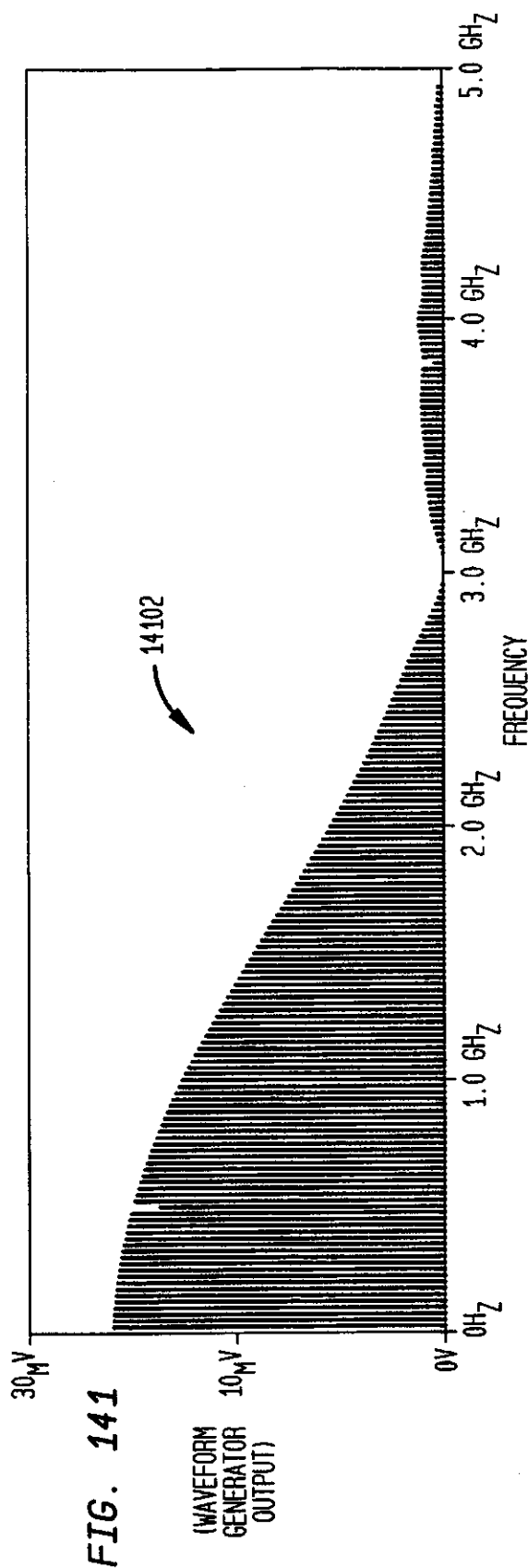
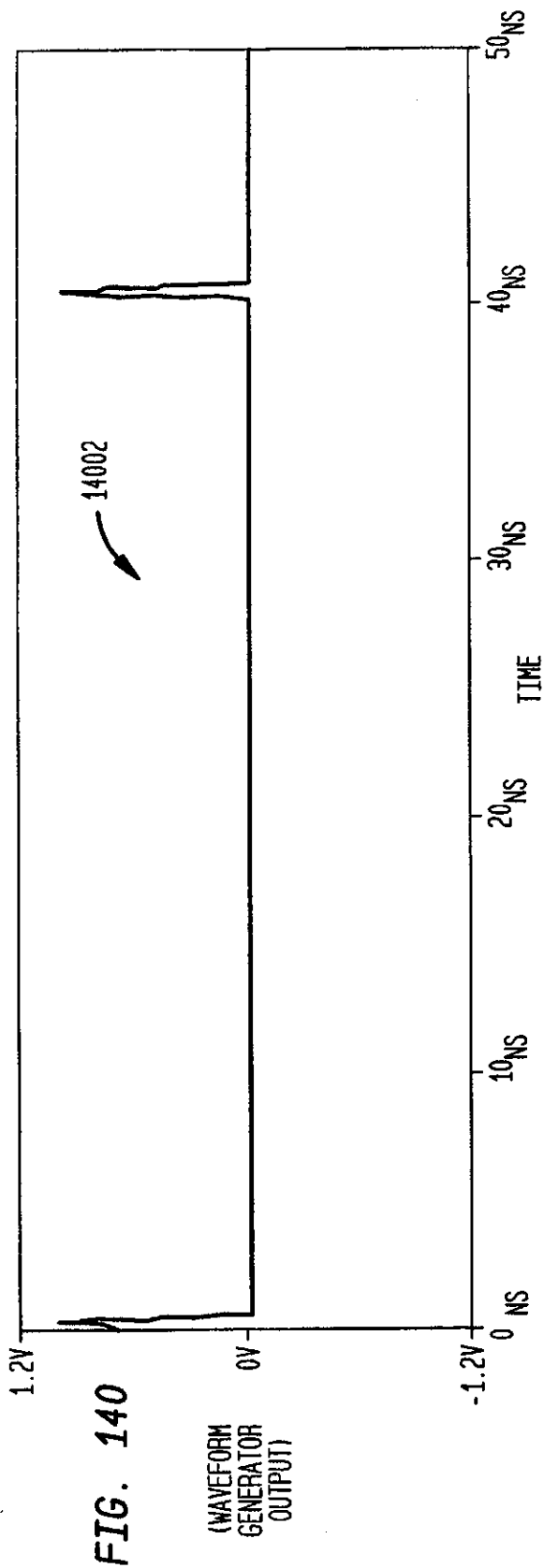


FIG. 139





177/283

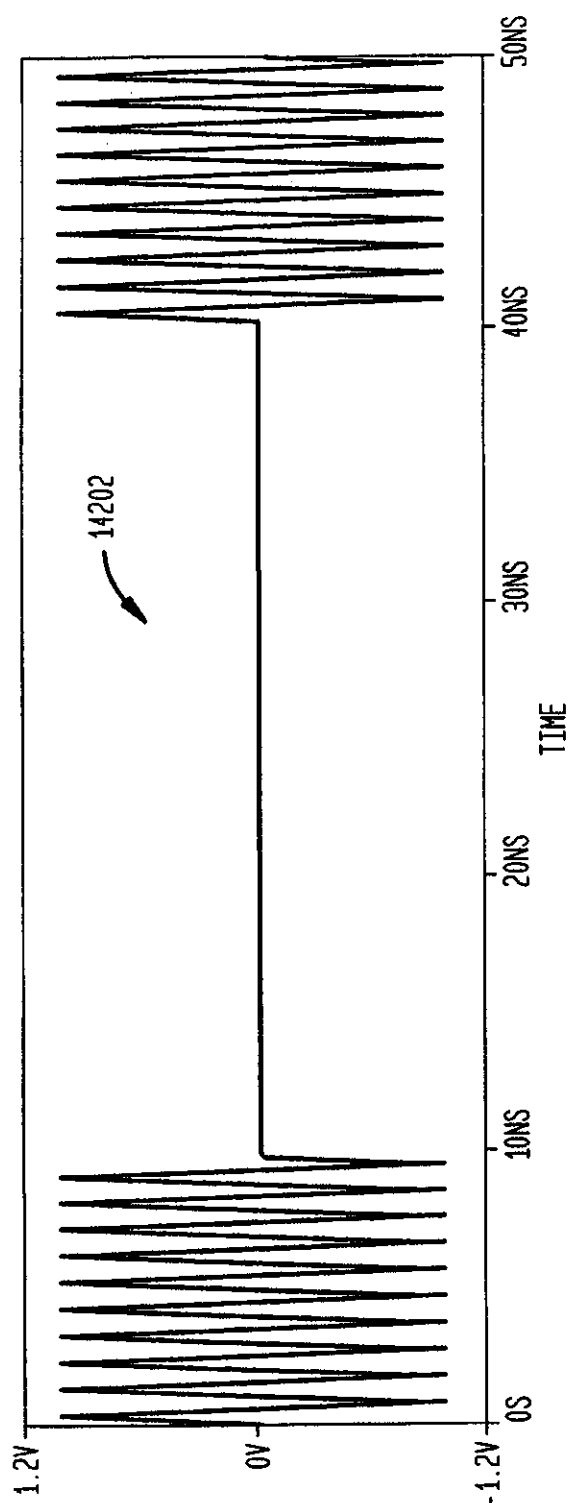


FIG. 142

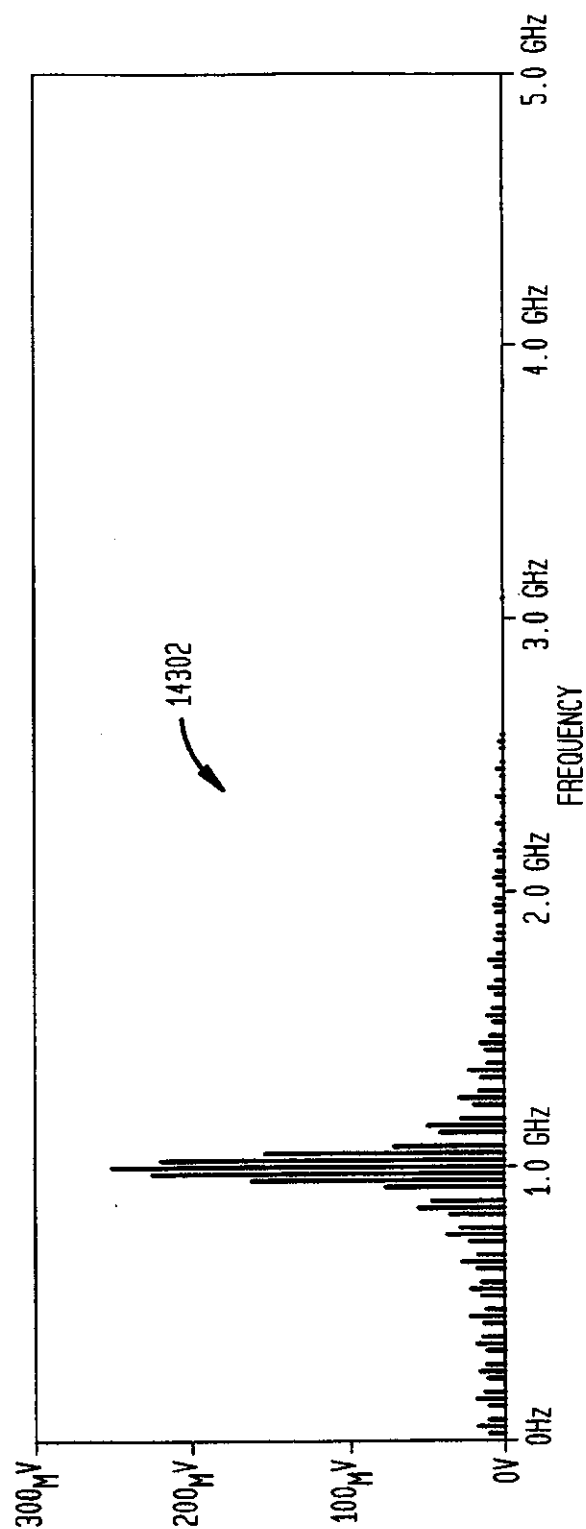
(WAVEFORM
GENERATOR
OUTPUT)

FIG. 143

(WAVEFORM
GENERATOR
OUTPUT)

FIG. 144

RF DIFFERENTIAL RECEIVER

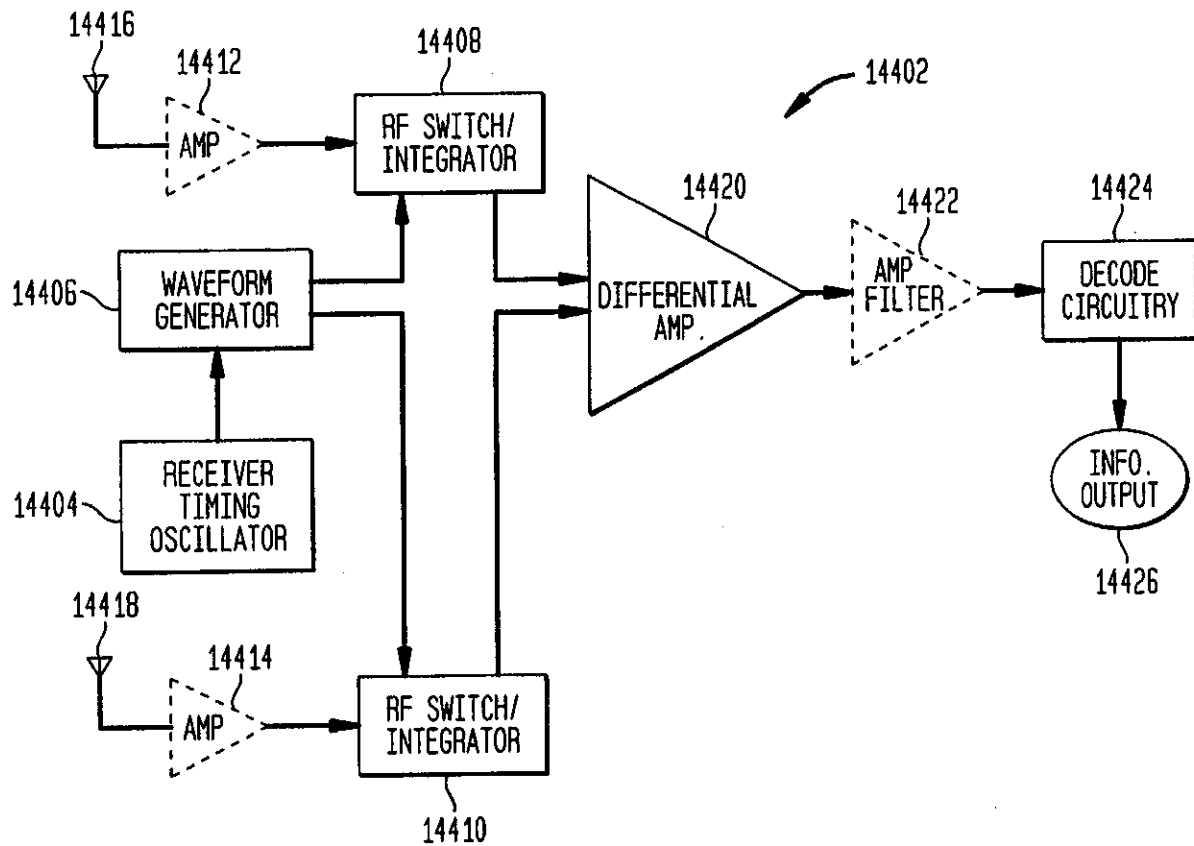
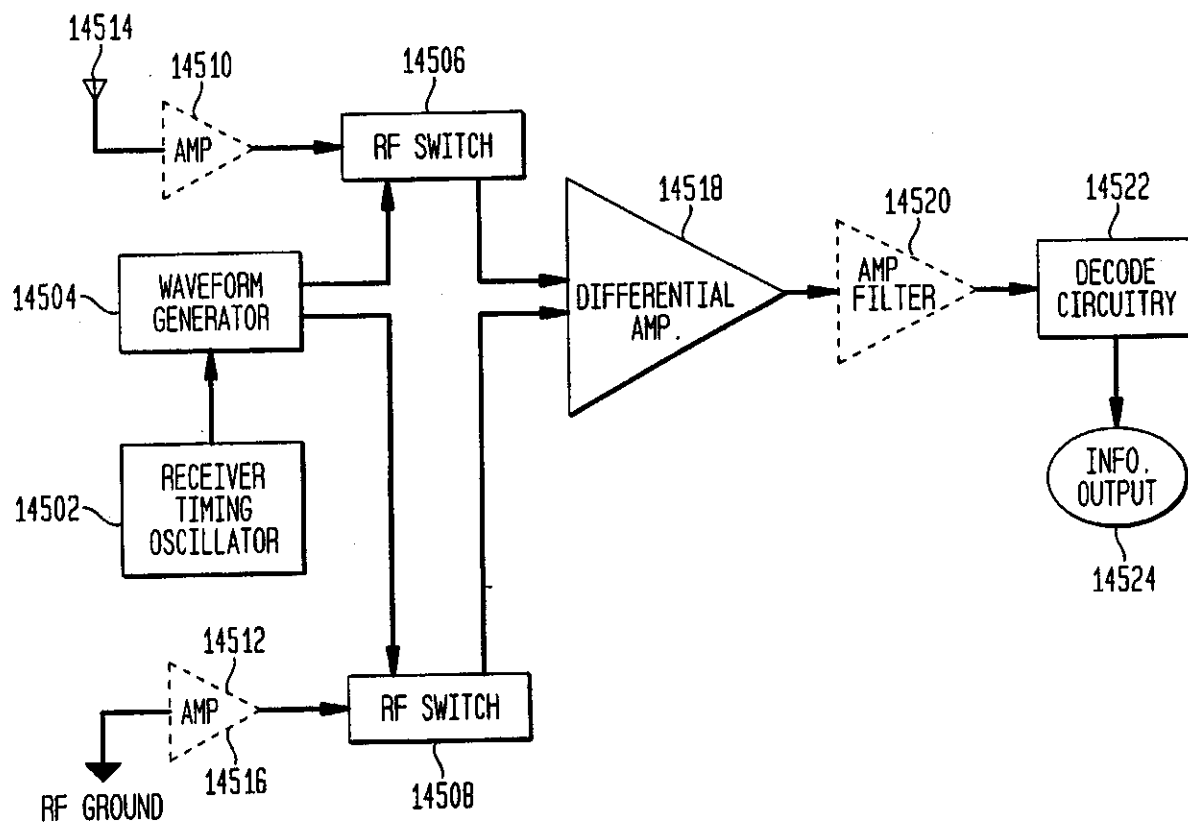


FIG. 145

PSEUDO DIFFERENTIAL RECEIVER



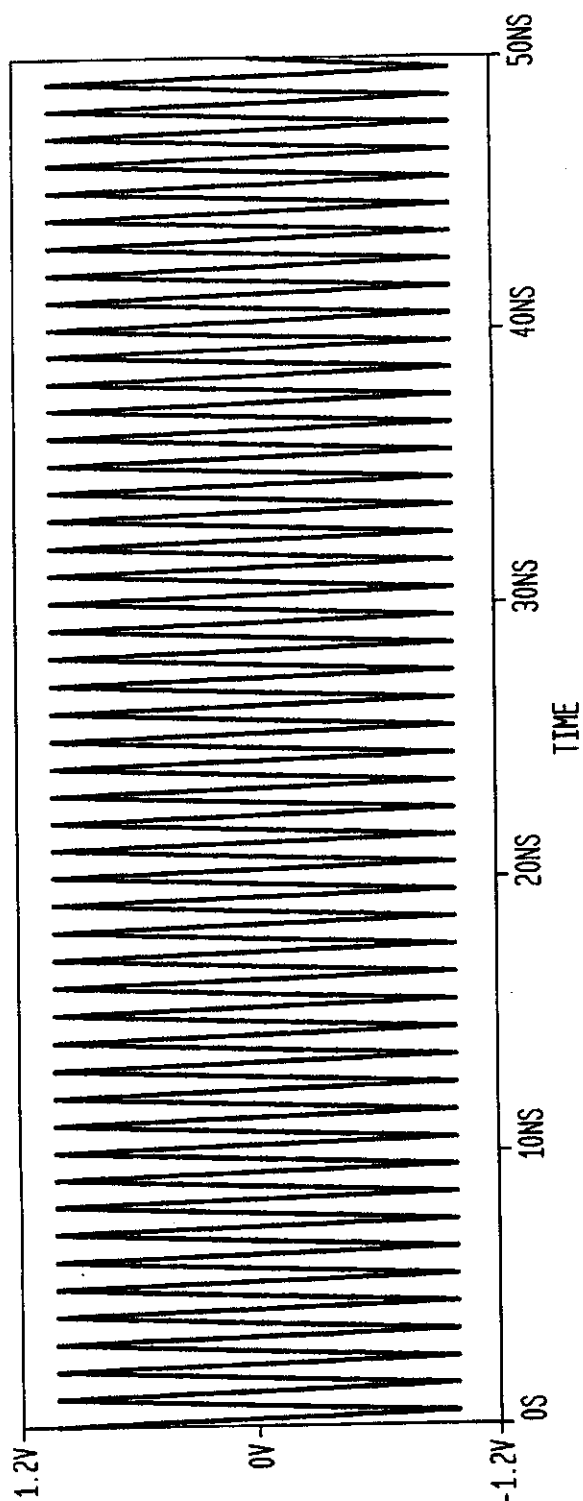


FIG. 146

(WAVEFORM
GENERATOR
OUTPUT)

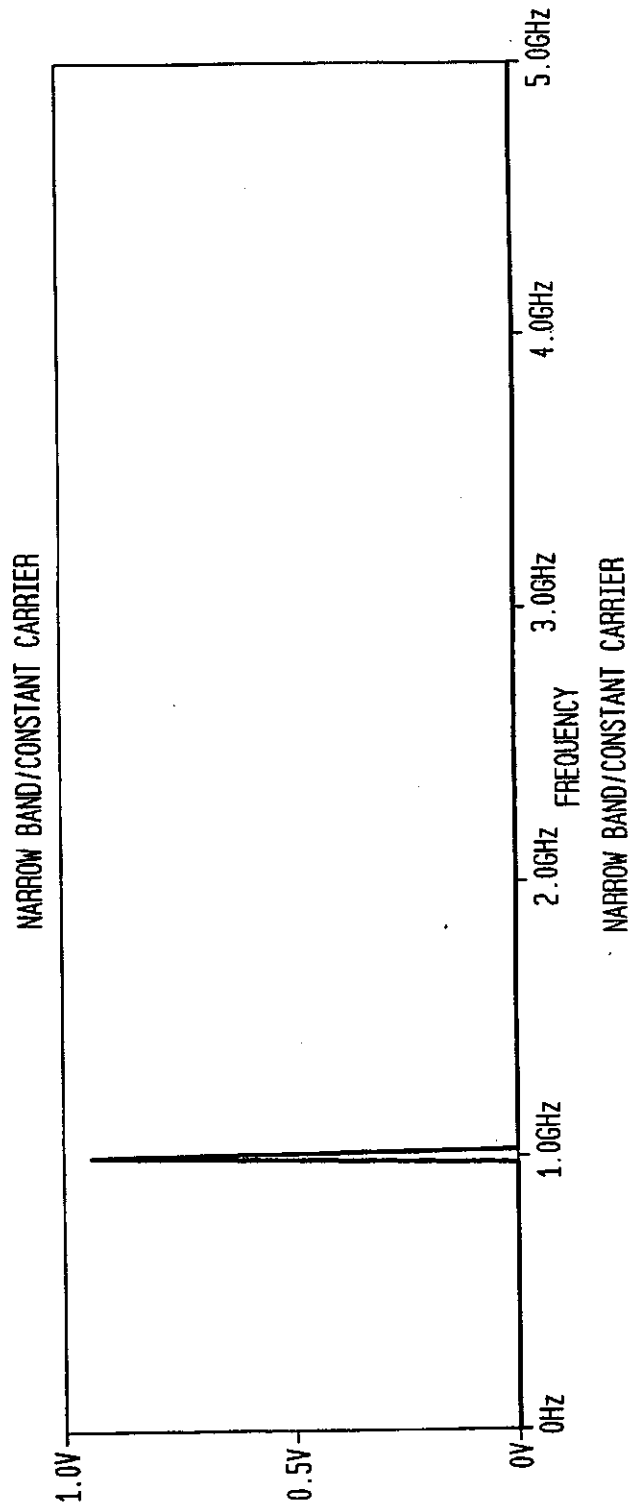


FIG. 147

(WAVEFORM
GENERATOR
OUTPUT)

FIG. 148

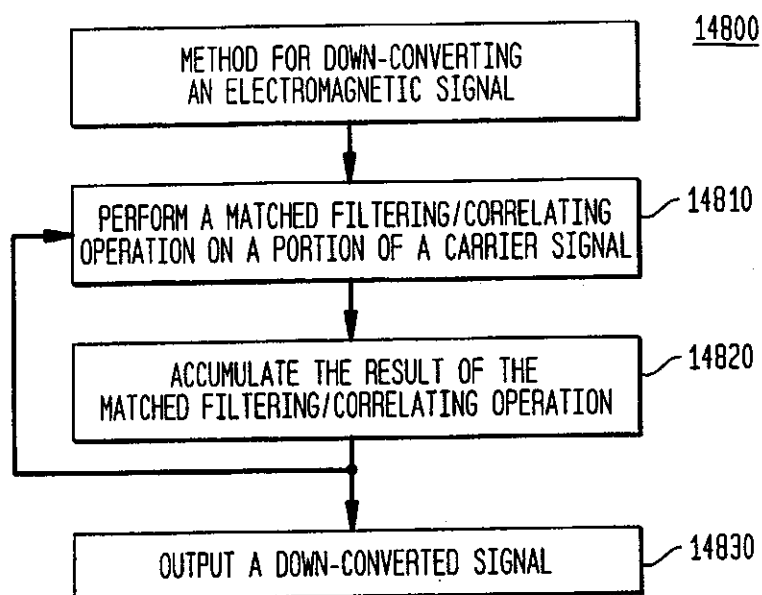
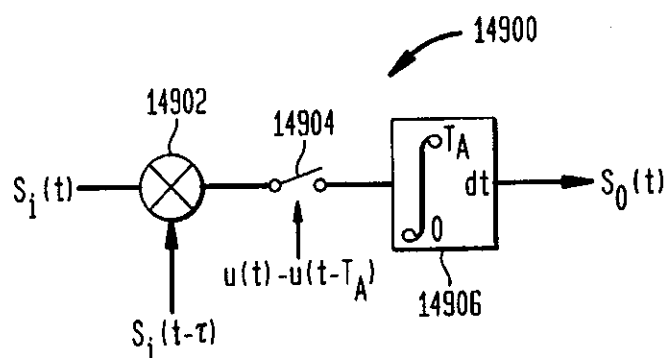


FIG. 149



182/283

FIG. 150

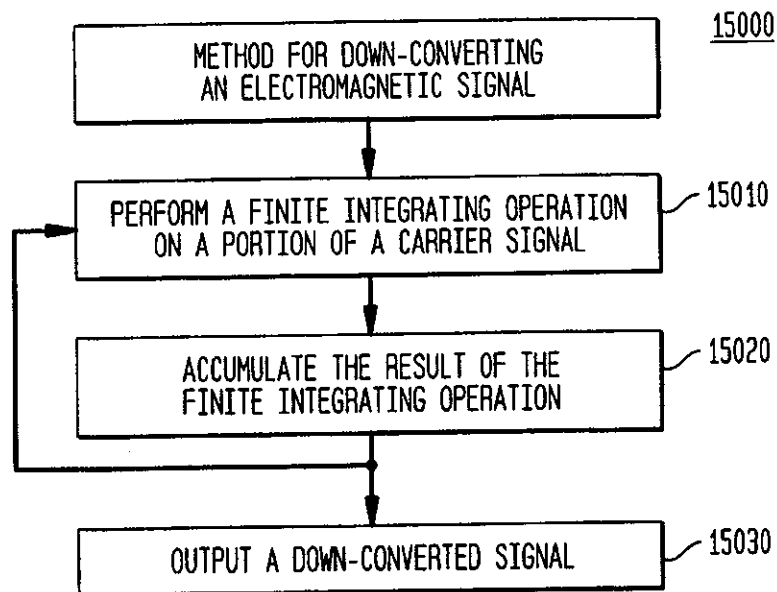


FIG. 151

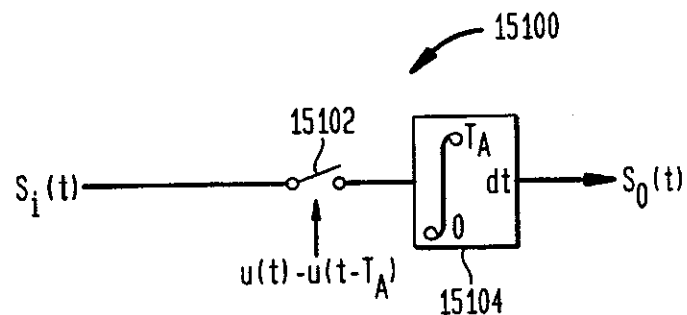


FIG. 152

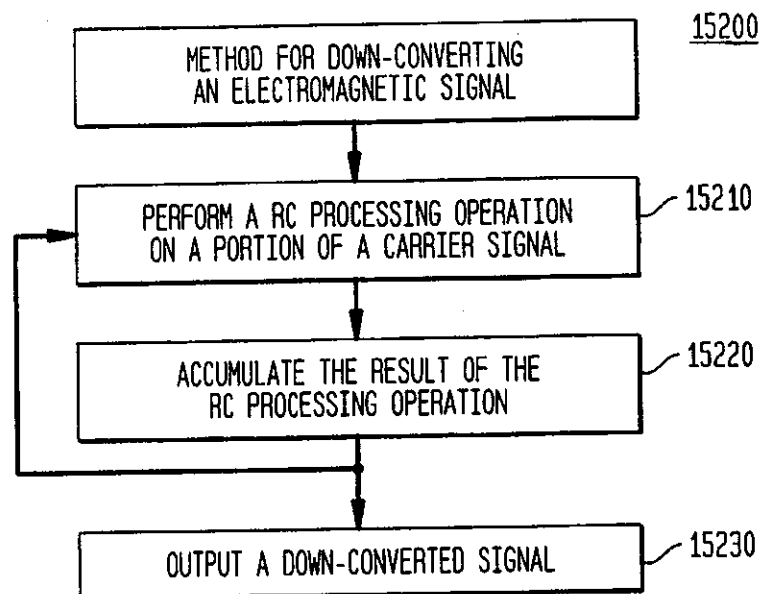
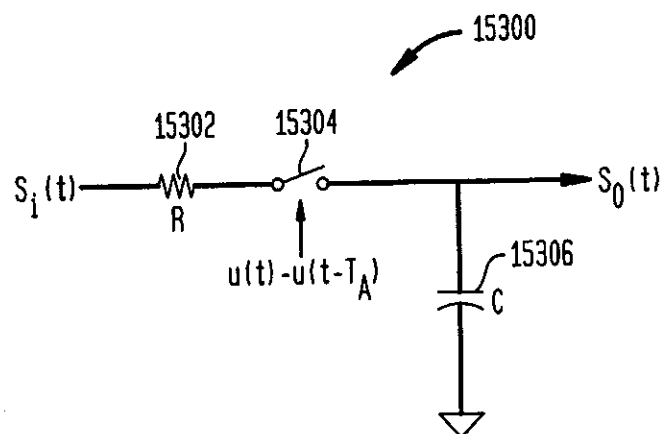


FIG. 153



184/283

FIG. 154

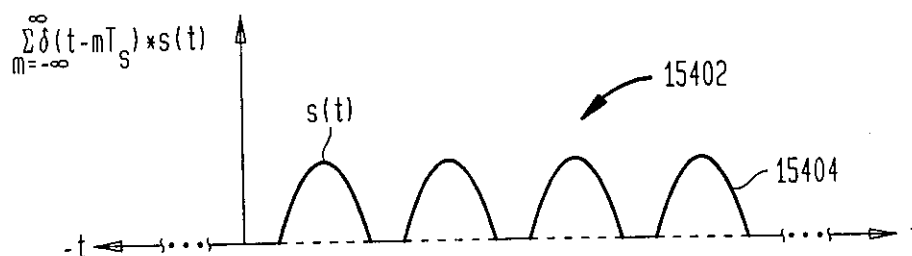


FIG. 155

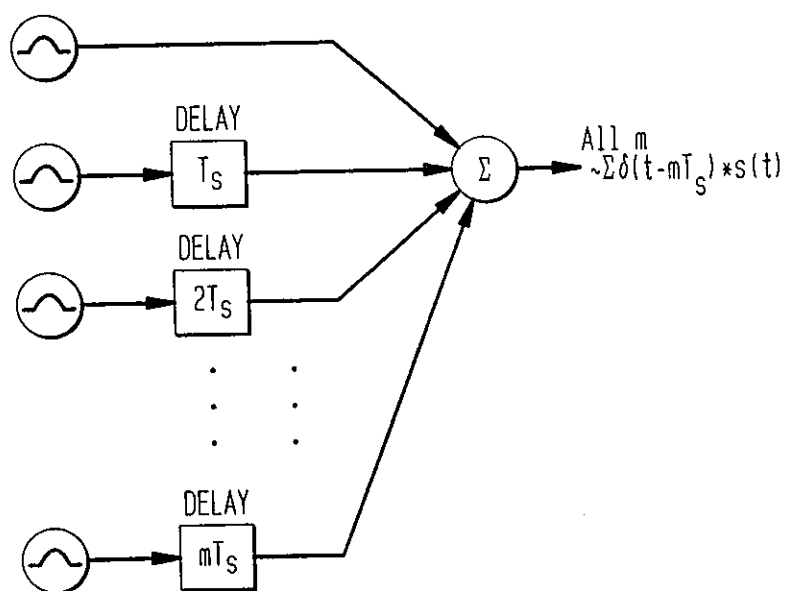


FIG. 156

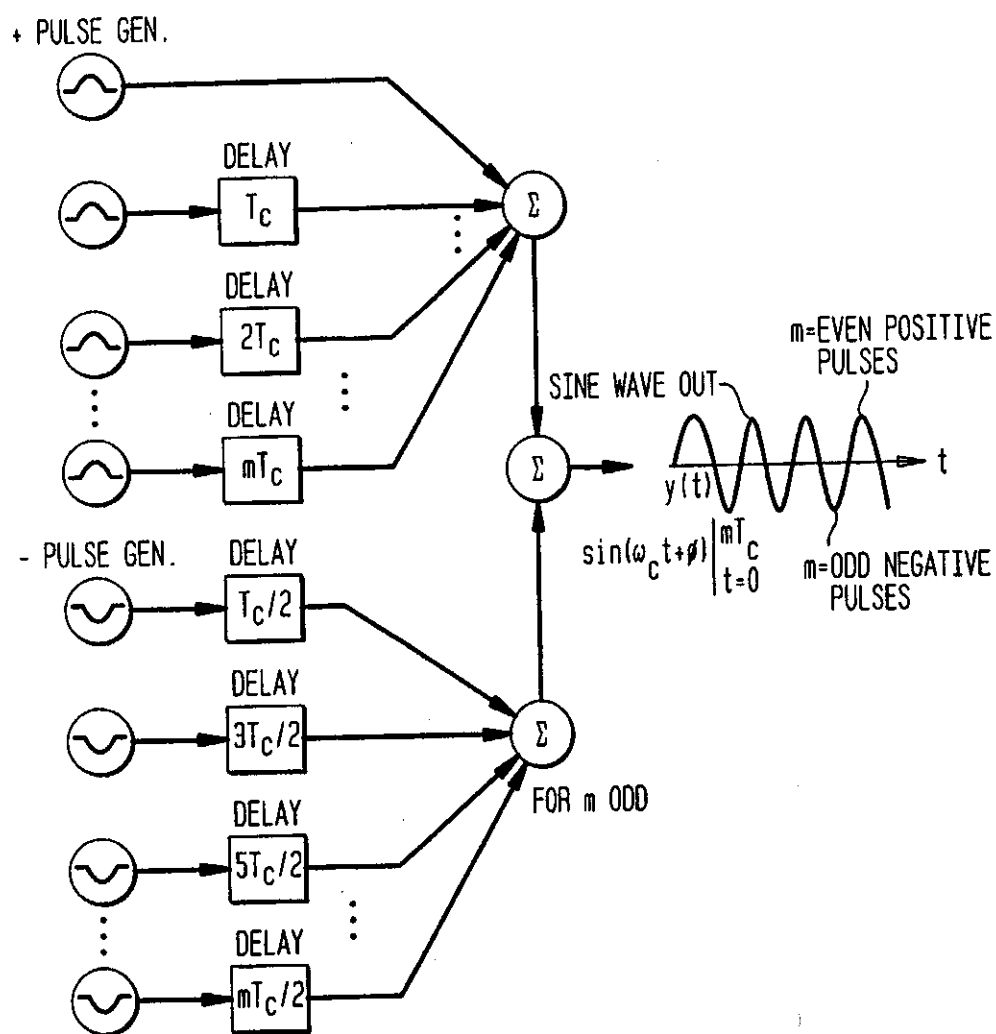
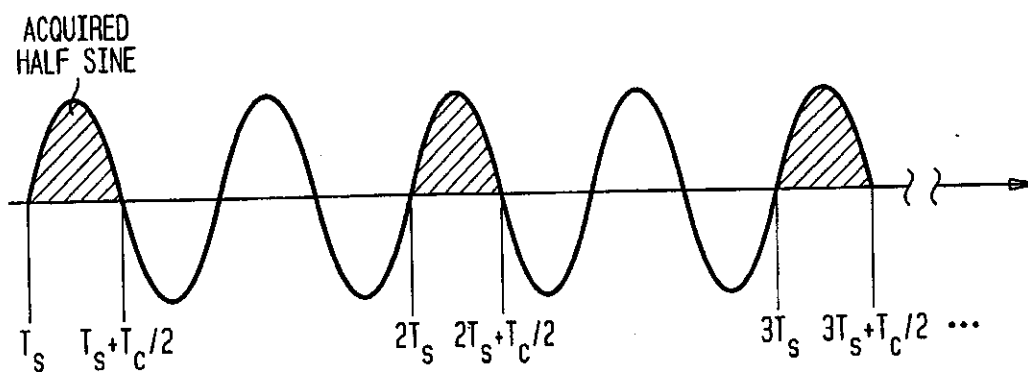


FIG. 157



CARRIER PROCESSED BY 3RD HARMONIC UFT PROCESSOR

FIG. 158

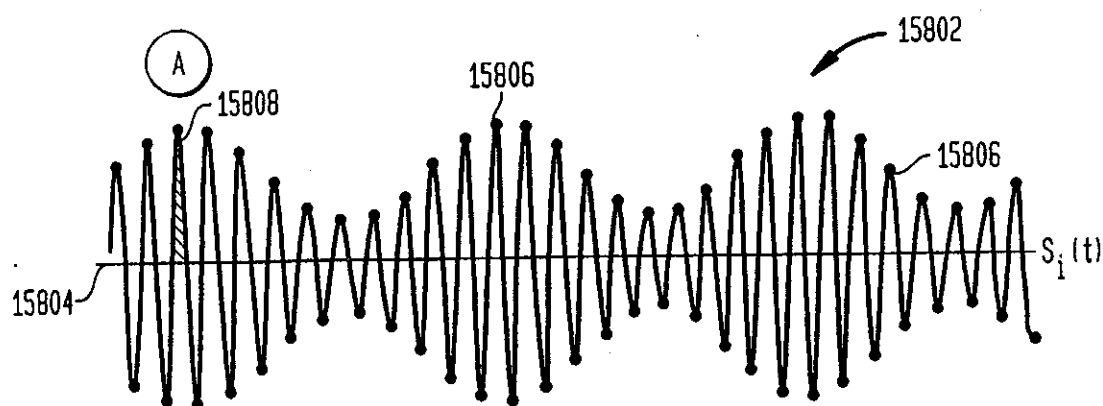


FIG. 159

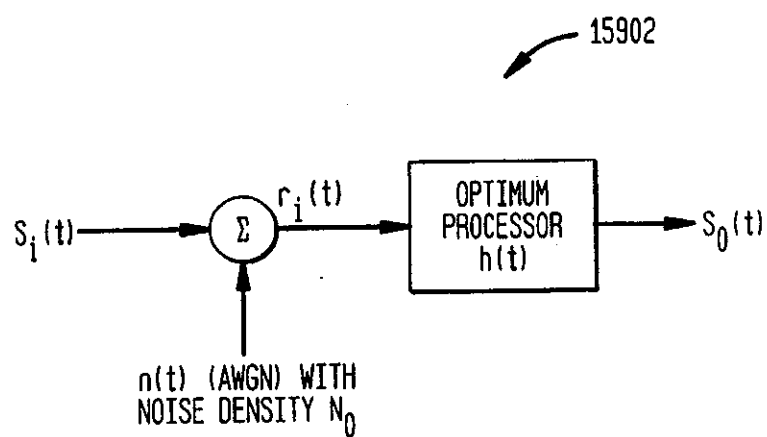


FIG. 160

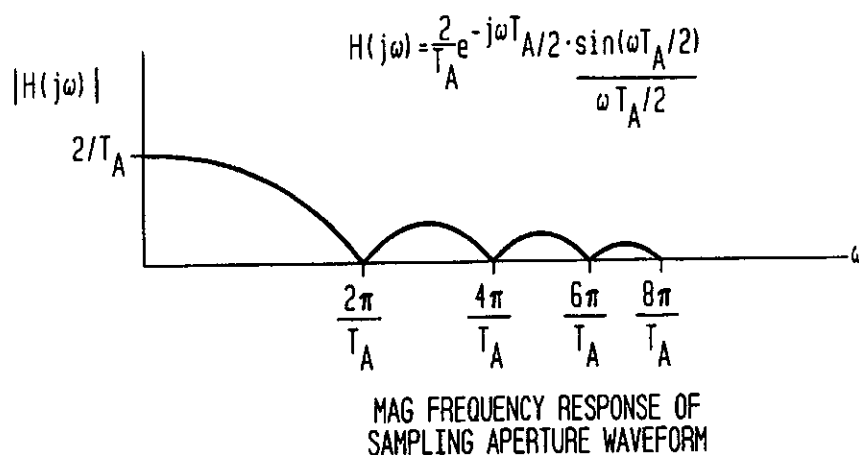


FIG. 161

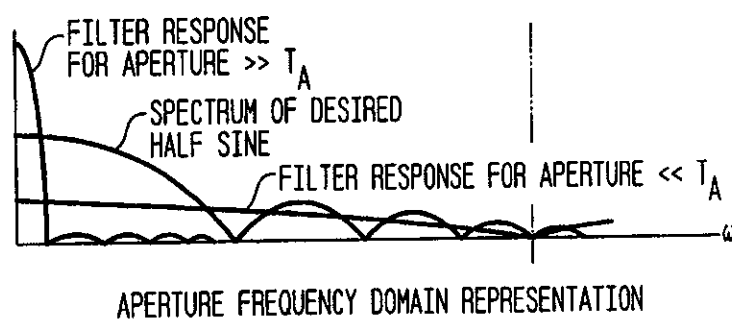


FIG. 162

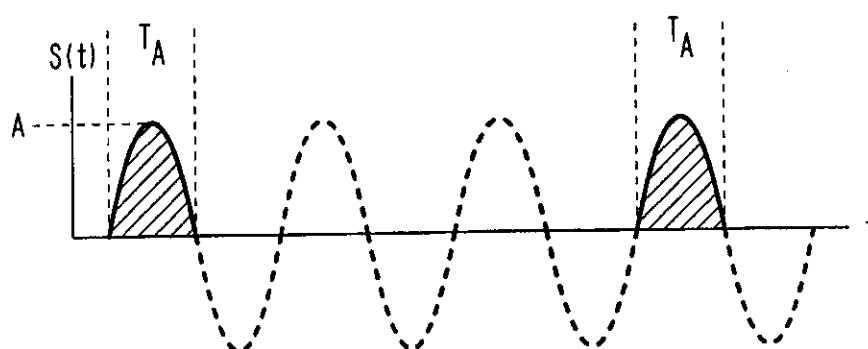
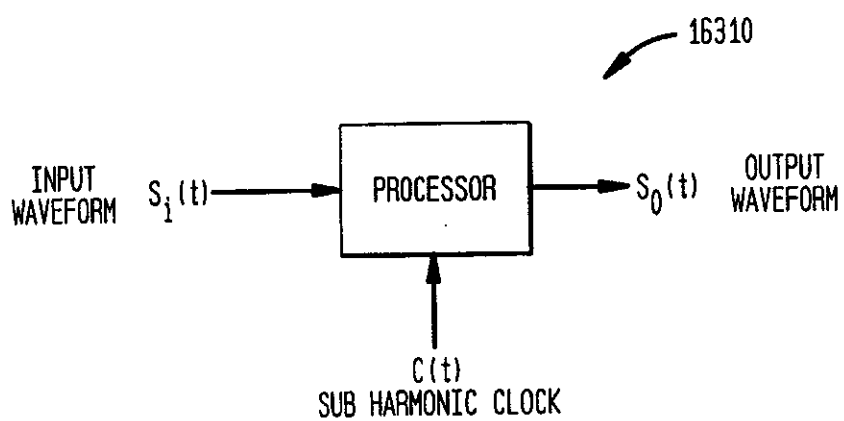


FIG. 163



189/283

FIG. 164A

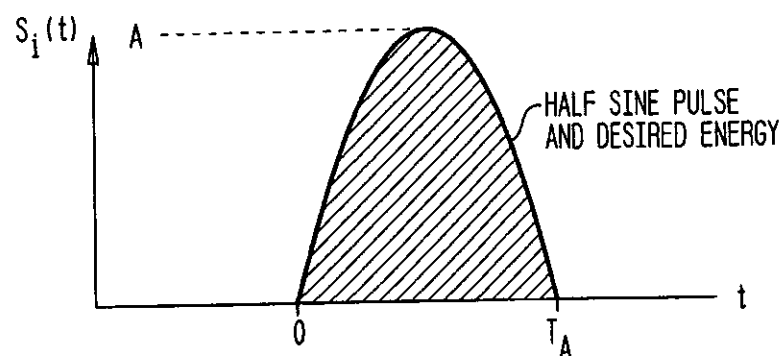


FIG. 164B

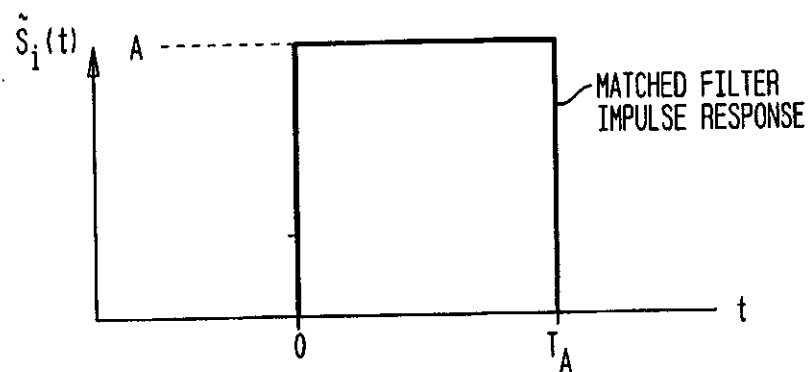
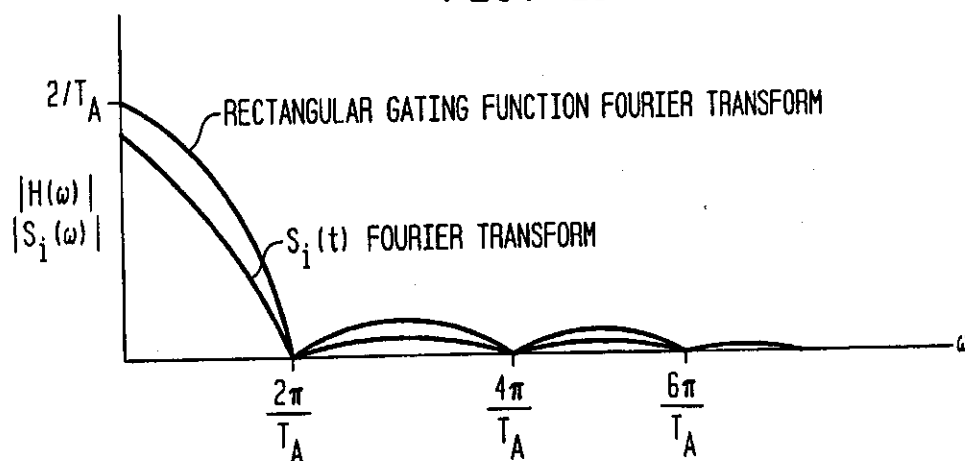


FIG. 164C



190/283

FIG. 165

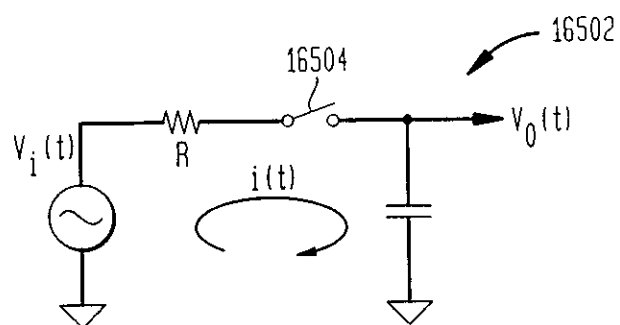


FIG. 166

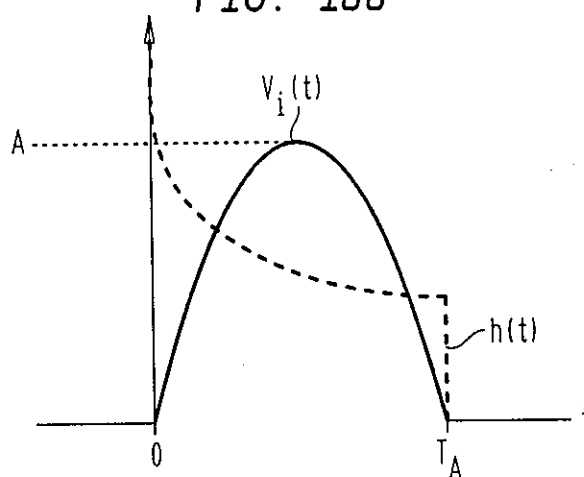
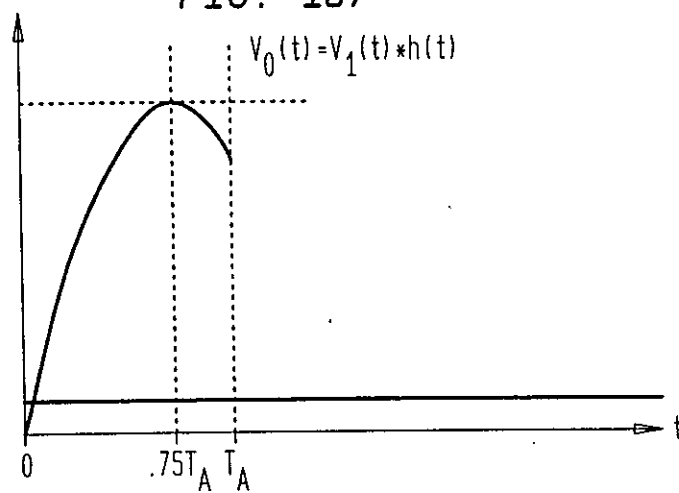


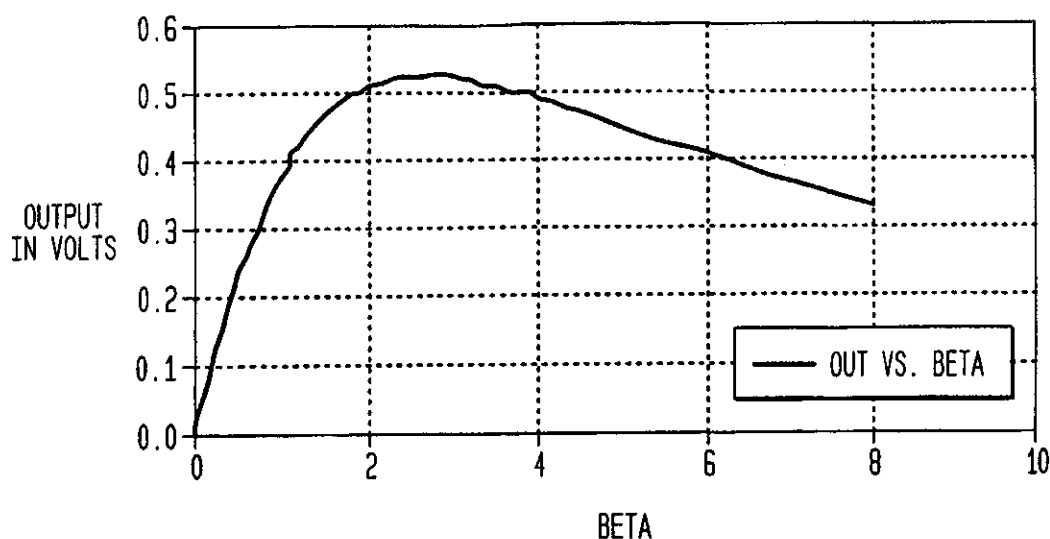
FIG. 167



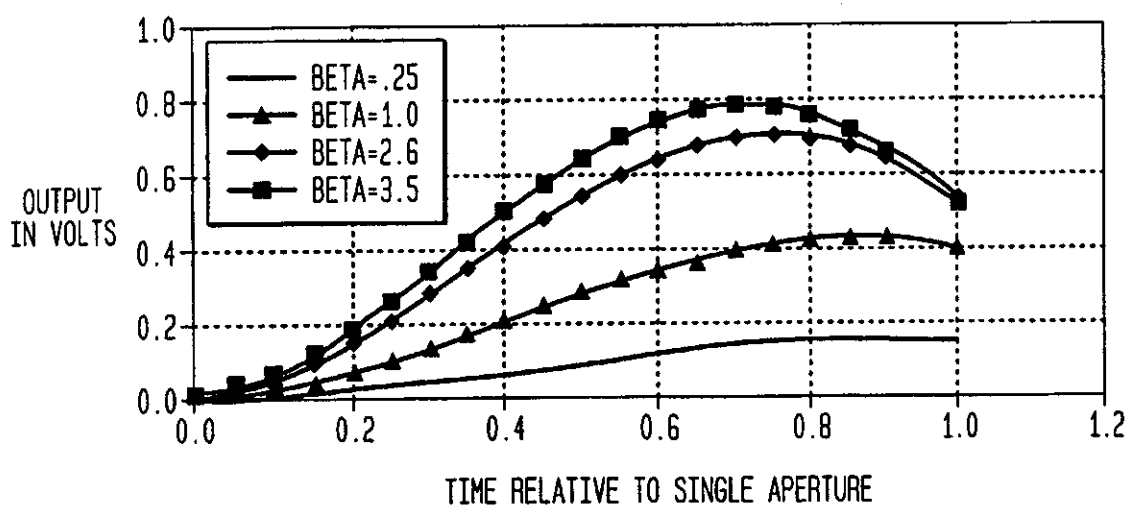
191/283

FIG. 168

UFT OUTPUT VS. BETA FOR SIMPLE RC IMPLEMENTATION

**FIG. 169**

UFT OUTPUT RESPONSE VS. NORMALIZED TIME WITH BETA AS A PARAMETER



192/283

FIG. 170

NORMALIZED SNR FOR MF, INT., RC UFT
IMPLEMENTATIONS, No.=1, $T_a=A$, $A=1$

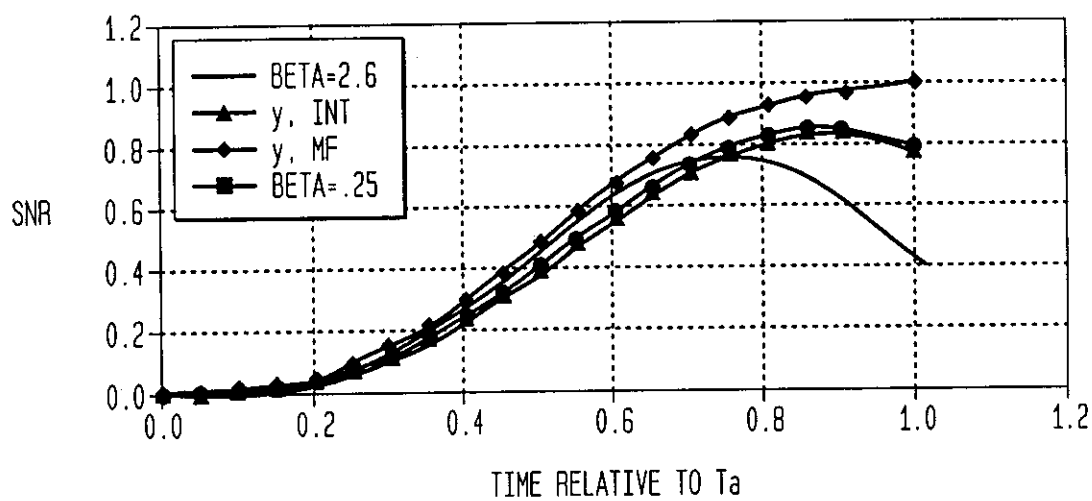
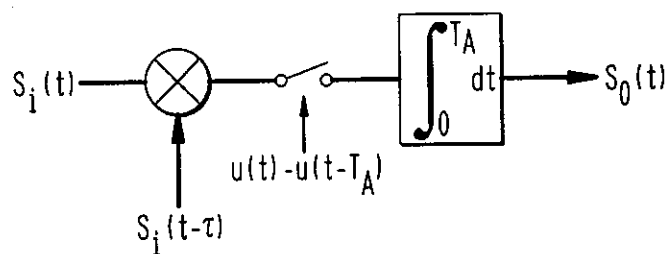


FIG. 171



193/283

FIG. 172

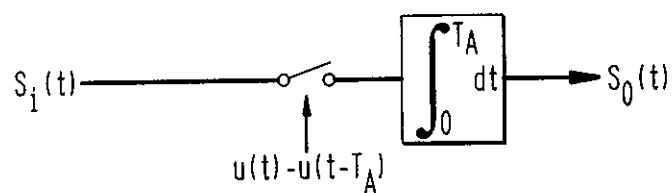


FIG. 173

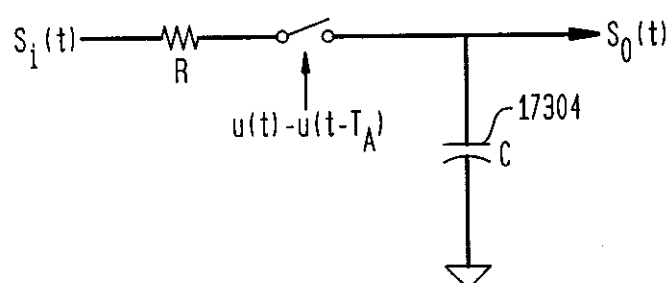


FIG. 174
UFT OUTPUT CHARGE TRANSFER

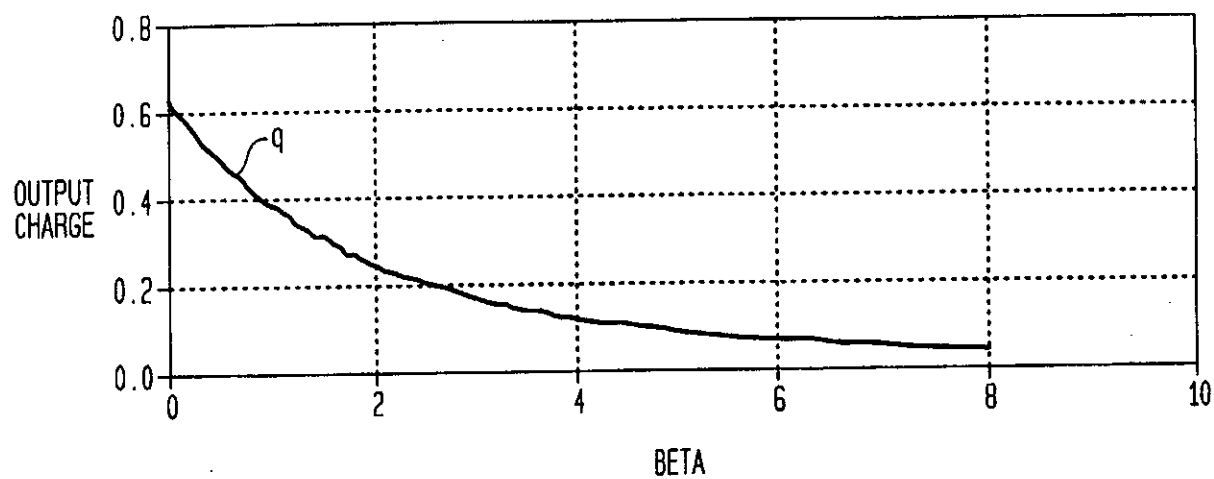


FIG. 175A

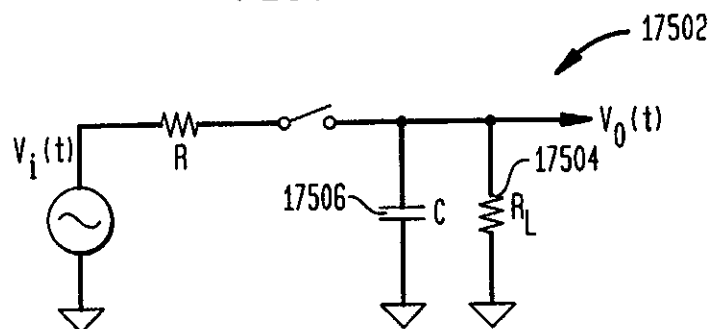


FIG. 175B

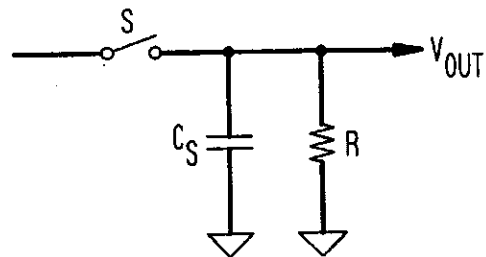


FIG. 175C

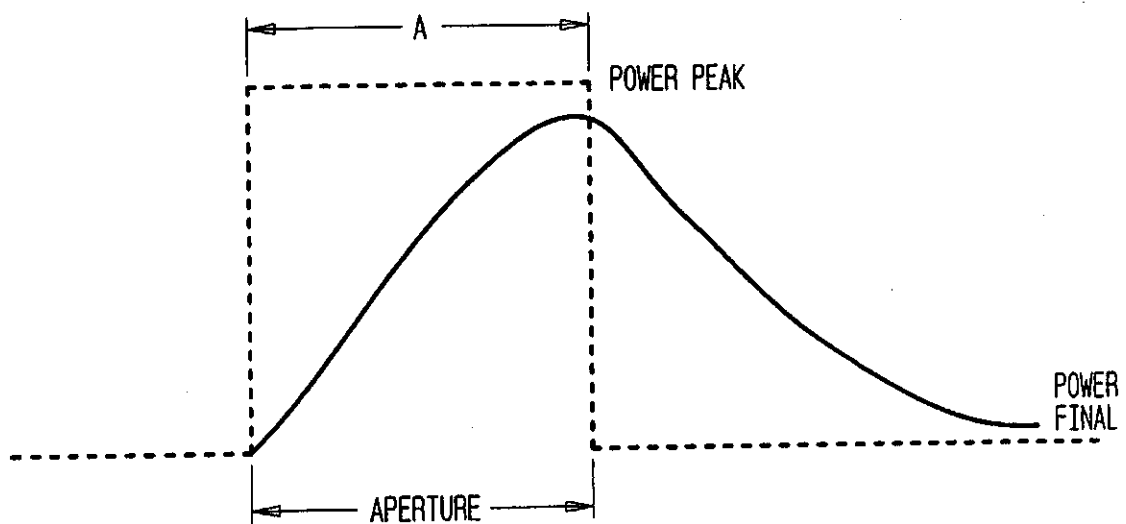
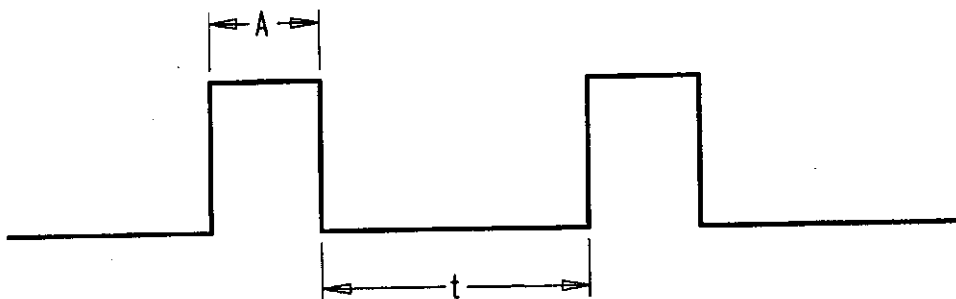


FIG. 175D



196/283

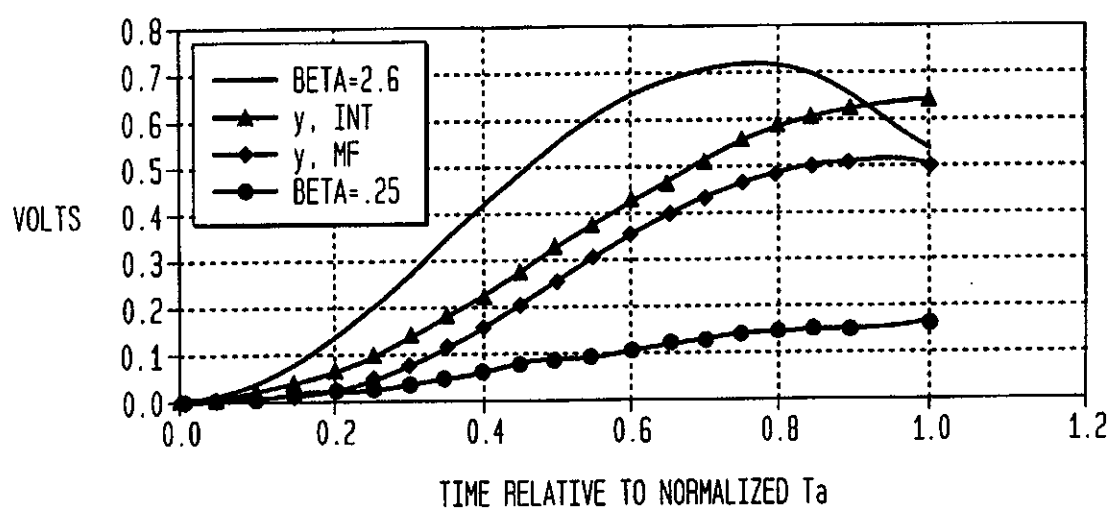
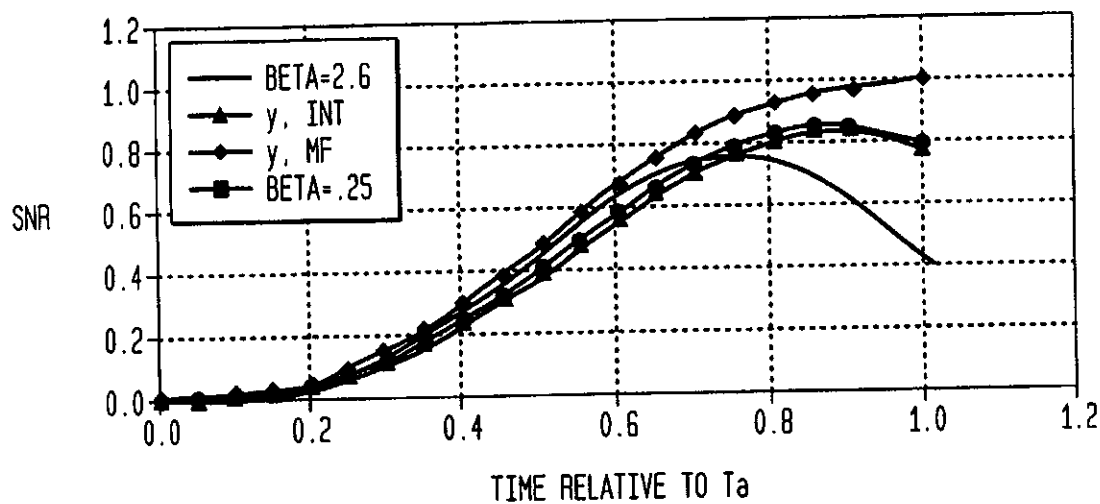
FIG. 176OUTPUT VOLTAGE FOR 3 UFT PROCESSORS;
MATCHED FILTER, INTEGRATOR, RC

FIG. 177A

NORMALIZED SNR FOR MF, INT., RC UFT
IMPLEMENTATIONS, No.=1, $T_a=1$, $A=1$ 

198/283

FIG. 177B

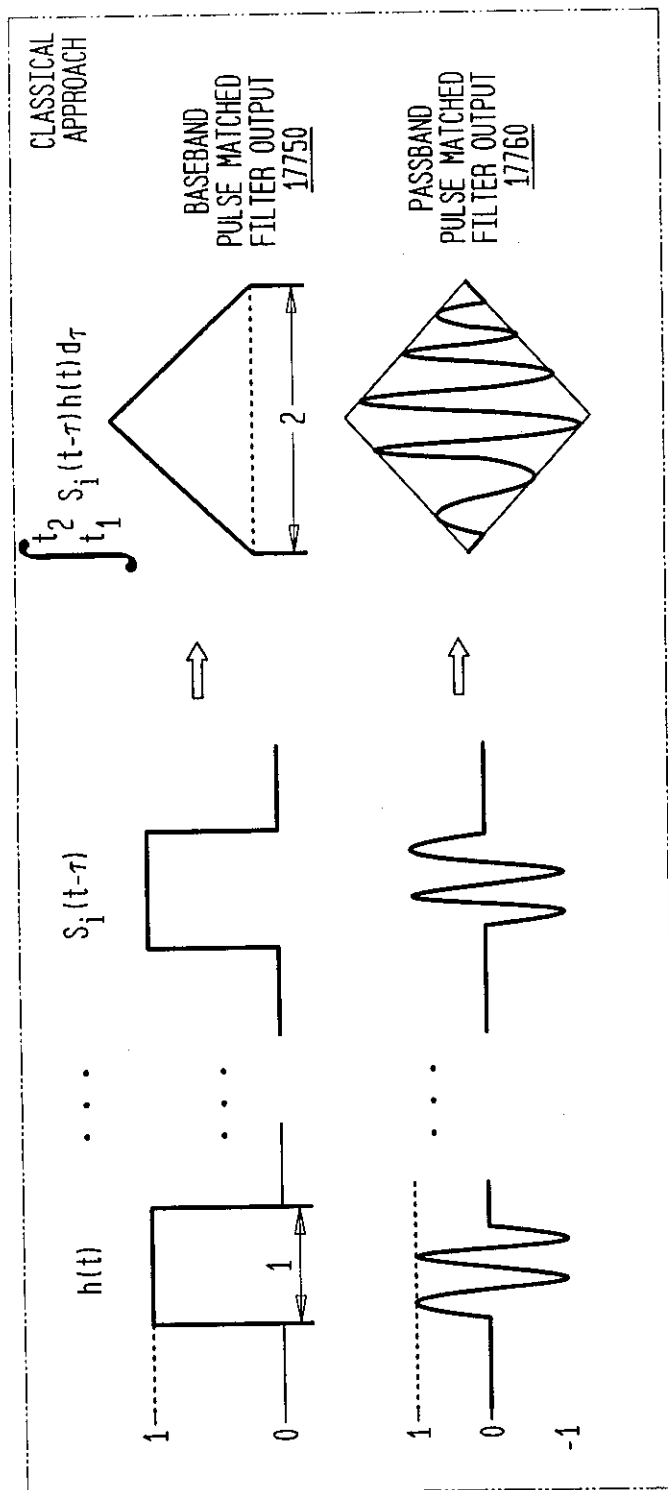


FIG. 177C

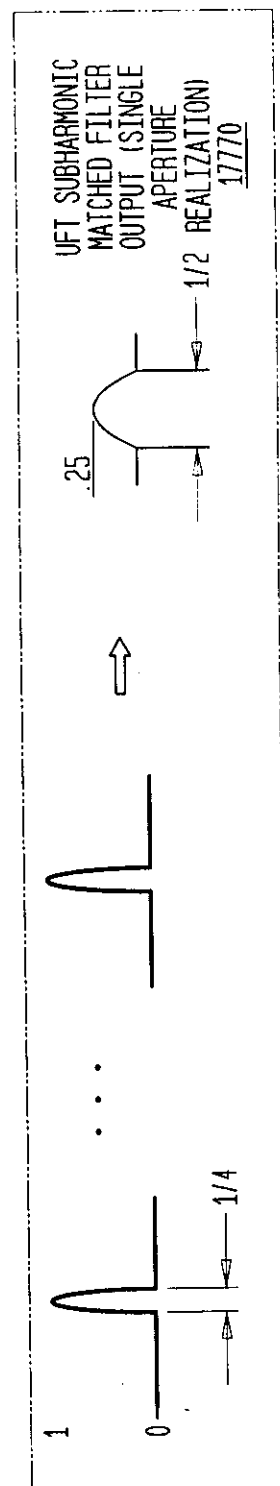


FIG. 177D

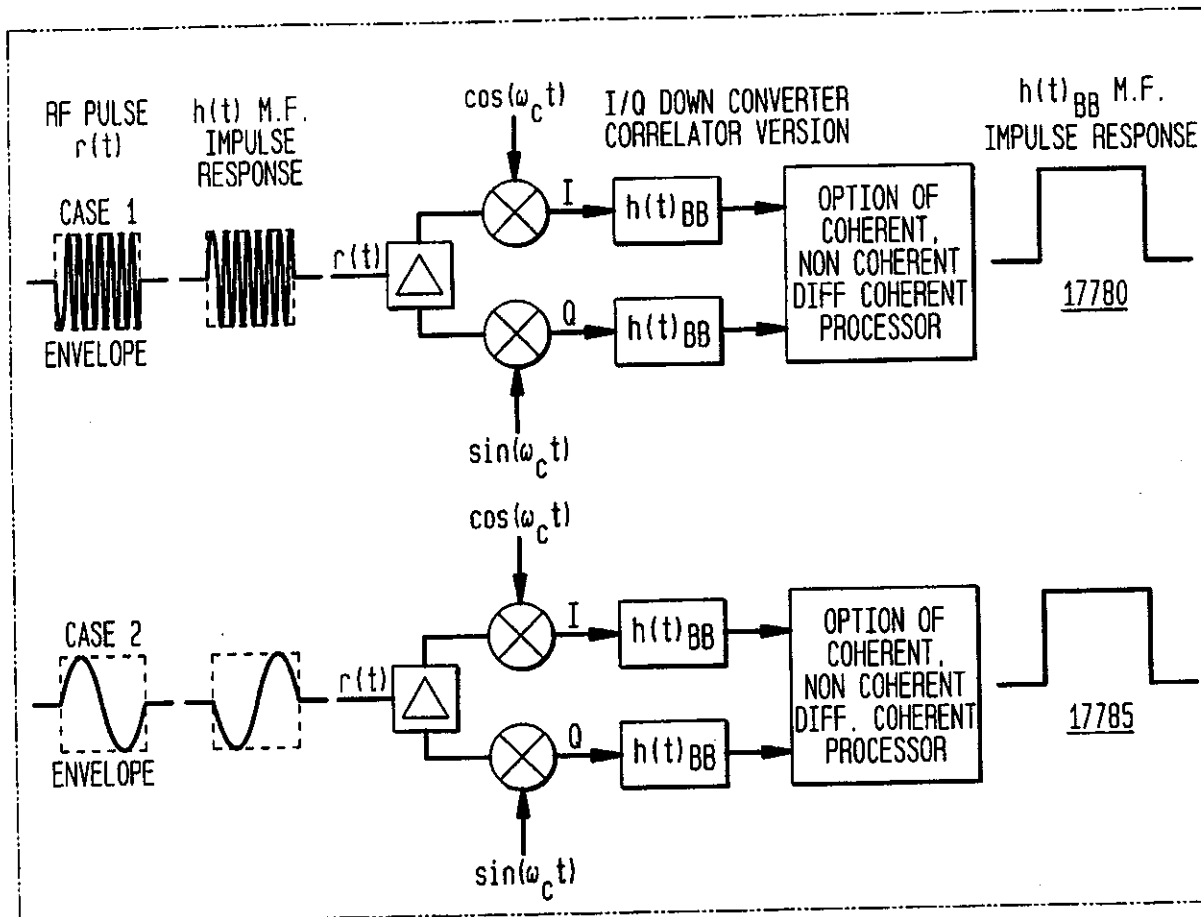
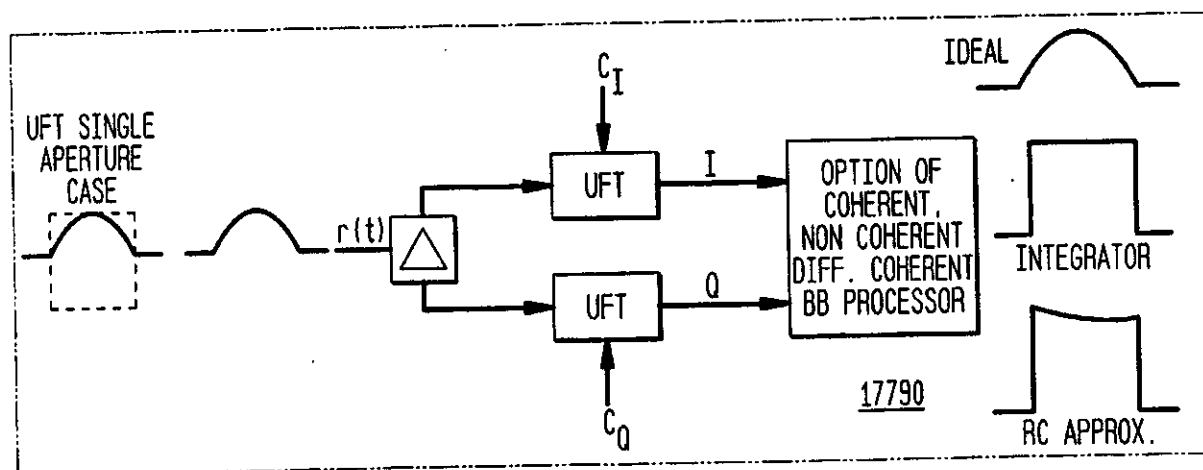
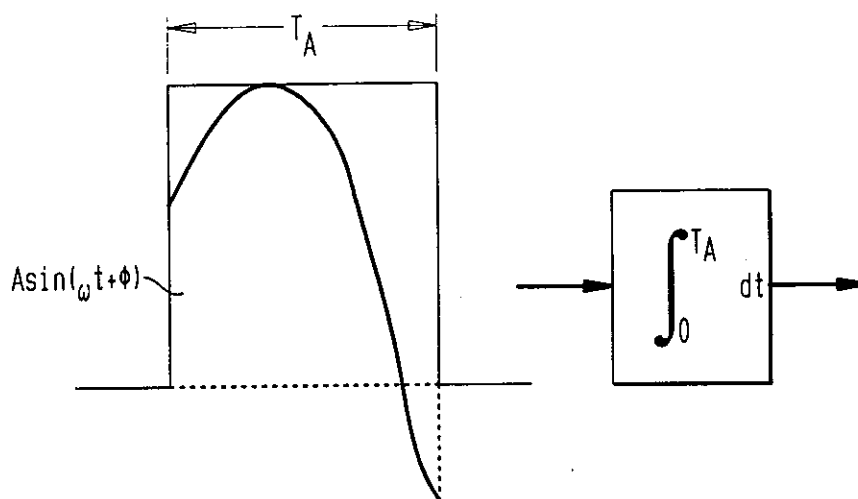


FIG. 177E



200/283

FIG. 177F



$$\begin{aligned}
 \int_0^{T_A} A u(t-T_A) \sin(\omega t + \phi) dt &= \int_0^{T_A} A (u(t-T_A) \cos \phi \sin(\omega t) + u(t-T_A) \sin \phi \cos(\omega t)) dt \\
 &= A \cos(\phi) \underbrace{\int_0^{T_A} u(t-T_A) \sin(\omega t) dt}_{\text{UFT CORRELATOR KERNEL}} + A \sin(\phi) \underbrace{\int_0^{T_A} u(t-T_A) \cos(\omega t) dt}_{=0} \\
 &= A \cos(\phi) \int_0^{T_A} u(t-T_A) \sin(\omega t) dt
 \end{aligned}$$

- A IS CONSTANT ON A SINE TO SINE BASIS
- ϕ IS CONSTANT ON A SINE TO SINE BASIS
- i.e., THE MODULATION RATE DUE TO INFORMATION FOR PHASE AND AMPLITUDE IS VERY SLOW COMPARED TO CARRIER FREQUENCY

FIG. 178A

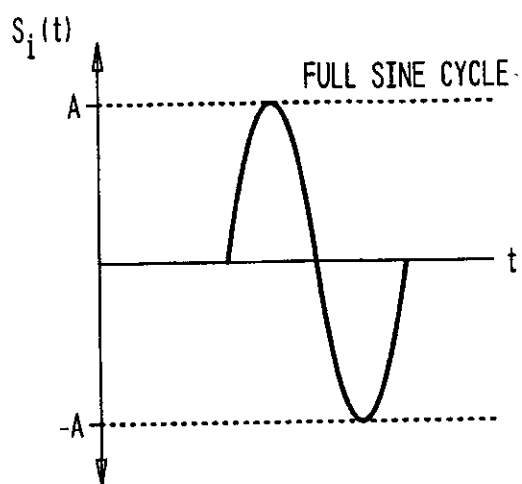
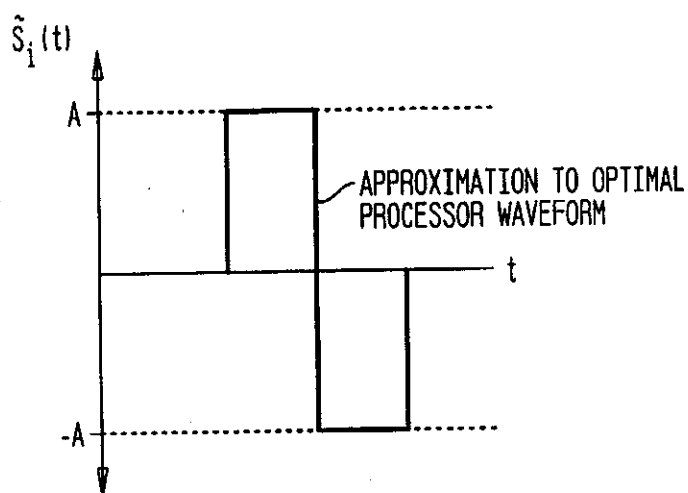


FIG. 178B



202/283

FIG. 179

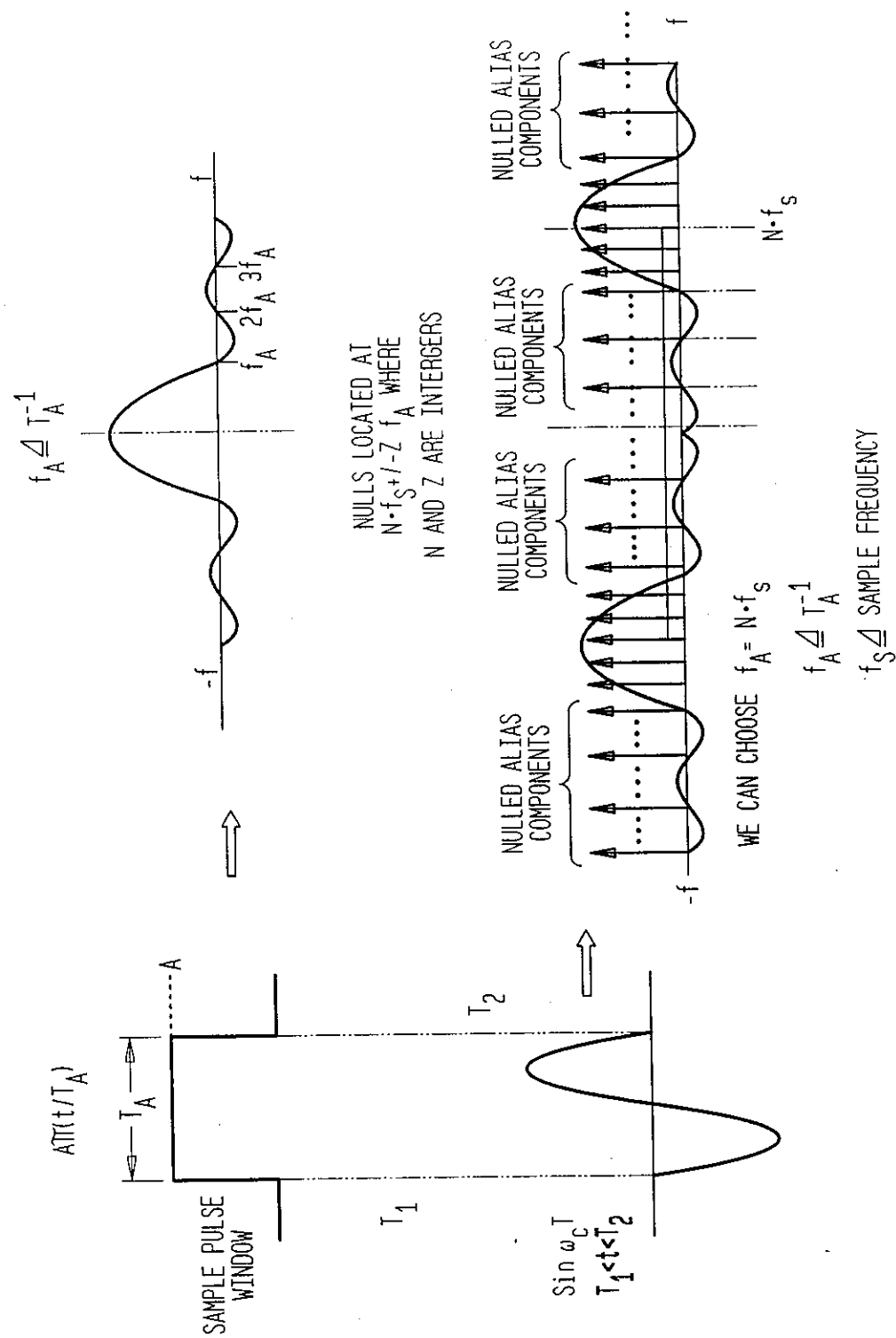
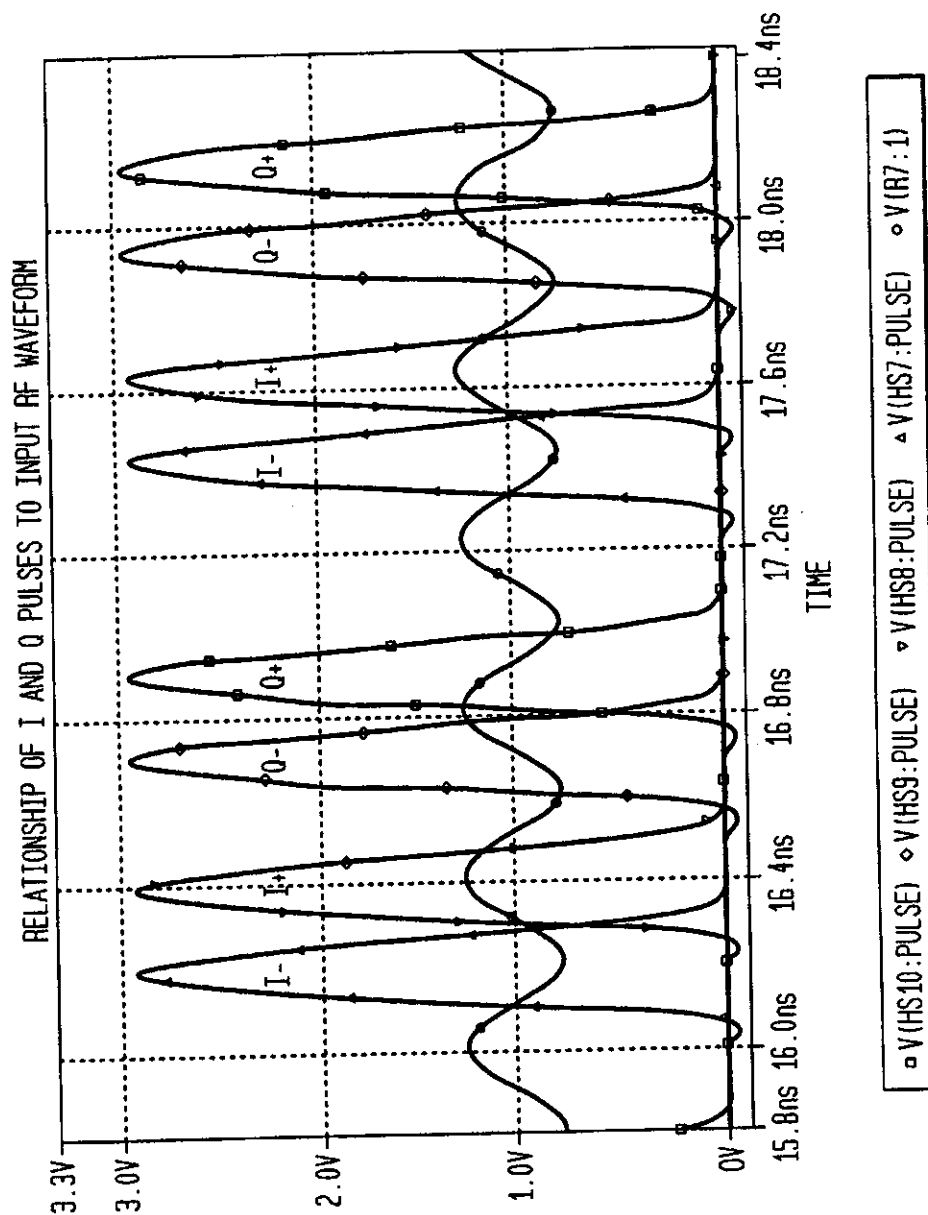
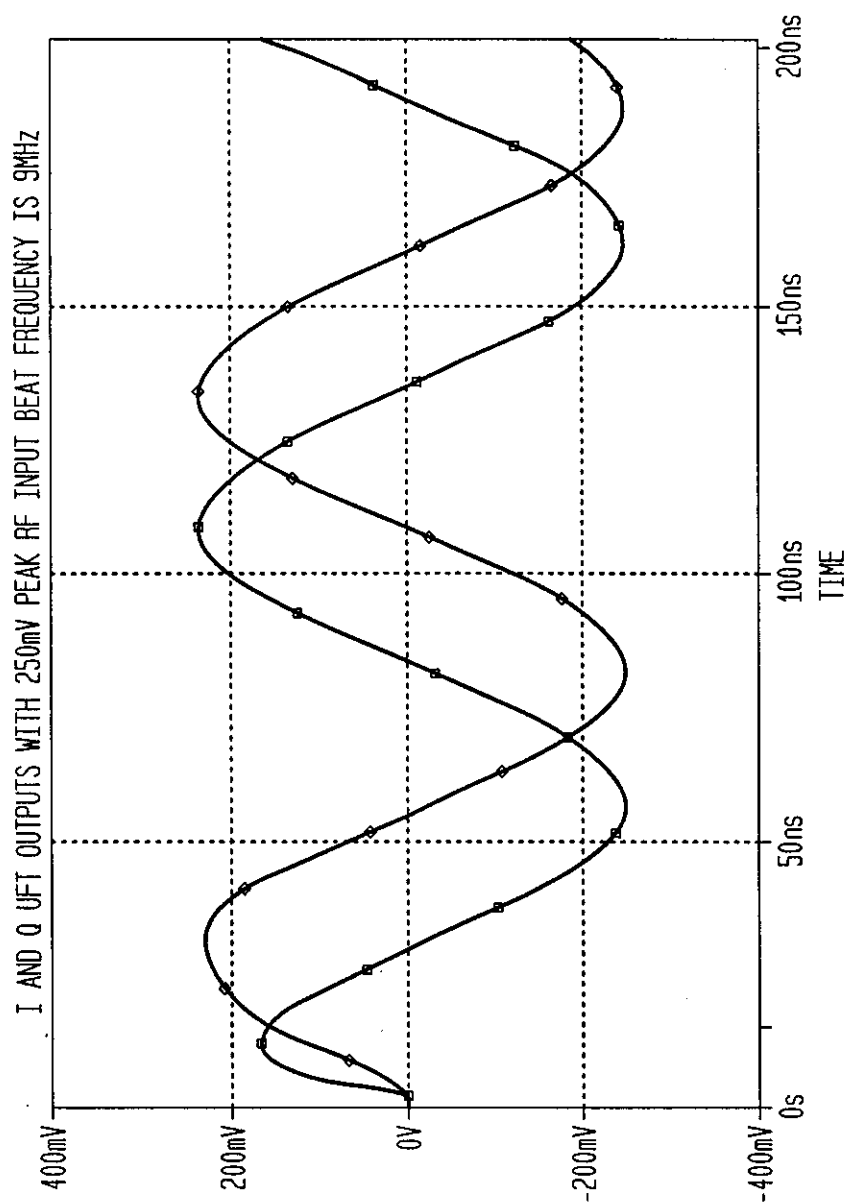


FIG. 180



204/283

FIG. 181



205/283

FIG. 182

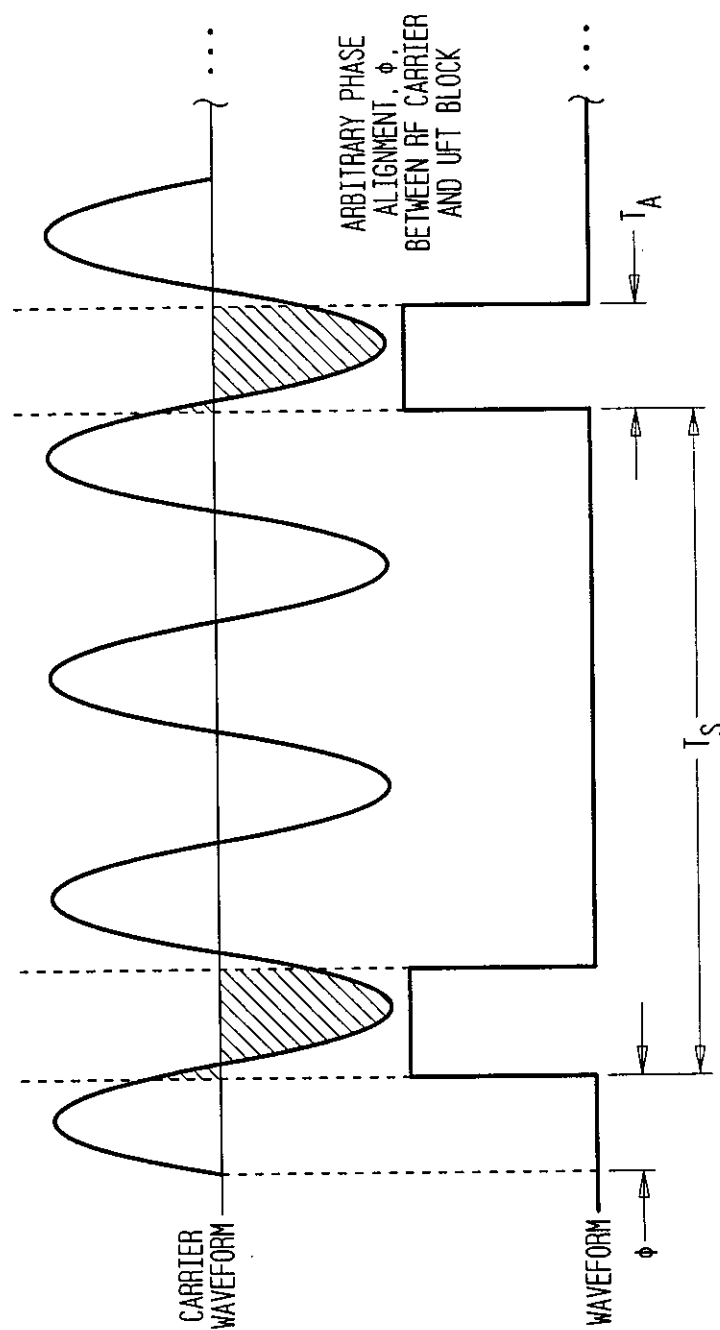


FIG. 183

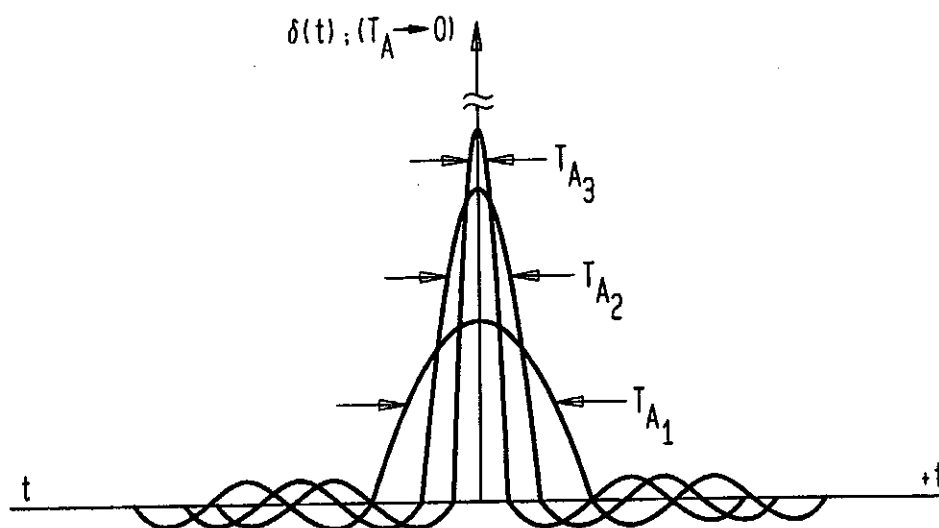
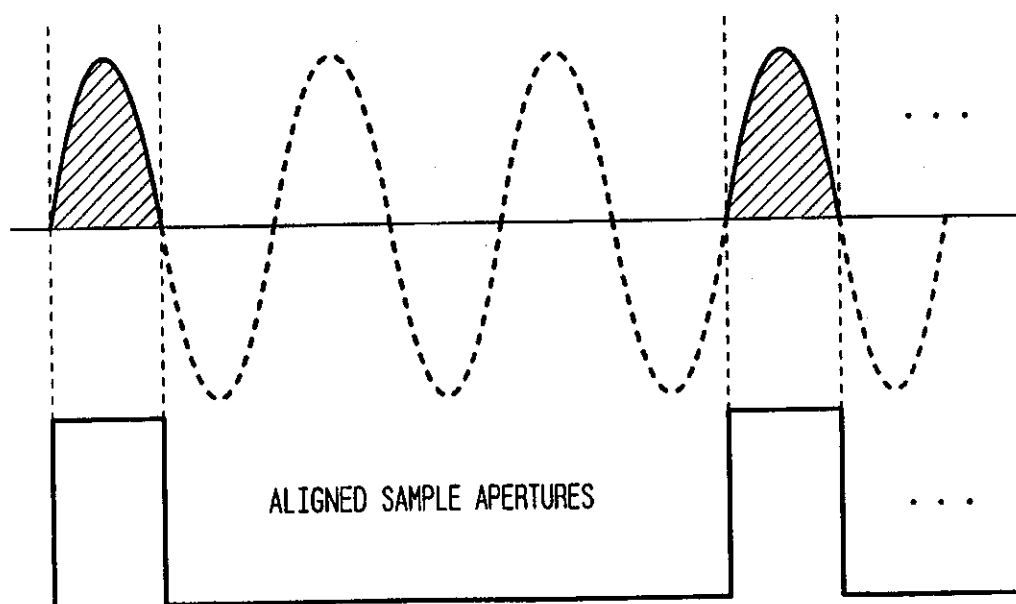


FIG. 184



207/283

FIG. 185

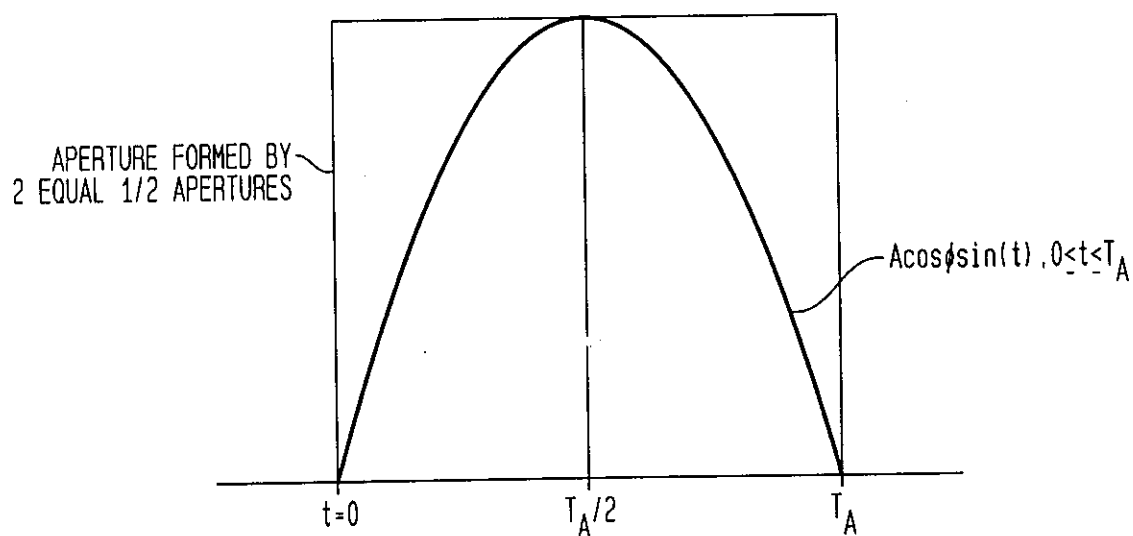
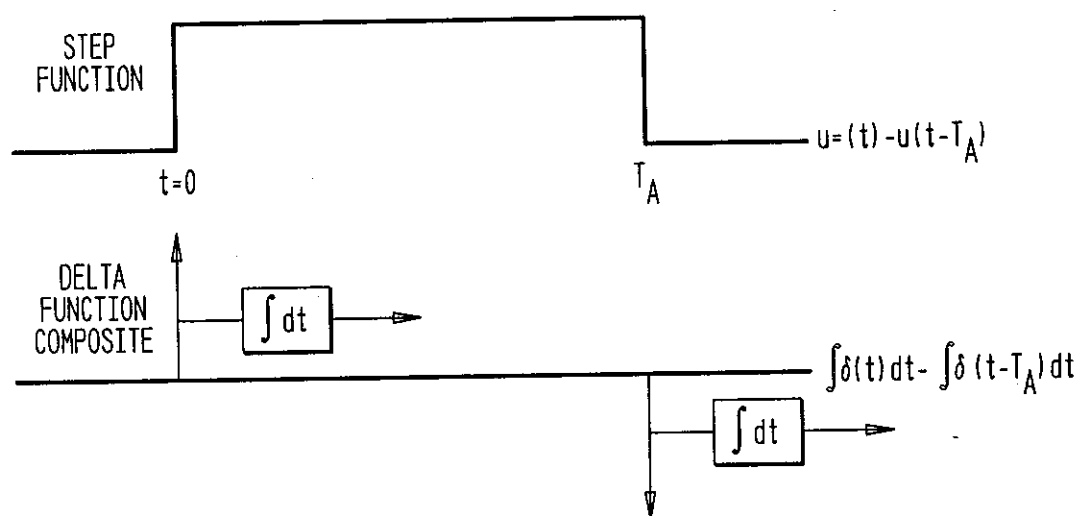


FIG. 186



208/283

FIG. 187

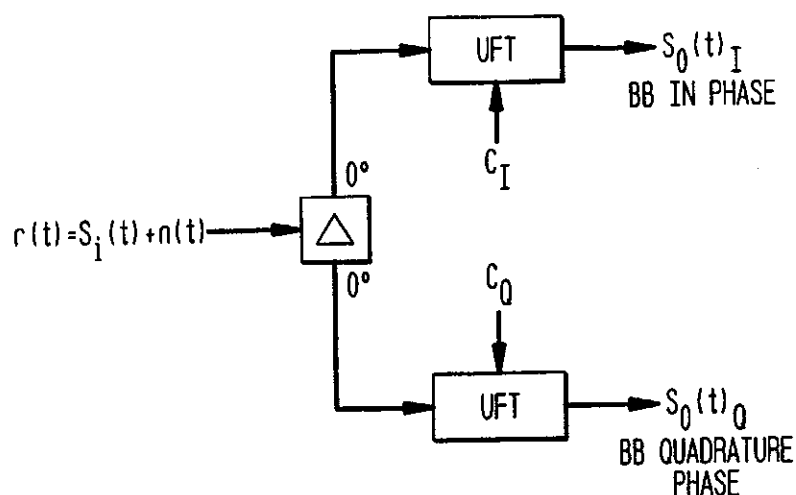


FIG. 188

$$C_I(t) = \sum_{m=-\infty}^{\infty} \delta(t - mT_S) * p_c(t) = \sum_{m=-\infty}^{\infty} p(t - mT_S) \quad 18802$$

$$C_I(t) = \sum_{m=-\infty}^{\infty} (u(t) - u(t - T_A)) * \delta(t - mT_S) \quad 18804$$

$$C_Q(t) = \sum_{m=-\infty}^{\infty} (u[t - T_A/2] - u[t - 3T_A/2]) * \delta(t - (mT_S + T_A/2)) \quad 18806$$

FIG. 189

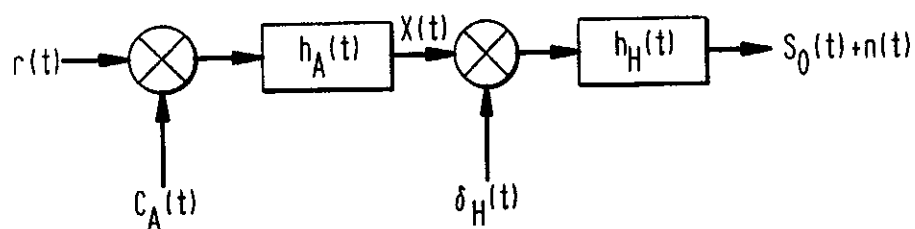


FIG. 190

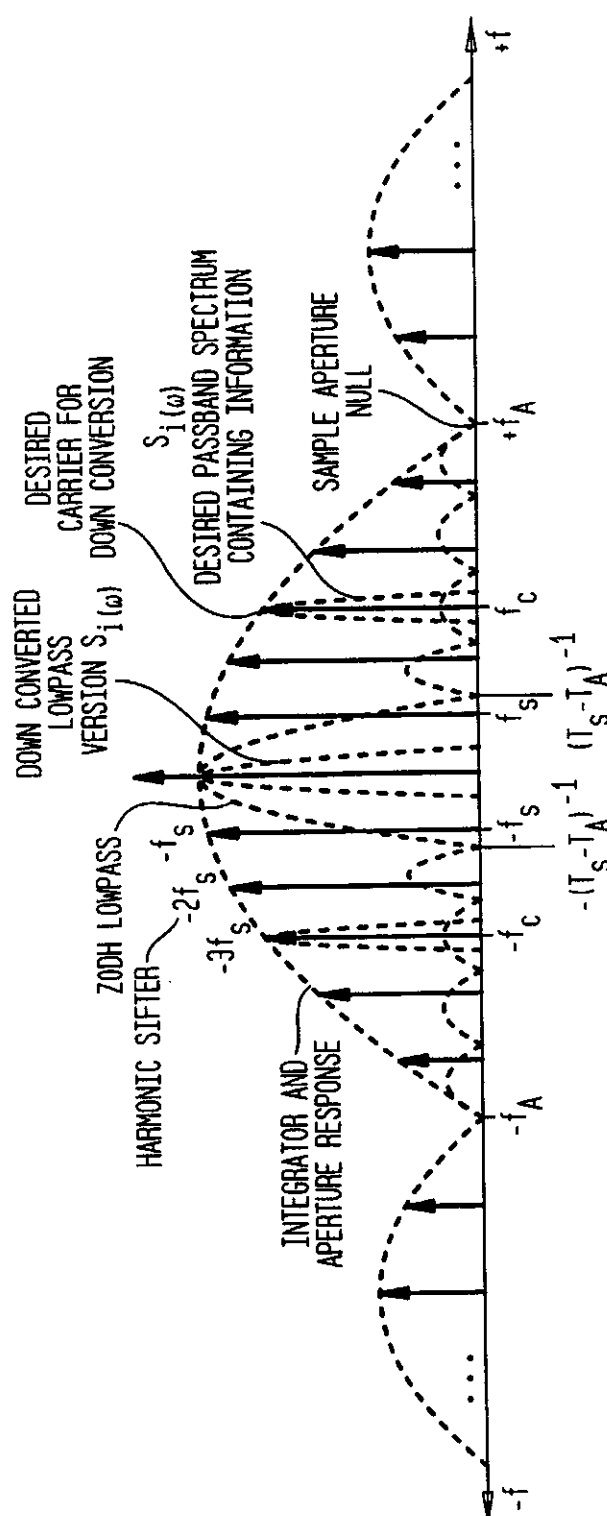


FIG. 191

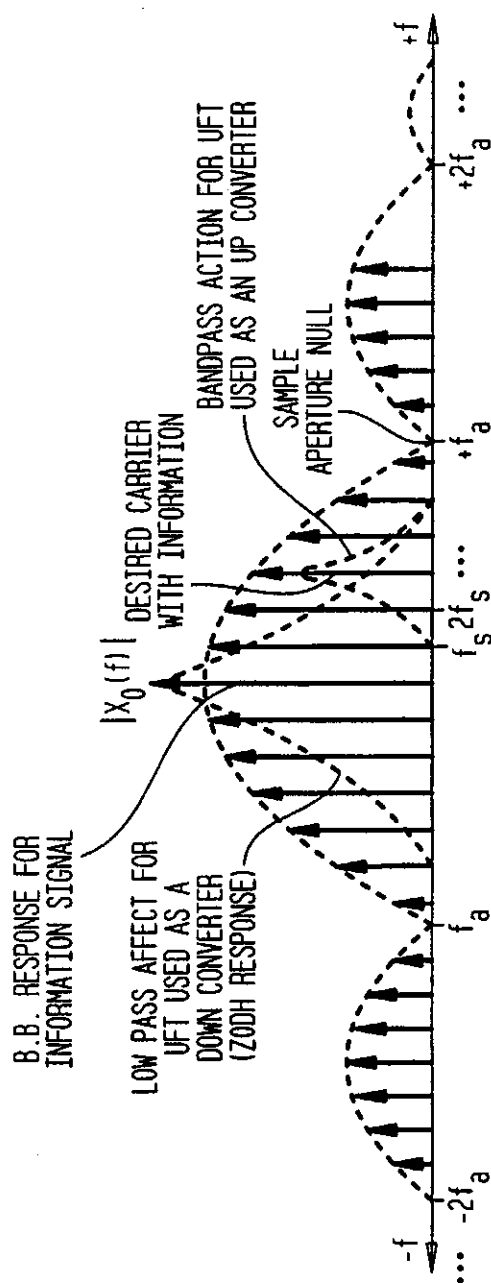
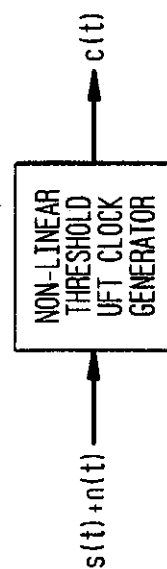
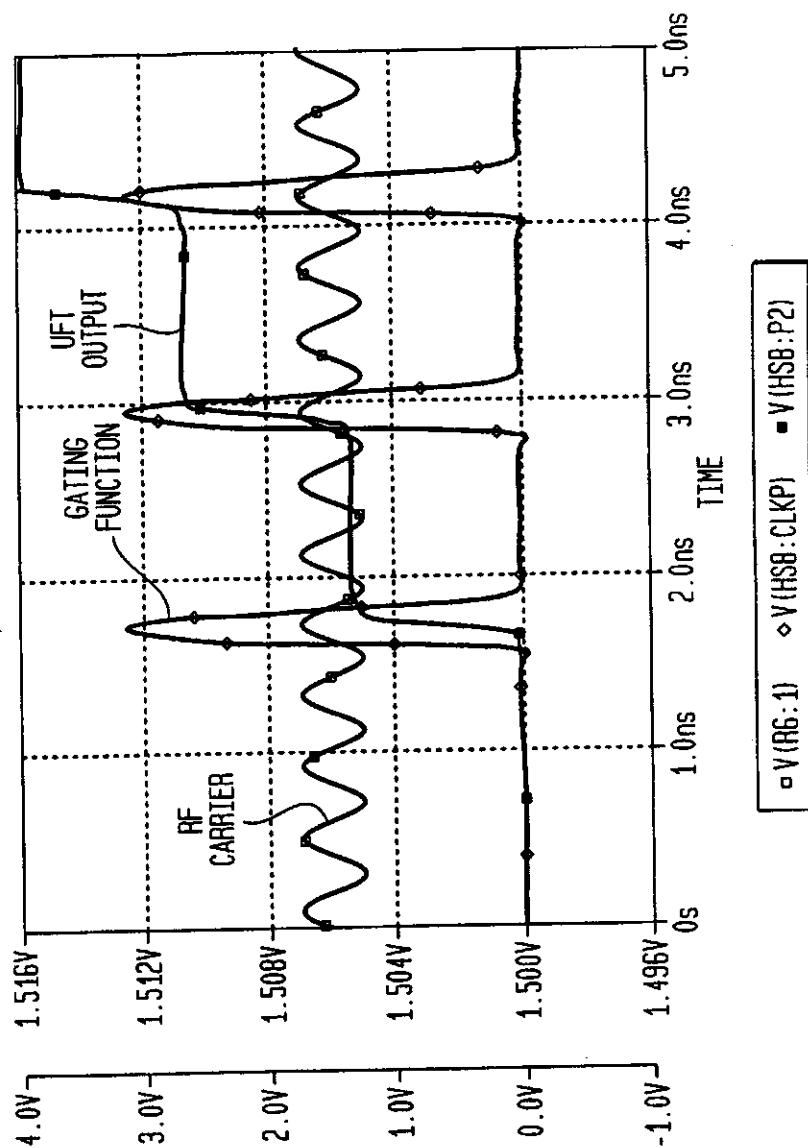


FIG. 192



212/283

FIG. 193



213/283

FIG. 194

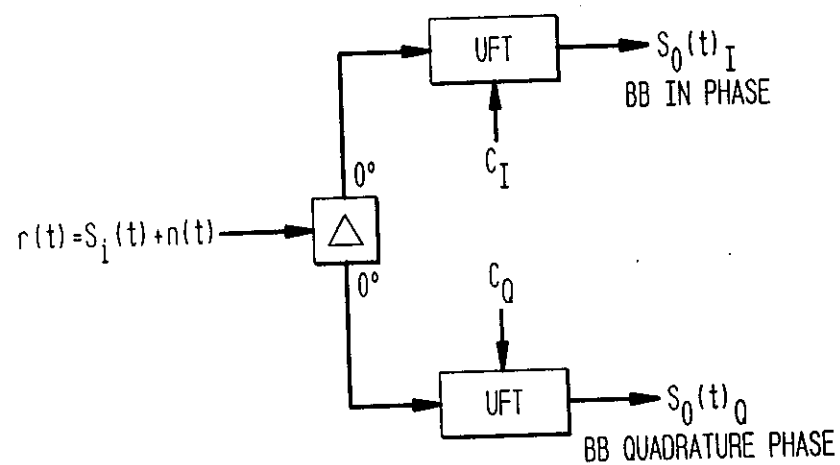


FIG. 195

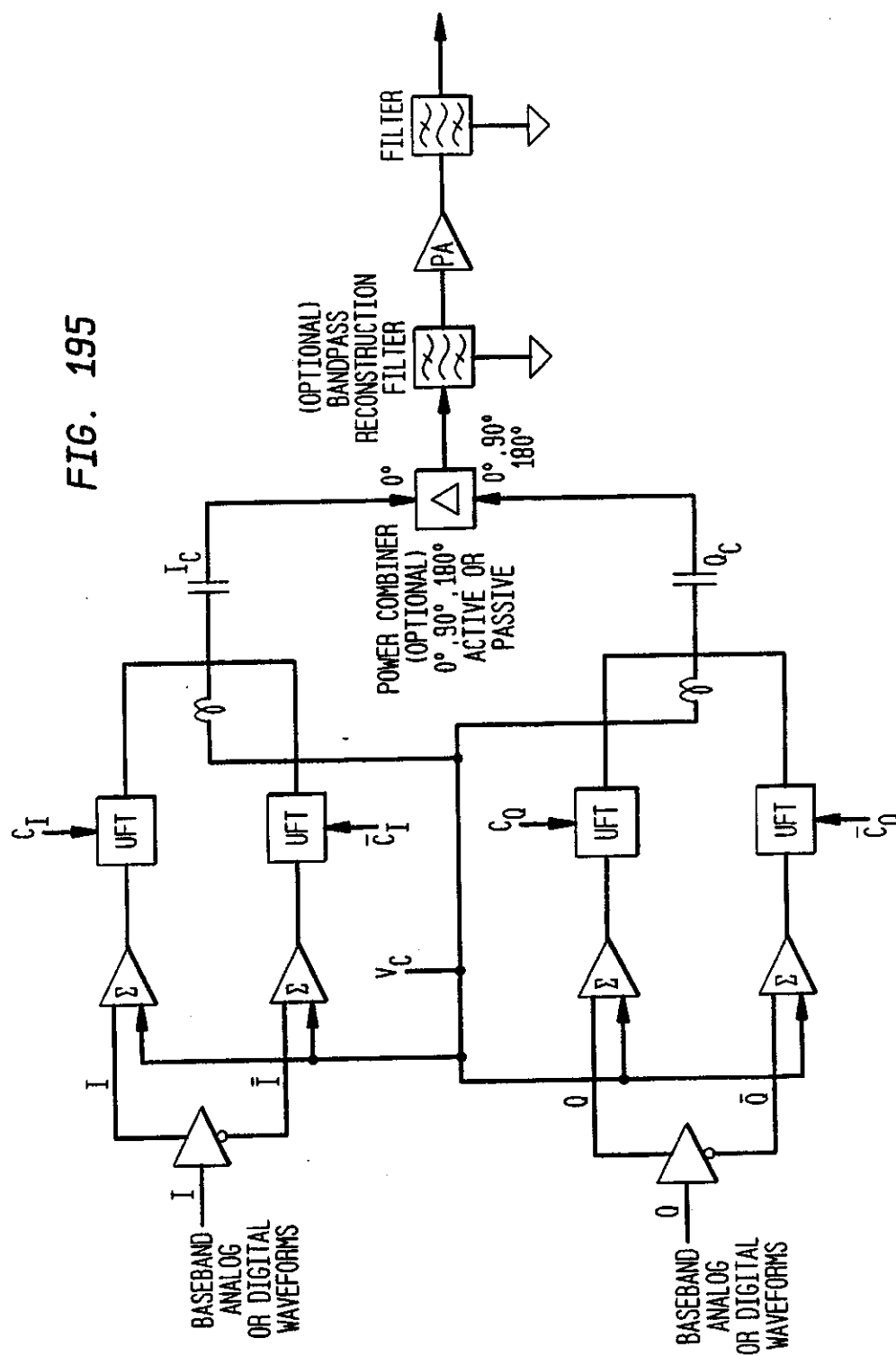


FIG. 196

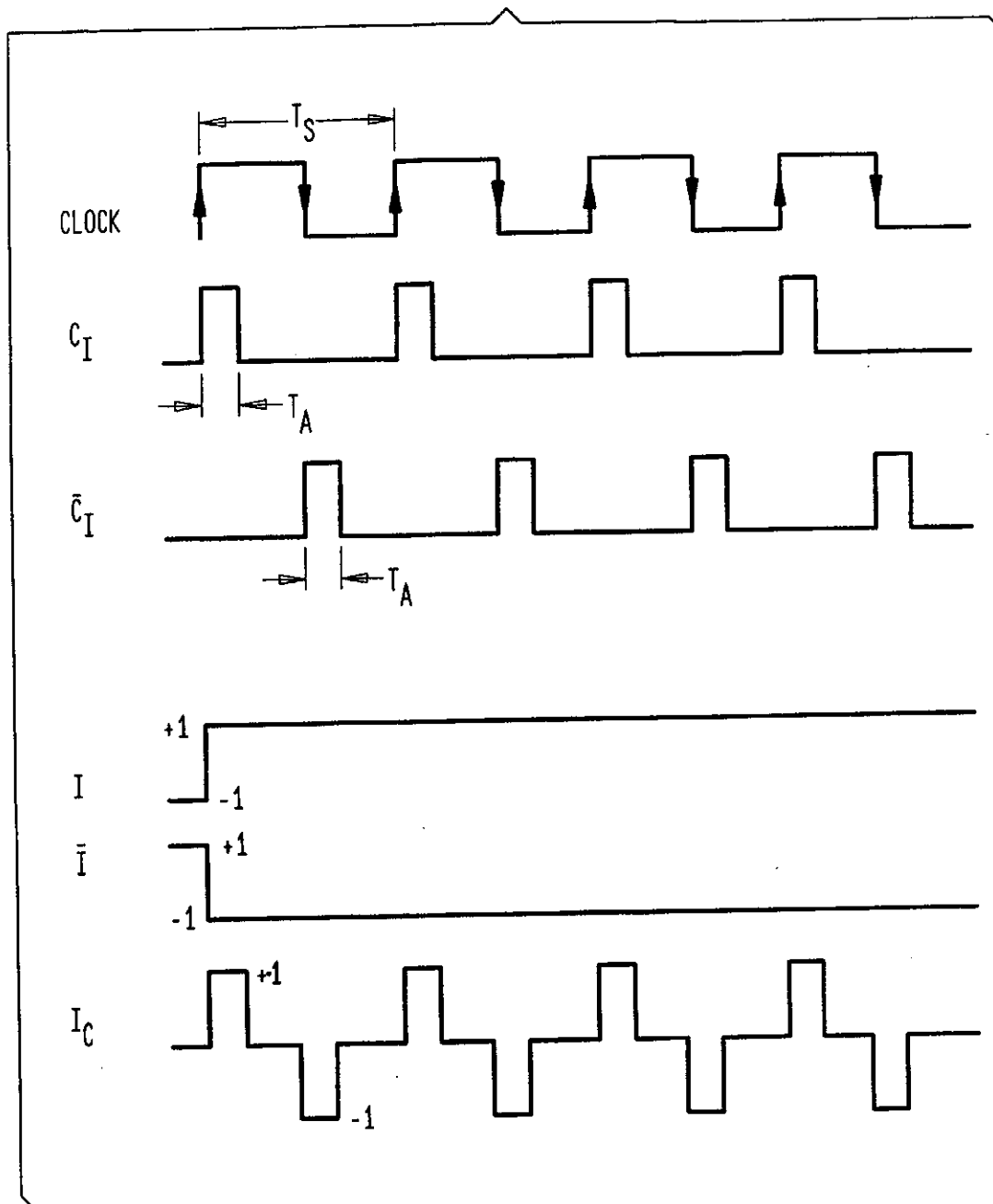
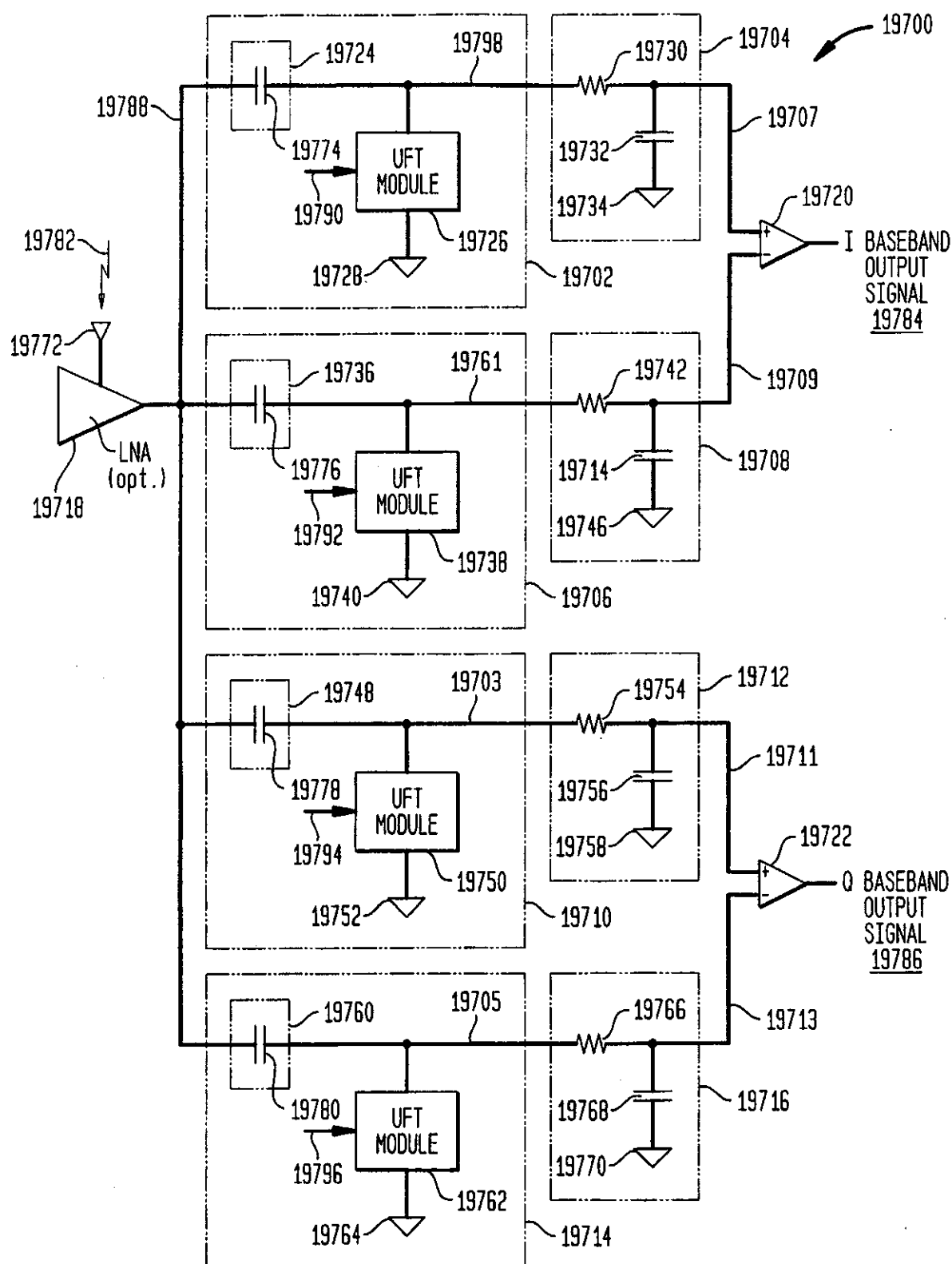


FIG. 197



217/283

FIG. 198

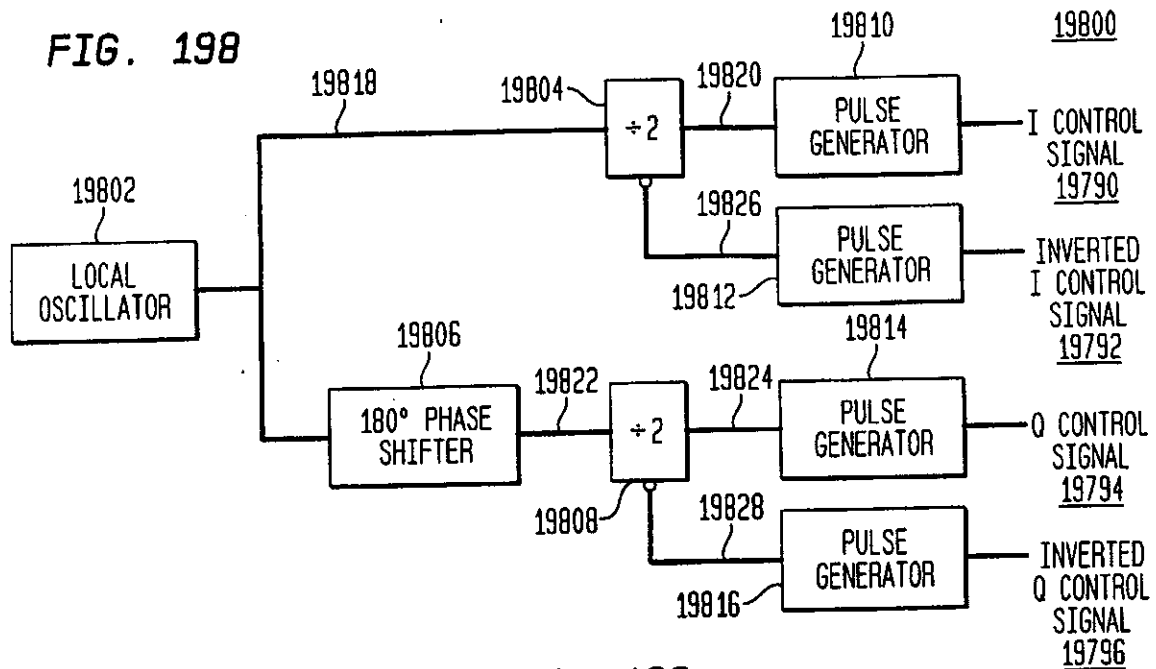
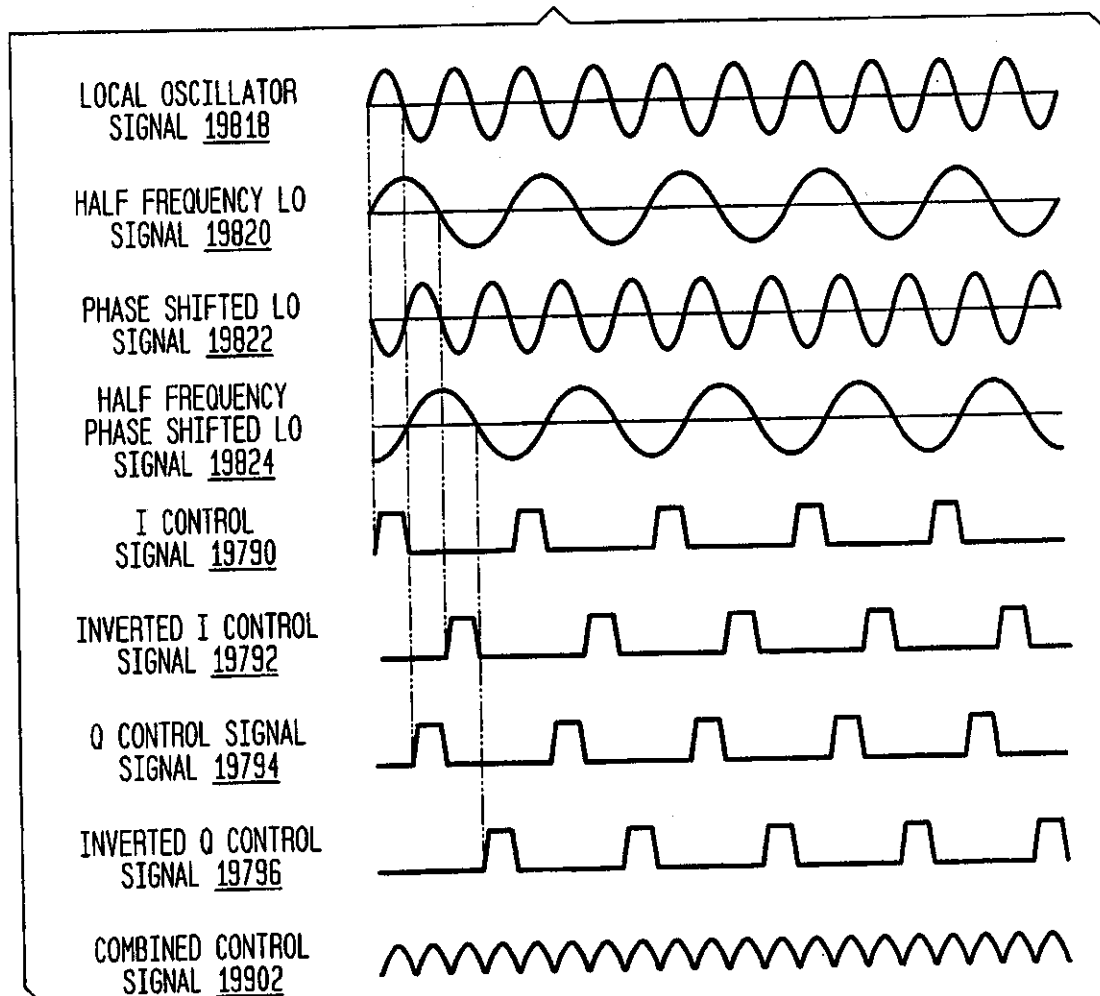
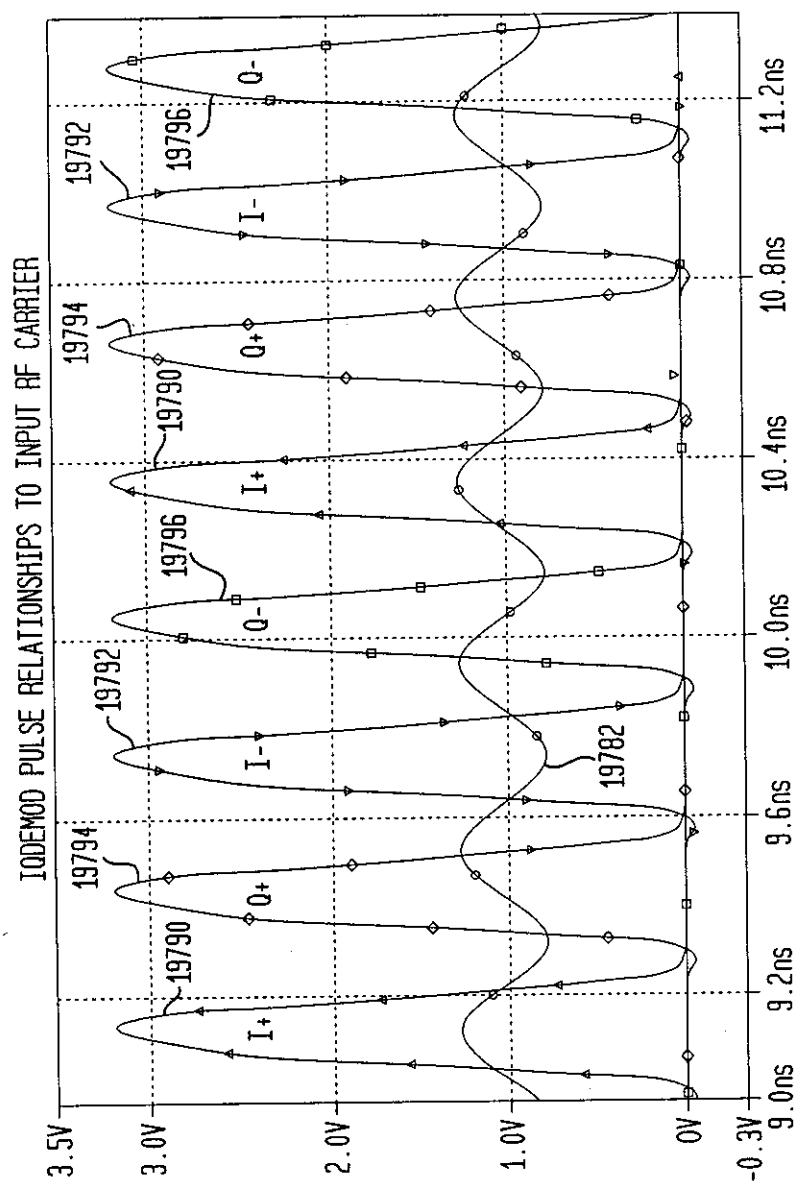


FIG. 199



218/283

FIG. 200



219/283

FIG. 201

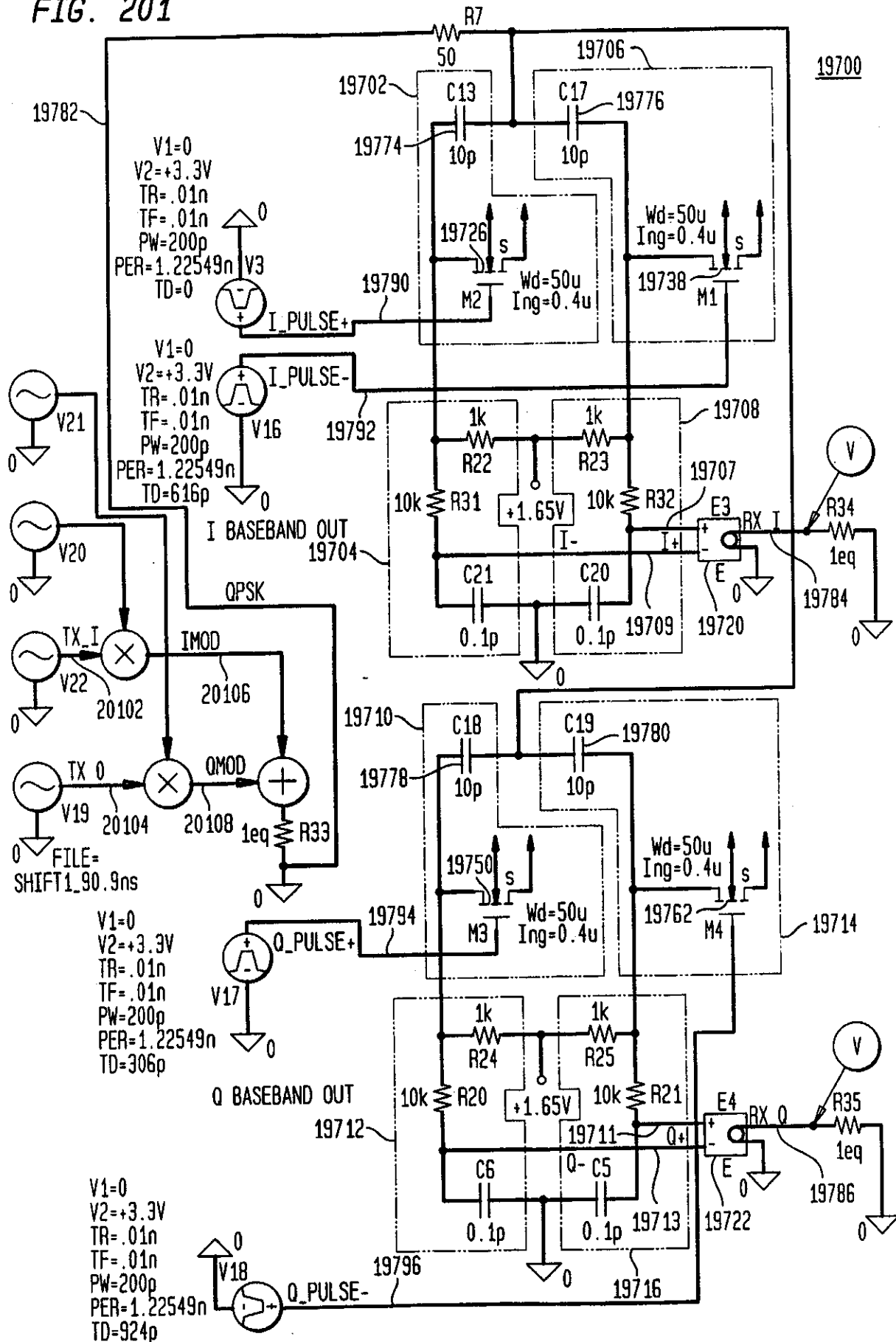


FIG. 202
IODEMOD SHOWING TIME RELATIONSHIP OF TX_I DATA

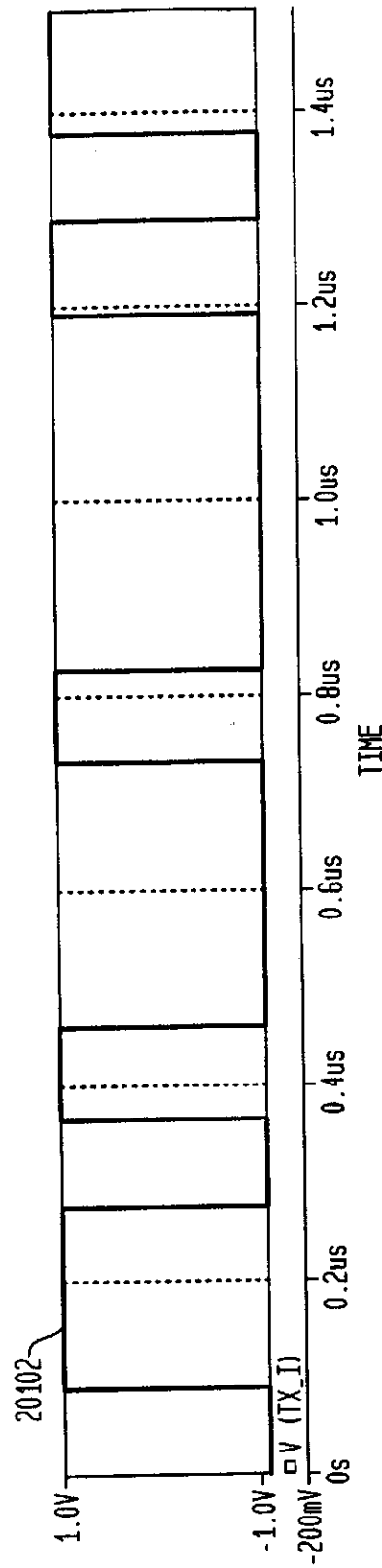
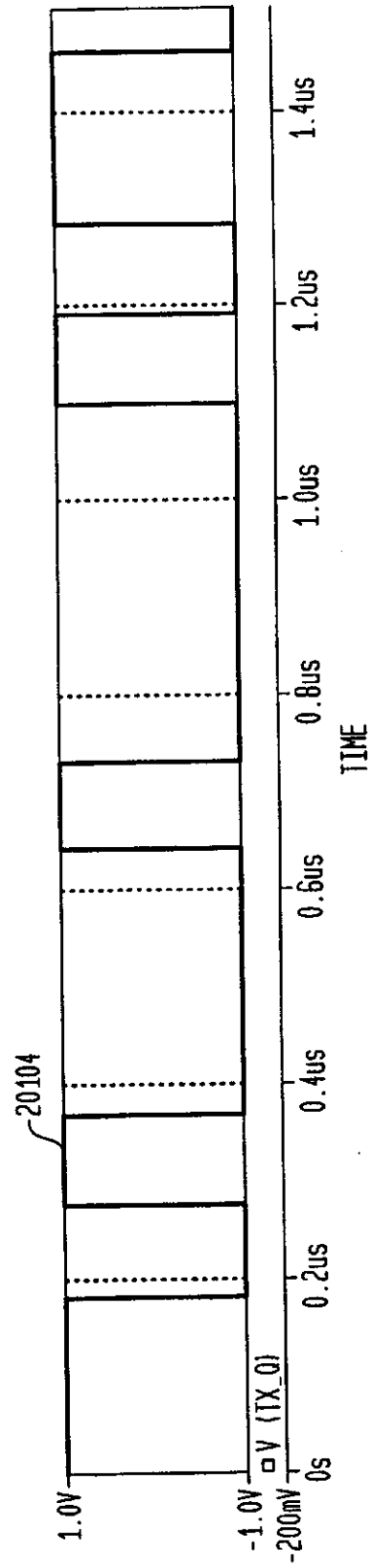
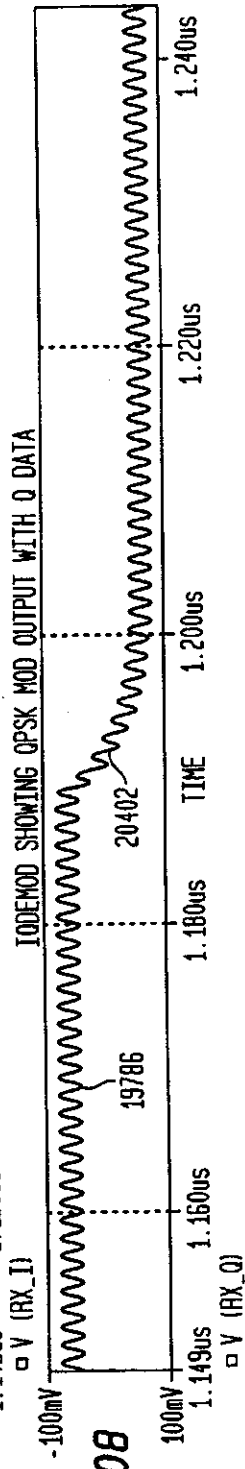
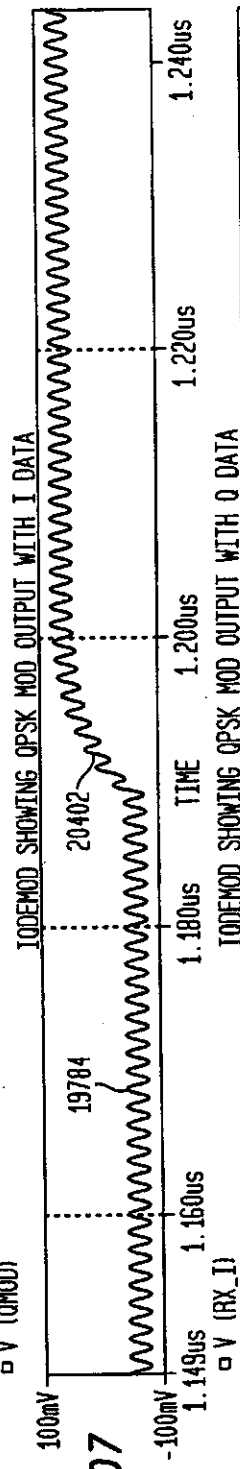
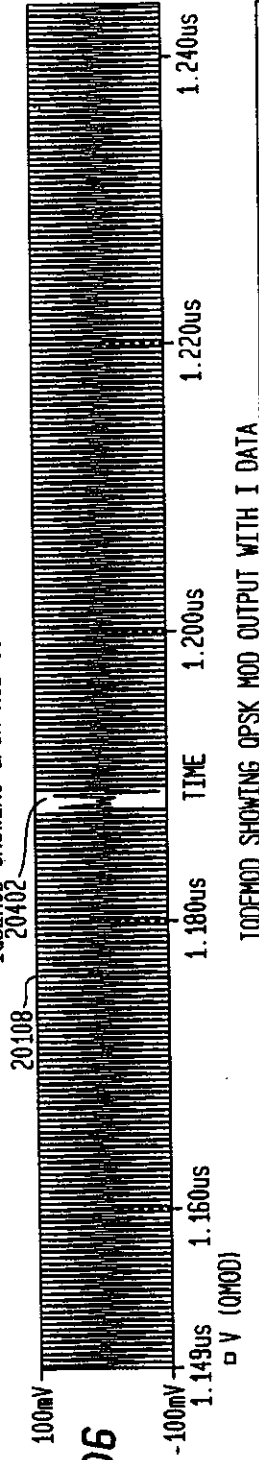
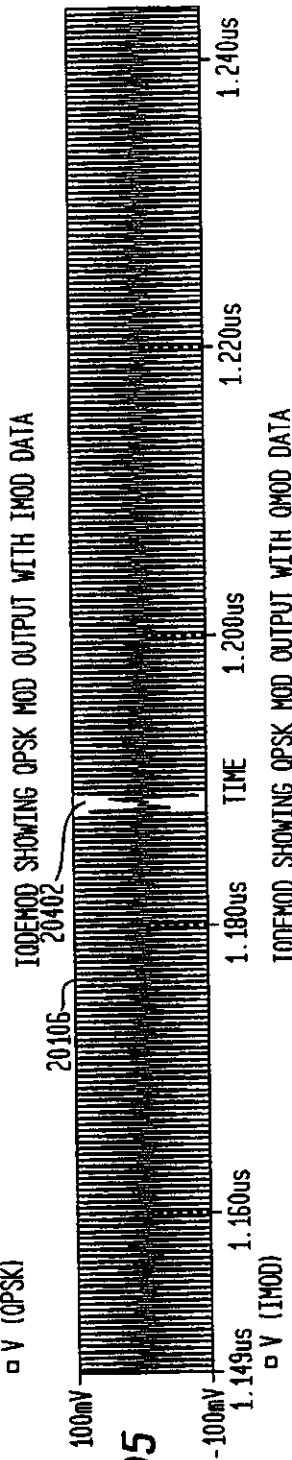
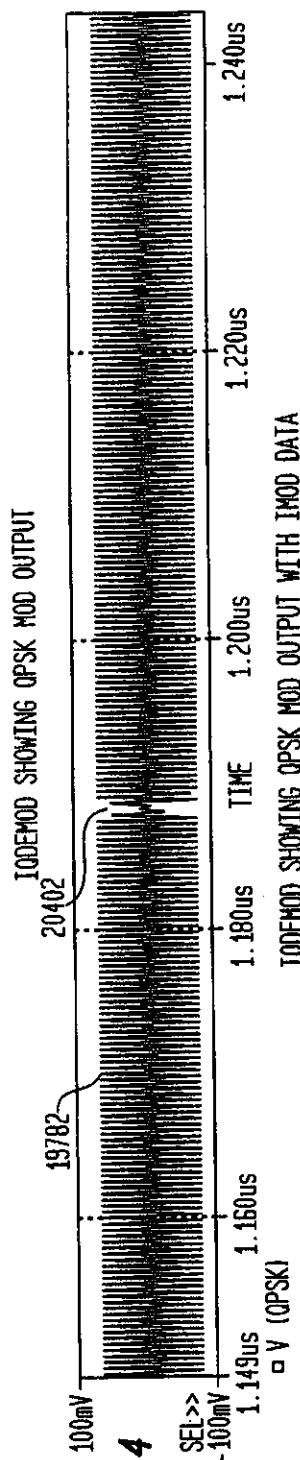


FIG. 203
IODEMOD SHOWING TIME RELATIONSHIP OF TX_Q DATA





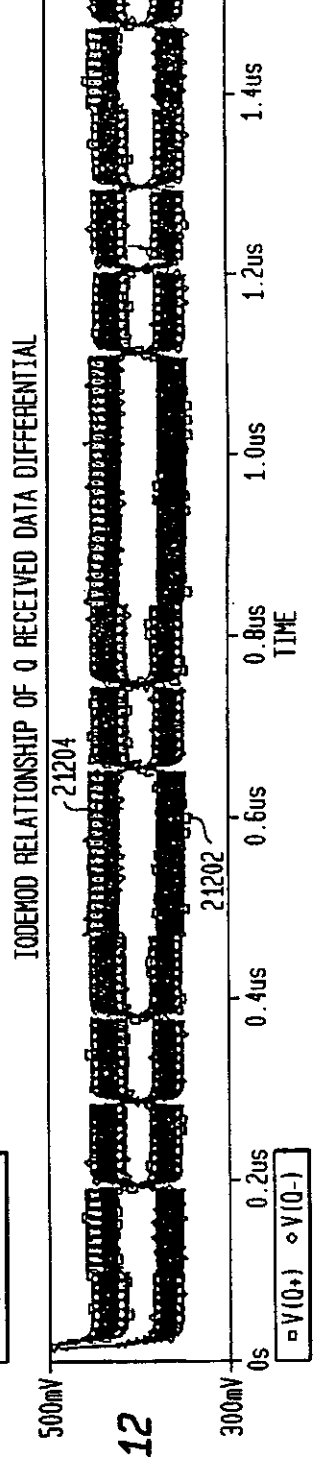
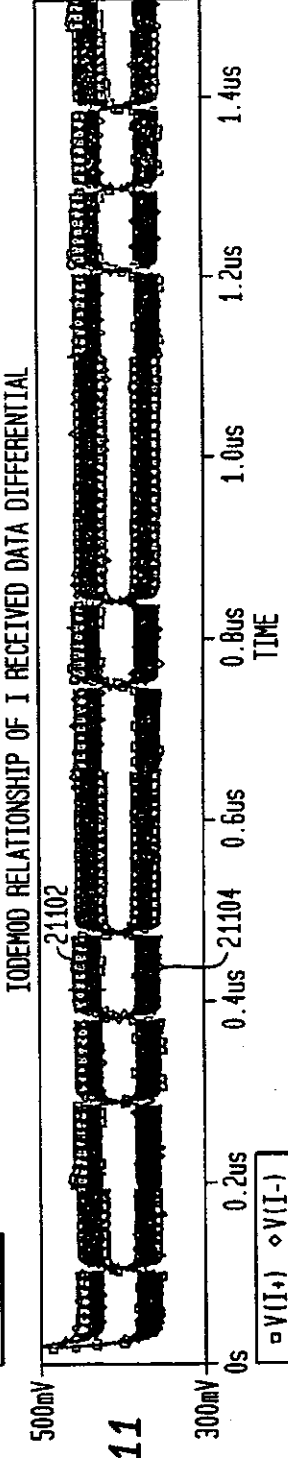
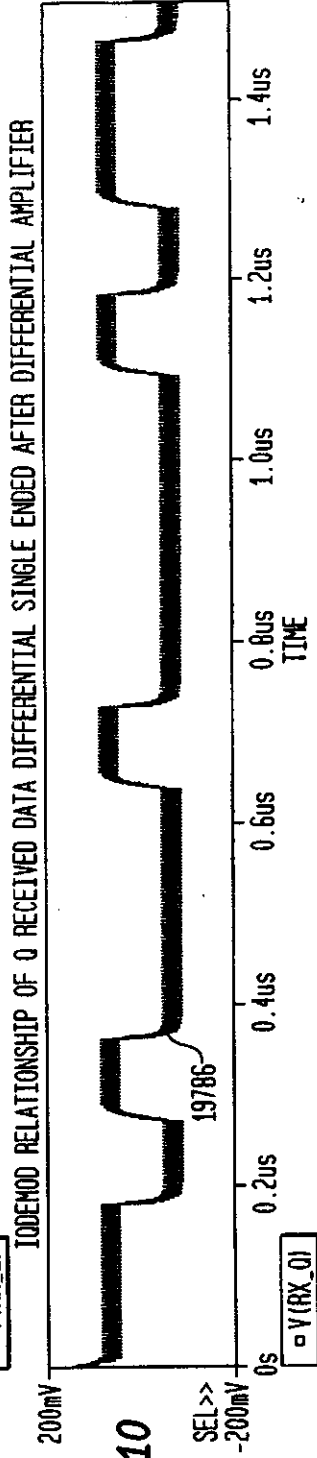
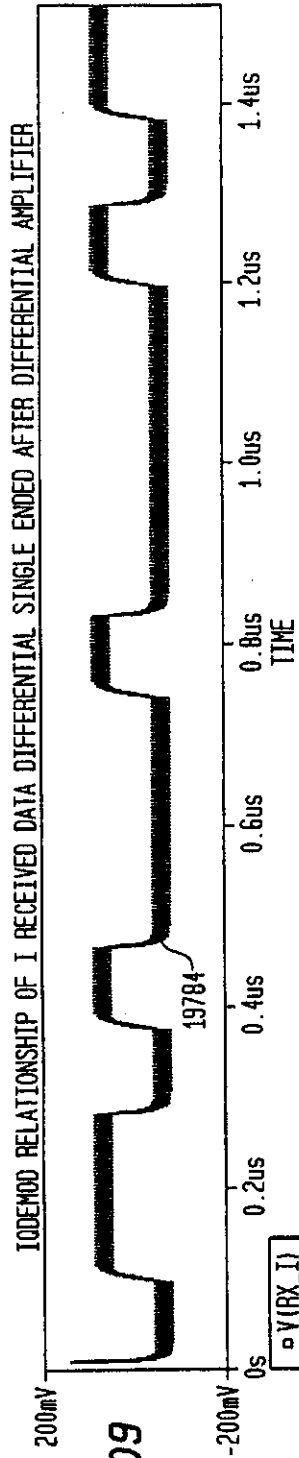
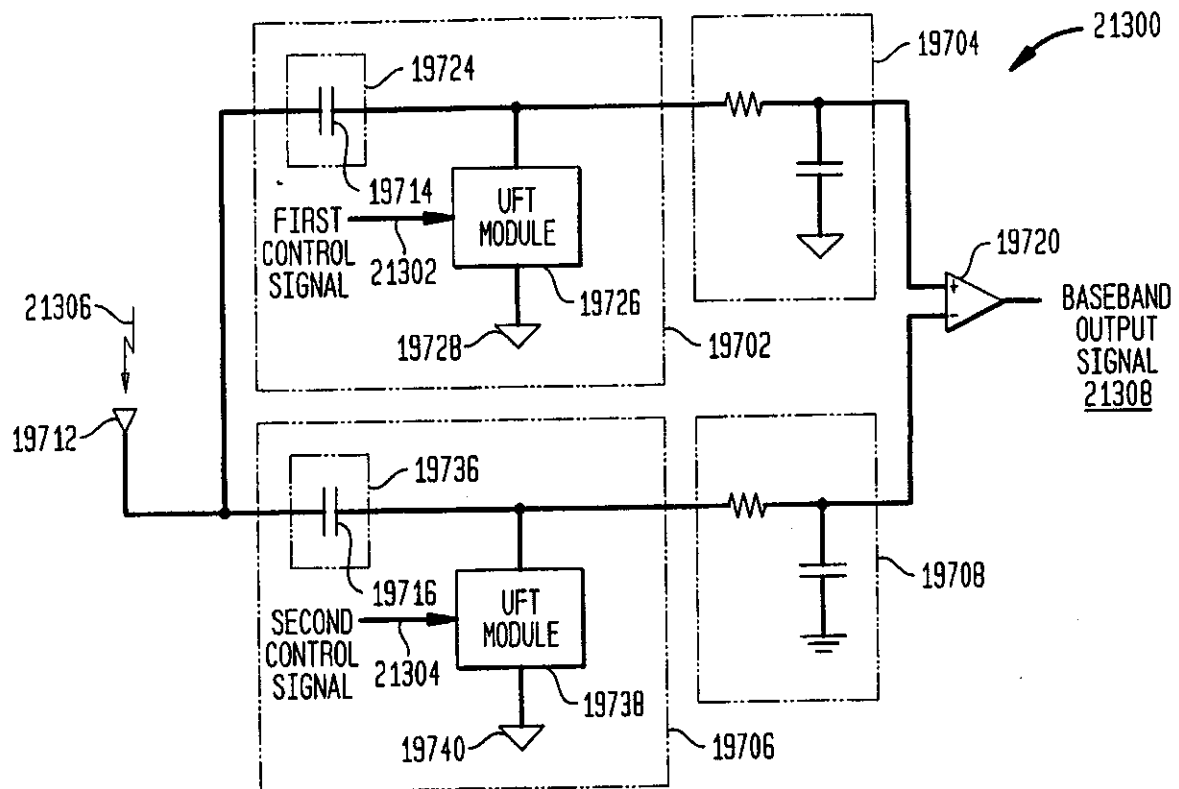
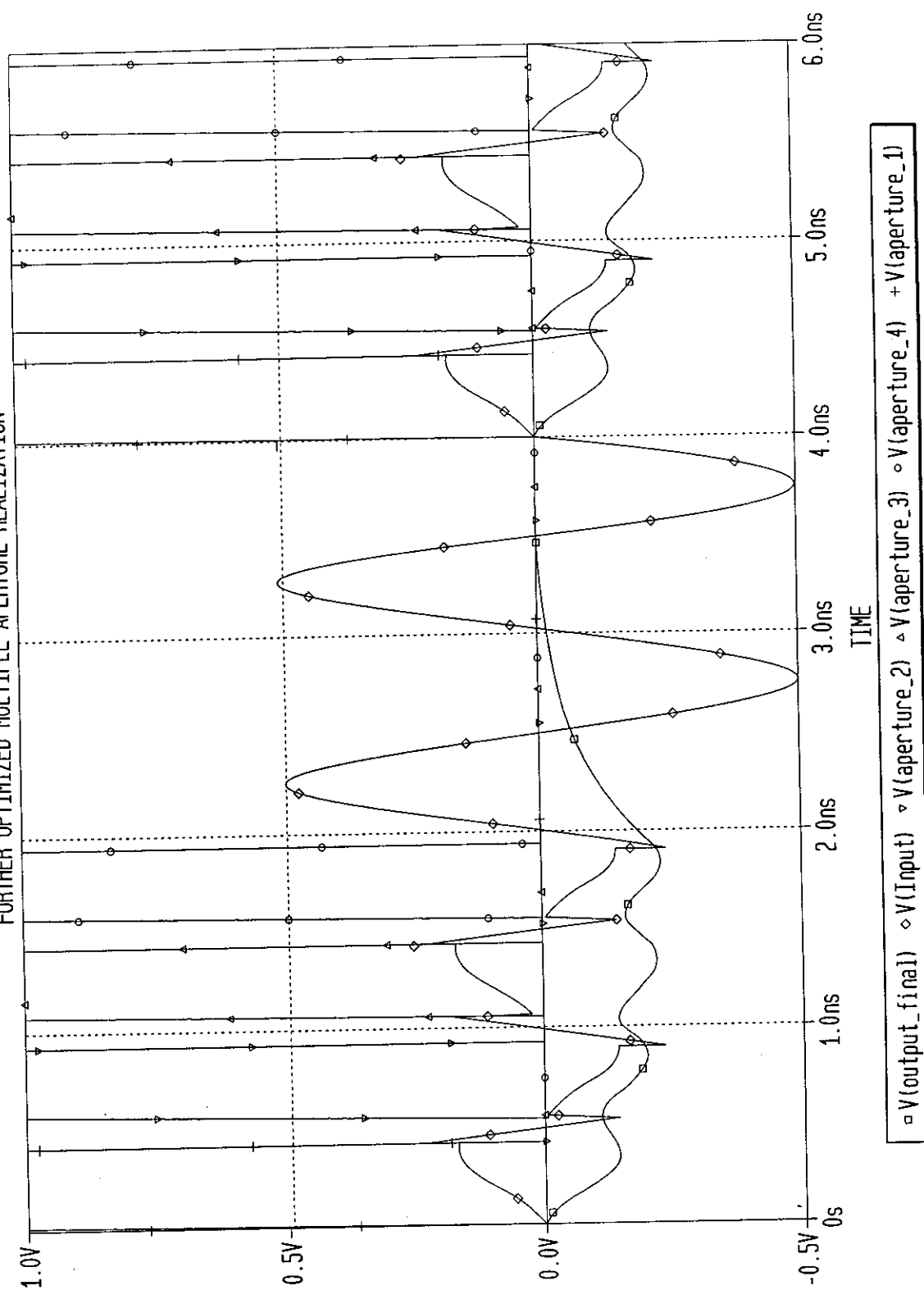


FIG. 213



224/283

FIG. 214
FURTHER OPTIMIZED MULTIPLE APERTURE REALIZATION



225/283

FIG. 215

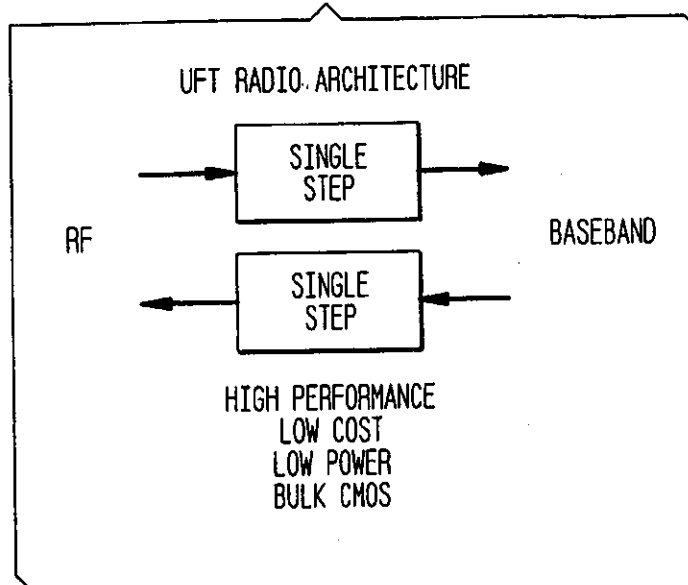
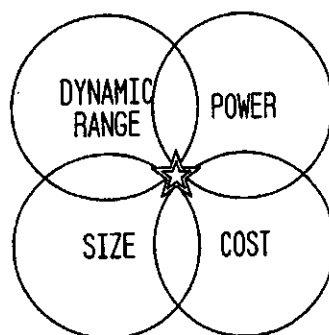


FIG. 216

WIRELESS TRADE-OFF DESIGN CONCERNS



226/283

FIG. 217

NOISE FIGURE CALCULATIONS BASED ON RMS
VOLTAGE AND CURRENT NOISE SPECIFICATIONS

ENTER, THE VOLTAGE NOISE DENSITY, e_n , AND THE
CURRENT NOISE DENSITY, i_n , FOR THE AMPLIFIER CHOSEN:

$$e_n := 6 \cdot 10^{-9} \text{ V/sqrt(Hz)}$$

$$i_n := 1 \cdot 10^{-12} \text{ A/sqrt(Hz)}$$

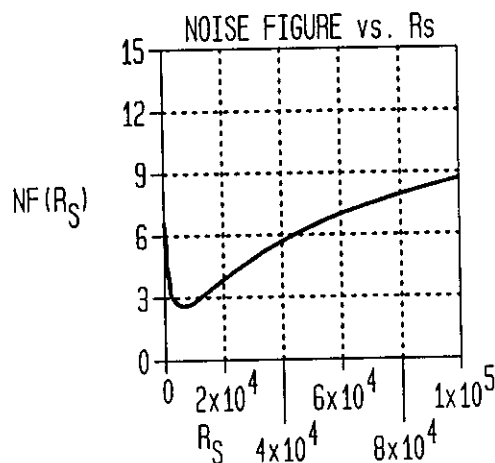
ENTER THE SOURCE RESISTANCE DRIVING THE AMPLIFIER:

$$K := 1.38 \cdot 10^{-23} \text{ J/K} \quad T := 290\text{K}$$

$$\text{PARALELL}(x,y) := \frac{x \cdot y}{x+y} \quad \text{NF}(R_S) := 20 \cdot \log \left(\sqrt{\frac{e_n^2 + 4 \cdot K \cdot T \cdot R_S + i_n^2 \cdot R_S^2}{4 \cdot K \cdot T \cdot R_S}} \right)$$

IF WE PLOT NOISE FIGURE VERSUS SOURCE RESISTANCE WE CAN GET
AN IDEA OF WHAT IS THE OPTIMUM SOURCE RESISTANCE.
IT IS NOT NECESSARILY THE LOWEST RESISTANCE!

$$R_S := 100, 200, \dots, 100 \cdot 10^3$$



227/283

FIG. 218A

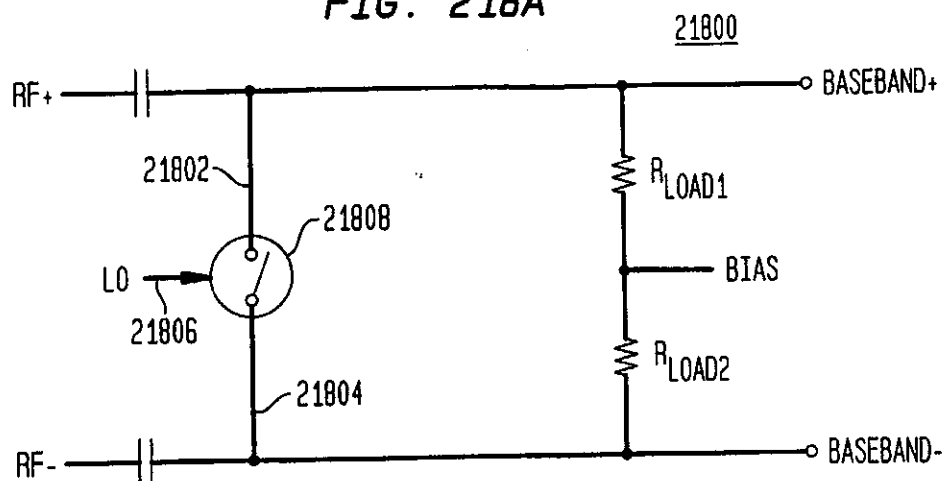


FIG. 218B

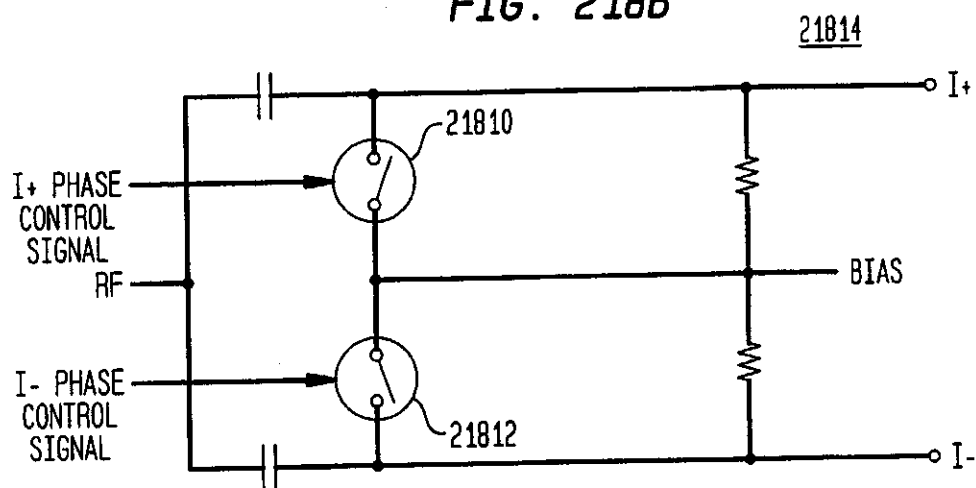
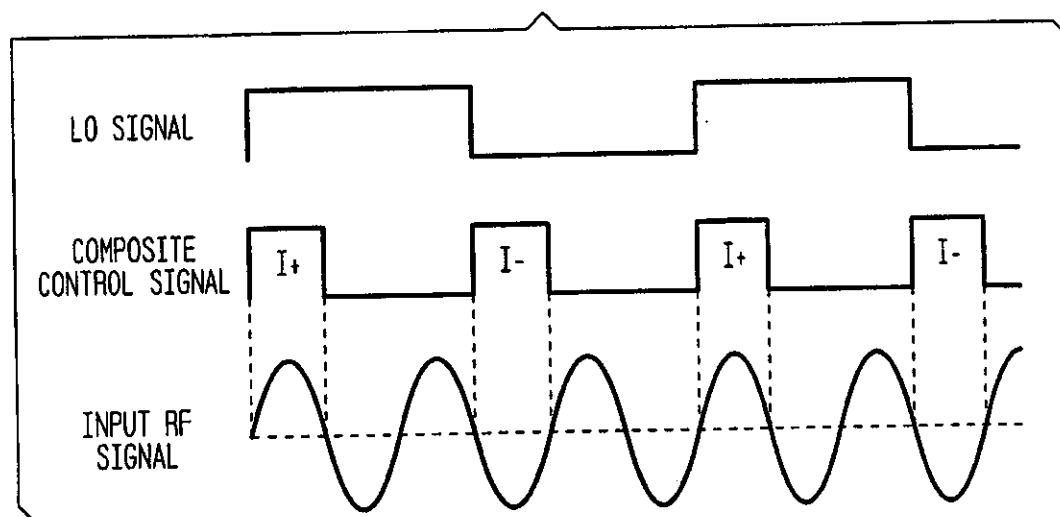


FIG. 218C



228/283

FIG. 218D

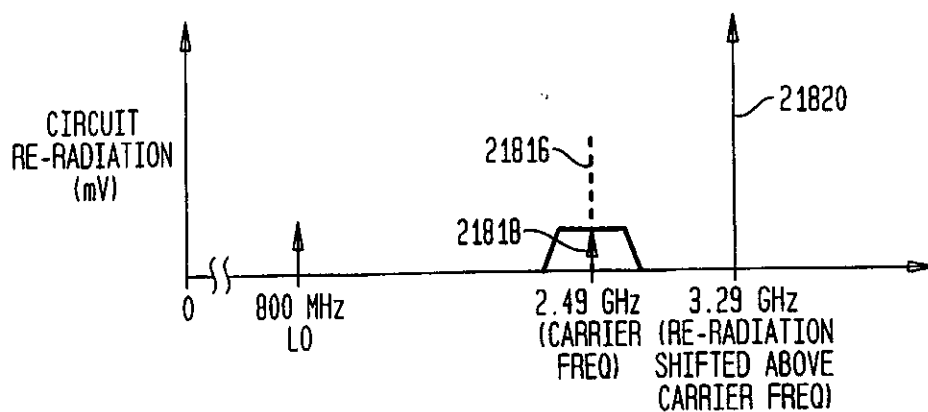


FIG. 218F

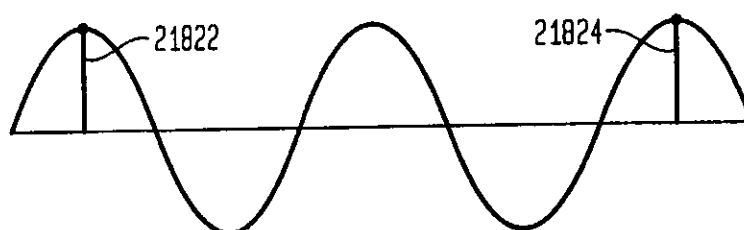


FIG. 218G

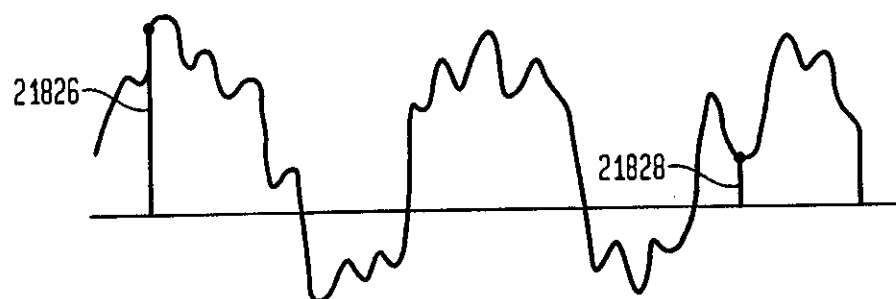
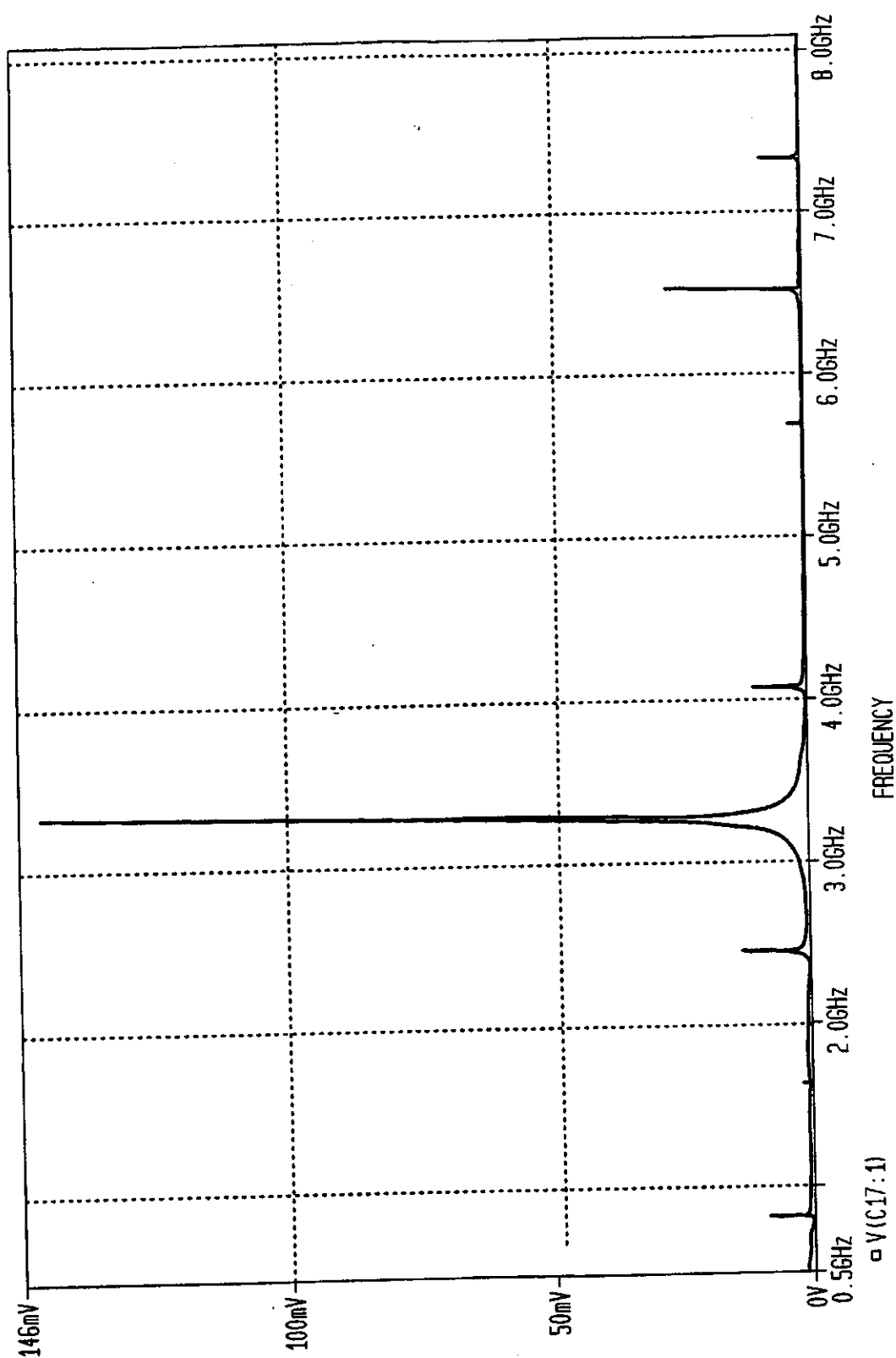


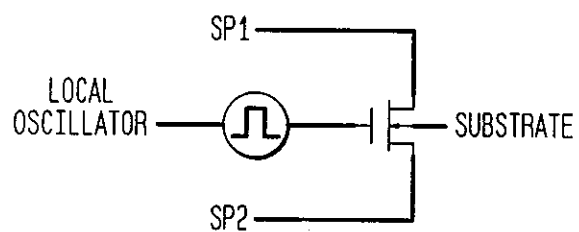
FIG. 218E



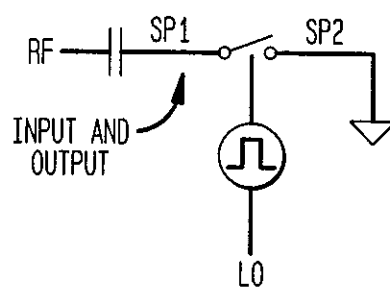
230/283

FIG. 219

IC CONCEPTUAL SCHEMATIC

*FIG. 220*

BASIC ARCHITECTURE



231/283

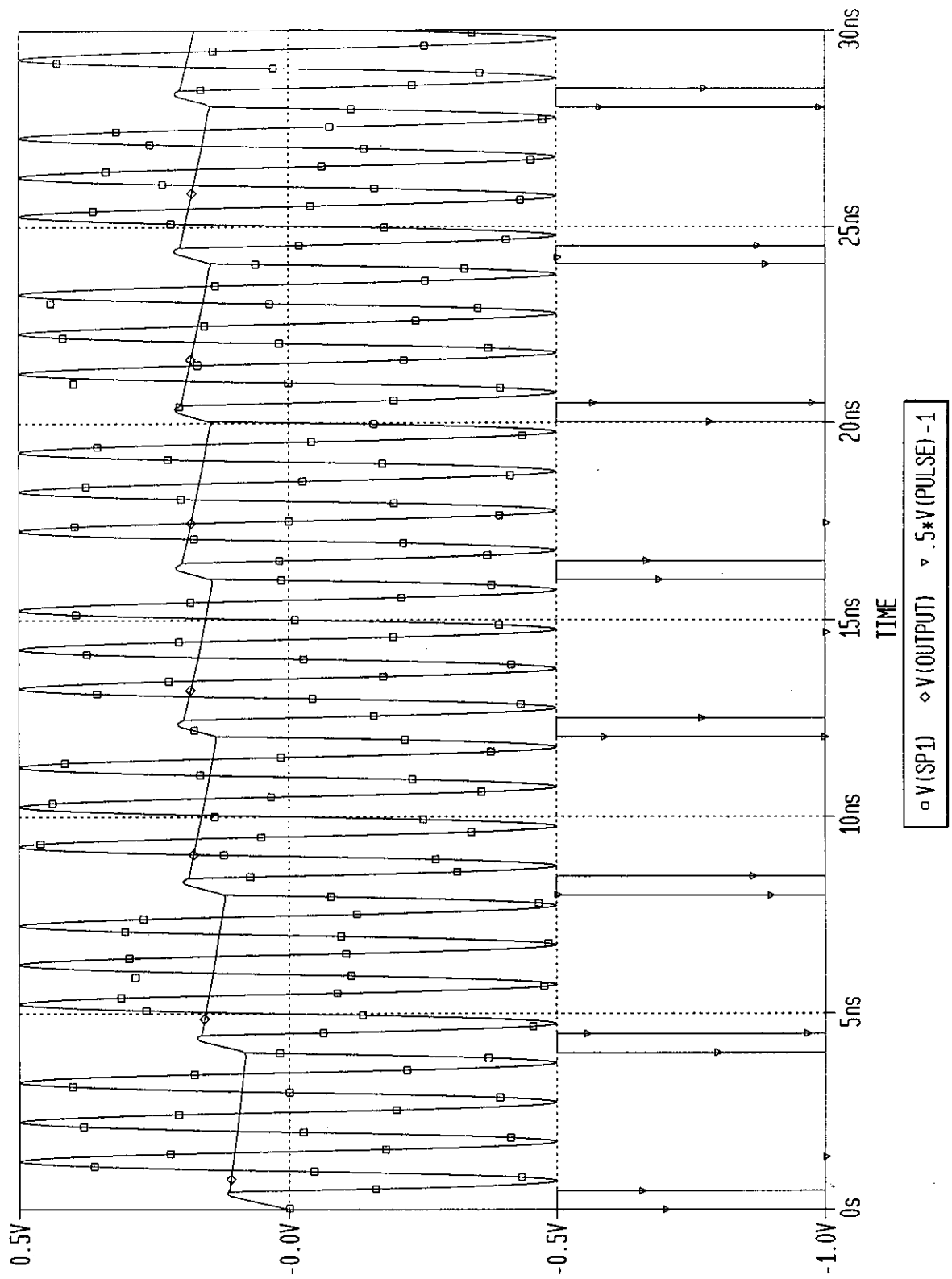


FIG. 221

232/283

FIG. 222

DC EQUATIONS

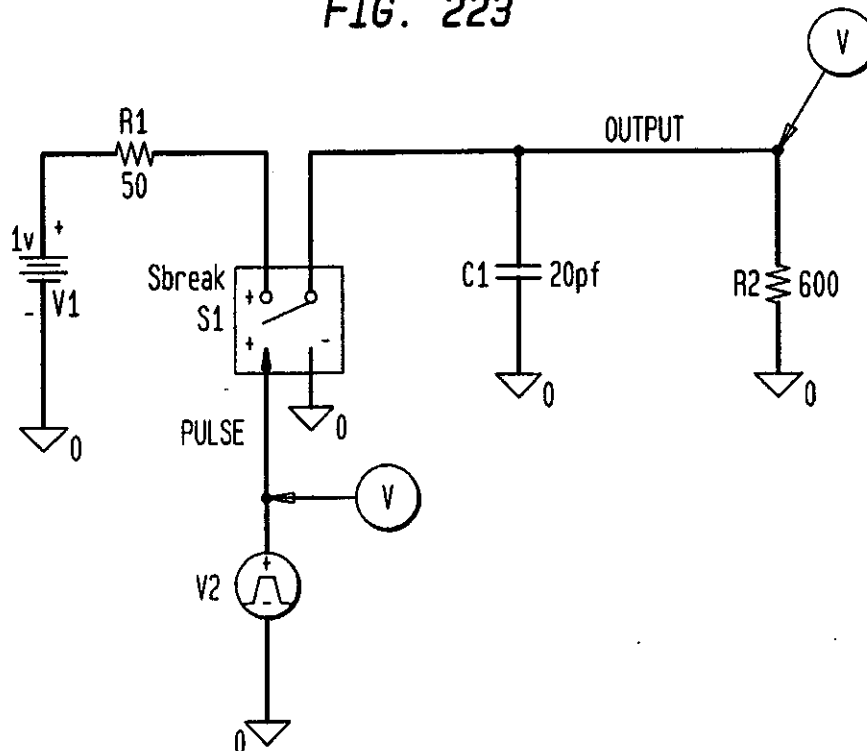
$$V_{in} = V \cdot \frac{R_{out}}{R_{in} + R_{out}}$$

$$V_c = V_{in} - (V_{in} - V_{init}) \cdot \exp\left(\frac{-t_c}{R_{in} \cdot C}\right)$$

$$V_d = V_c \cdot \exp\left(\frac{-t_d}{R_{out} \cdot C}\right)$$

DEFENITIONS: Rin - INPUT RESISTANCE
 Rout - OUTPUT RESISTANCE
 C - CAPACITOR
 tc - CHARGE TIME OR APERATURE
 td - DISCHARGE TIME OR LO PERIOD-tc
 V - INPUT VOLTAGE
 Vinit - INITIAL CAPACITOR VOLTAGE
 Vc - FINAL CHARGE CAPACITOR VOLTAGE
 Vd - FINAL DISCHARGE CAPACITOR VOLTAGE

FIG. 223



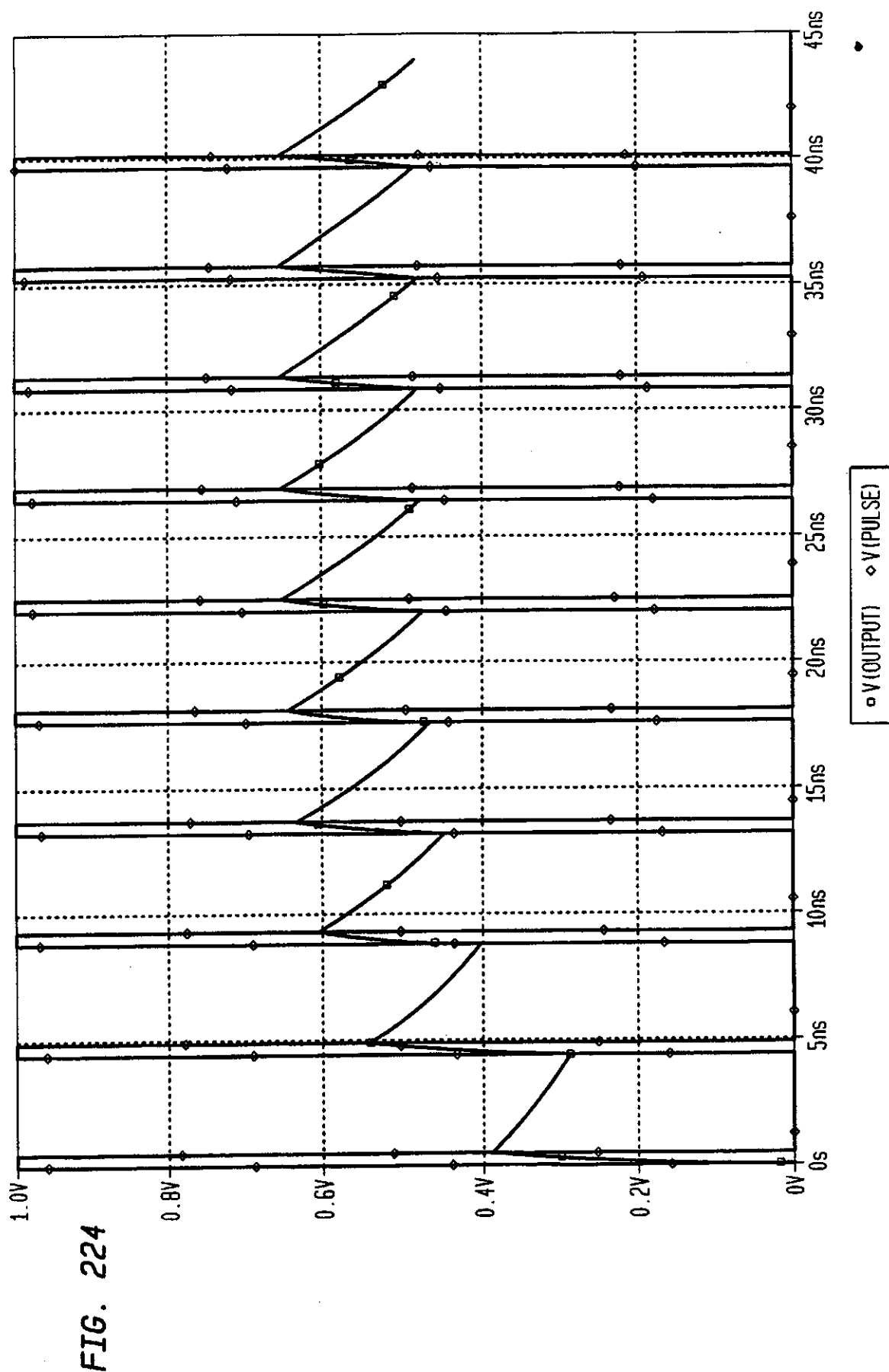
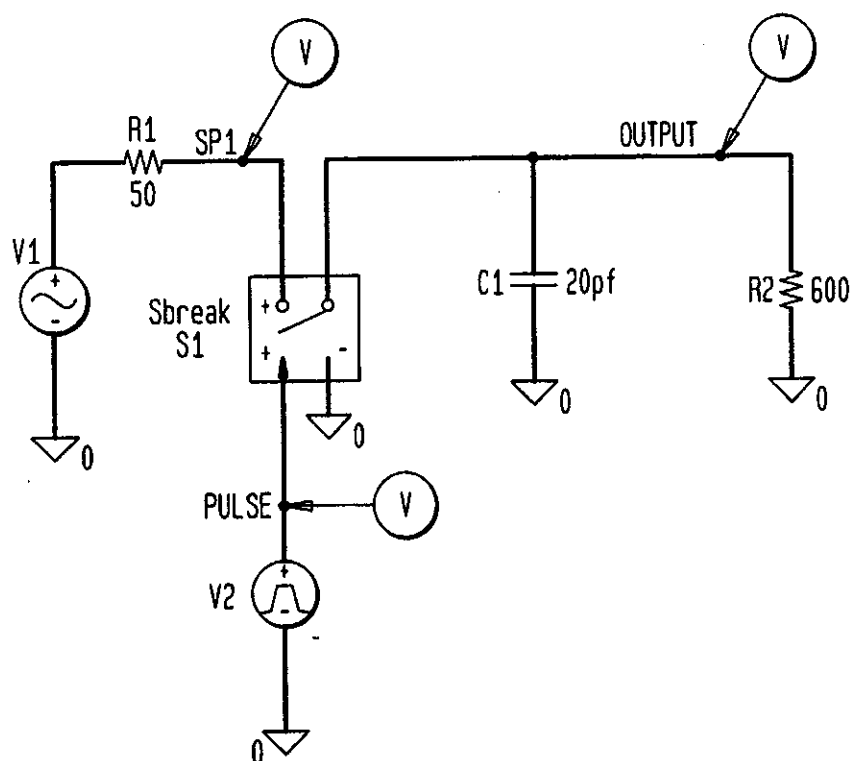
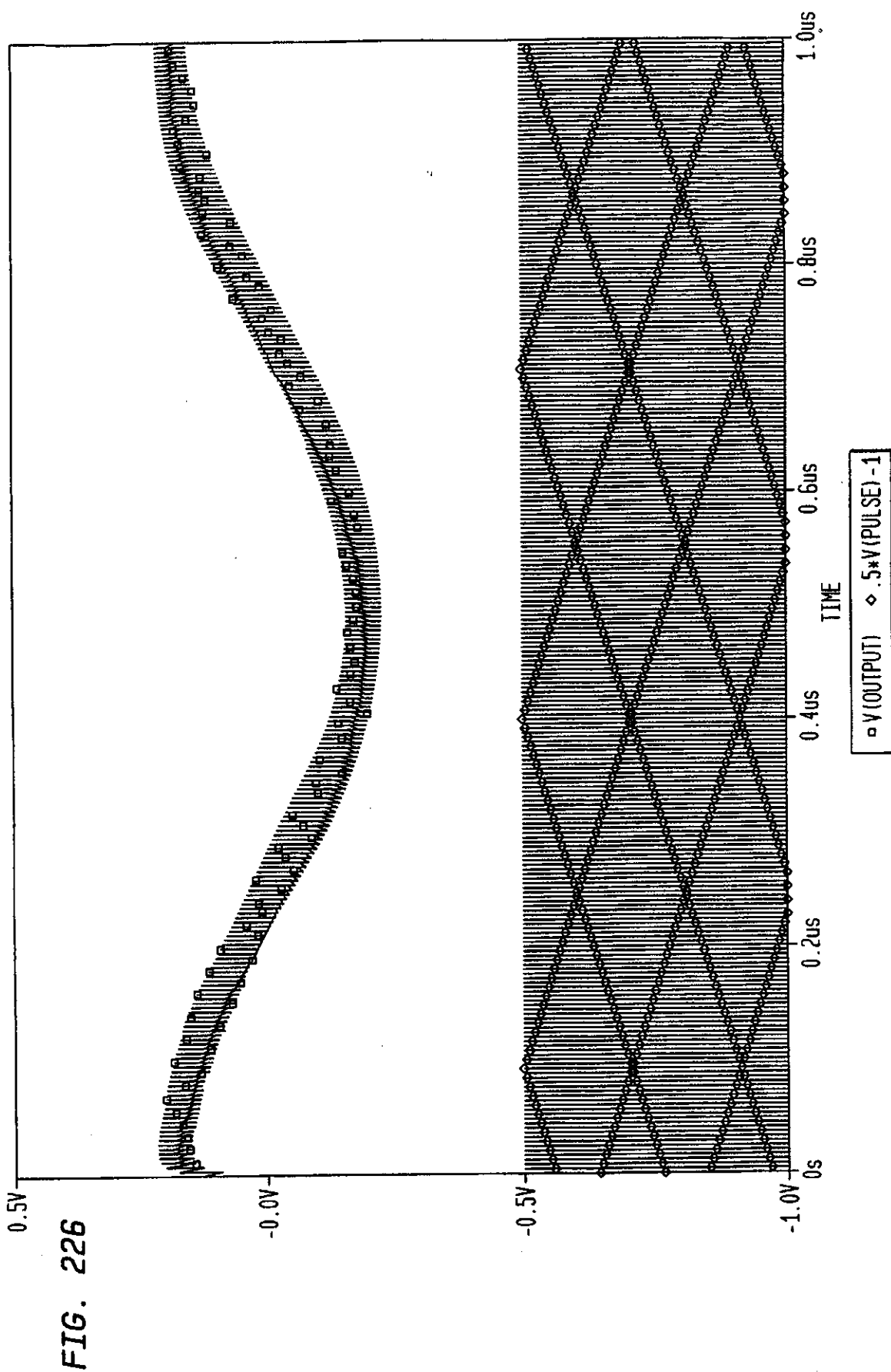


FIG. 225





236/283

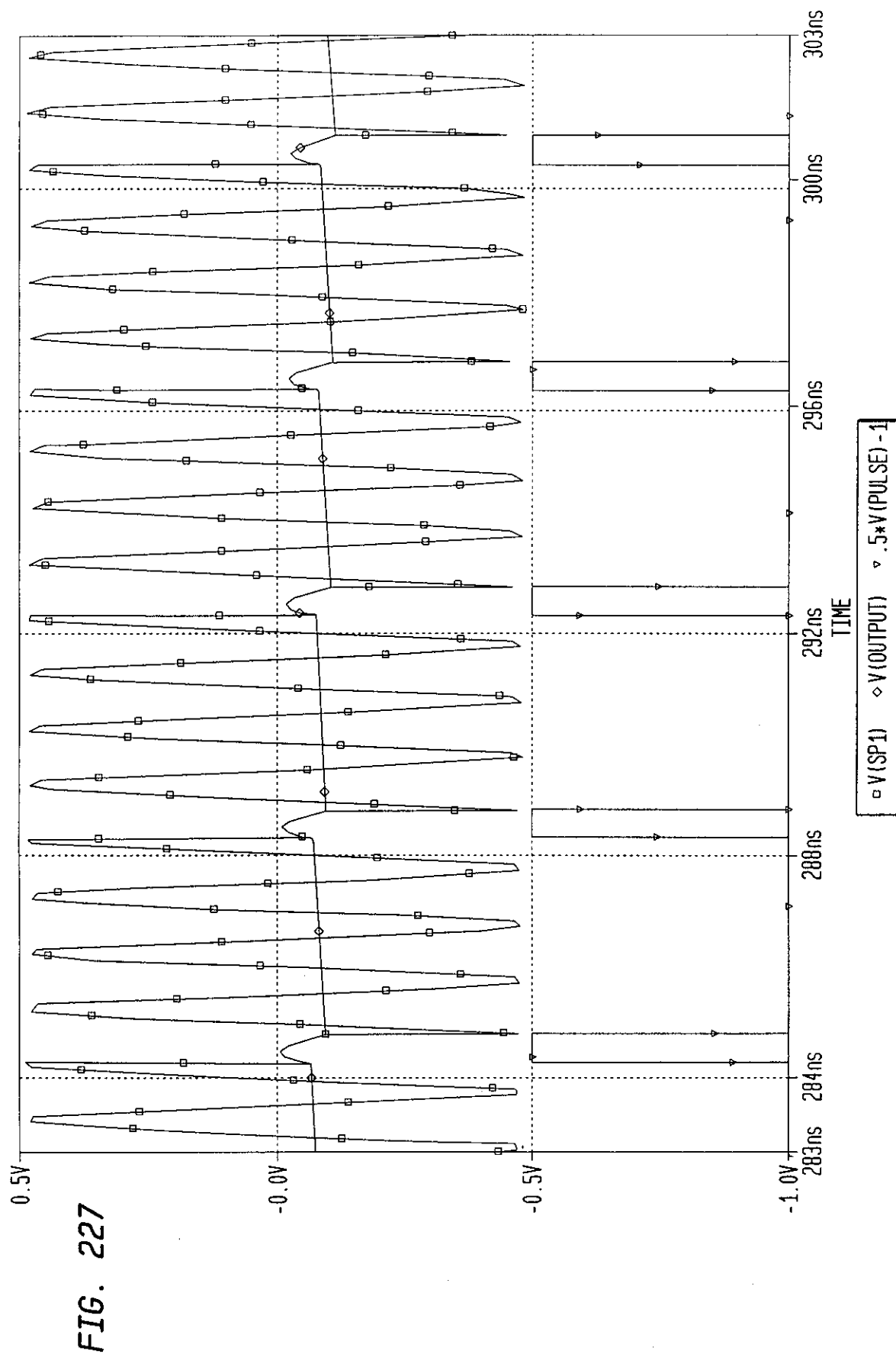


FIG. 228

CHARGE TRANSFER

DEFINITIONS:

q=CHARGE IN COULOMBS
C=CAPACITANCE IN FARADS
V=VOLTAGE IN VOLTS
A=INPUT SIGNAL AMPLITUDE

$$q=C \cdot V$$

$$V=A \cdot \sin(t)$$

$$q(t)=C \cdot A \cdot \sin(t)$$

$$\Delta q(t)=C \cdot A \cdot \sin(t)-C \cdot A \cdot \sin(t-T)$$

$$\Delta q(t)=C \cdot A \cdot (\sin(t)-\sin(t-T))$$

EQUATION A

$\Delta q(t)$ EXPRESSES THE CHANGE IN CHARGE ACROSS CAPACITOR C DURING APERTURE T. AS CAN BE SEEN, WHEN APERTURE T TENDS TOWARDS 0, $\Delta q(t)$ TENDS TOWARDS 0.

238/283

FIG. 229

USING THE SUM TO PRODUCT TRIGONOMETRIC IDENTITY,

$$\sin(\alpha) - \sin(\beta) = 2 \cdot \sin\left(\frac{\alpha - \beta}{2}\right) \cdot \cos\left(\frac{\alpha + \beta}{2}\right) \quad \text{IDENTITY 1}$$

EQUATION 1 CAN BE RE-WRITTEN AS:

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left[\frac{t - (t - T)}{2}\right] \cdot \cos\left[\frac{t + (t - T)}{2}\right]$$

$$\Delta q(t) = 2 \cdot C \cdot A \cdot \sin\left(\frac{1}{2} \cdot T\right) \cdot \cos\left(t - \frac{1}{2} \cdot T\right) \quad \text{EQUATION B}$$

THE $\sin$ TERM IN EQUATION B IS A FUNCTION OF APERTURE T ONLY. IT IS EASILY SEEN THAT $\Delta q(t)$ WILL OBTAIN A MAXIMUM VALUE WHEN T IS EQUAL TO AN ODD MULTIPLE OF π ; i.e., $\pi, 3\pi, 5\pi \dots$. THEREFORE, CAPACITOR C EXPERIENCES THE GREATEST CHANGE IN CHARGE WHEN THE APERTURE HAS A VALUE OF π OR A TIME INTERVAL REPRESENTATIVE OF 180 DEGREES OF THE INPUT SINUSOID. CONVERSELY, WHEN T IS EQUAL TO $2\pi, 4\pi, 6\pi \dots$ MINIMAL CHARGE IS TRANSFERRED.

239/283

FIG. 230

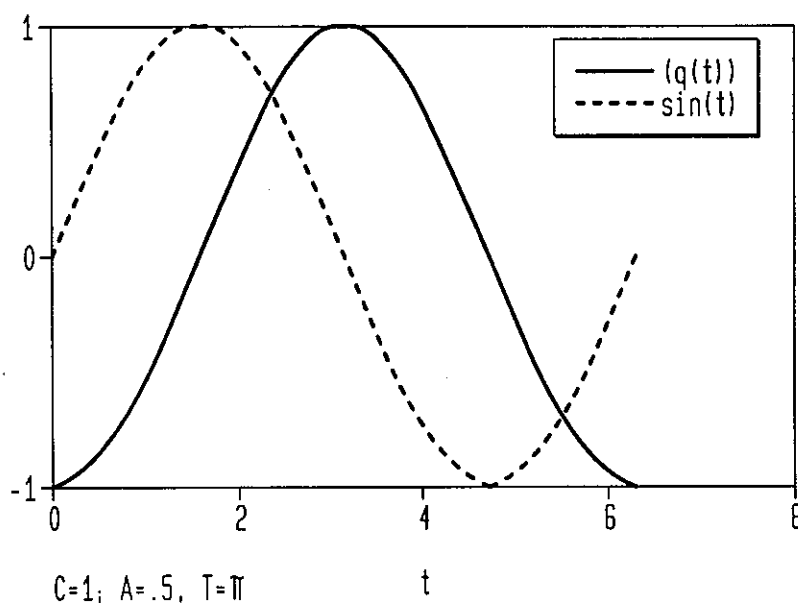
SOLVING FOR $q(t)$ BY INTEGRATING EQUATION A ALLOWS
THE CHARGE ON C WITH RESPECT TO TIME TO BE GRAPHED
ON THE SAME AXIS AS THE INPUT SINUSOID $\sin(t)$.

$$q(t) = \int C \cdot A \cdot (\sin(t) - \sin(t-T)) dt$$

$$q(t) = -\cos(t) \cdot C \cdot A + \cos(t-T) \cdot C \cdot A$$

$$q(t) = C \cdot A (\cos(t-T) - \cos(t)) \quad \text{EQUATION C}$$

FIG. 231



GRAPH 1

240/283

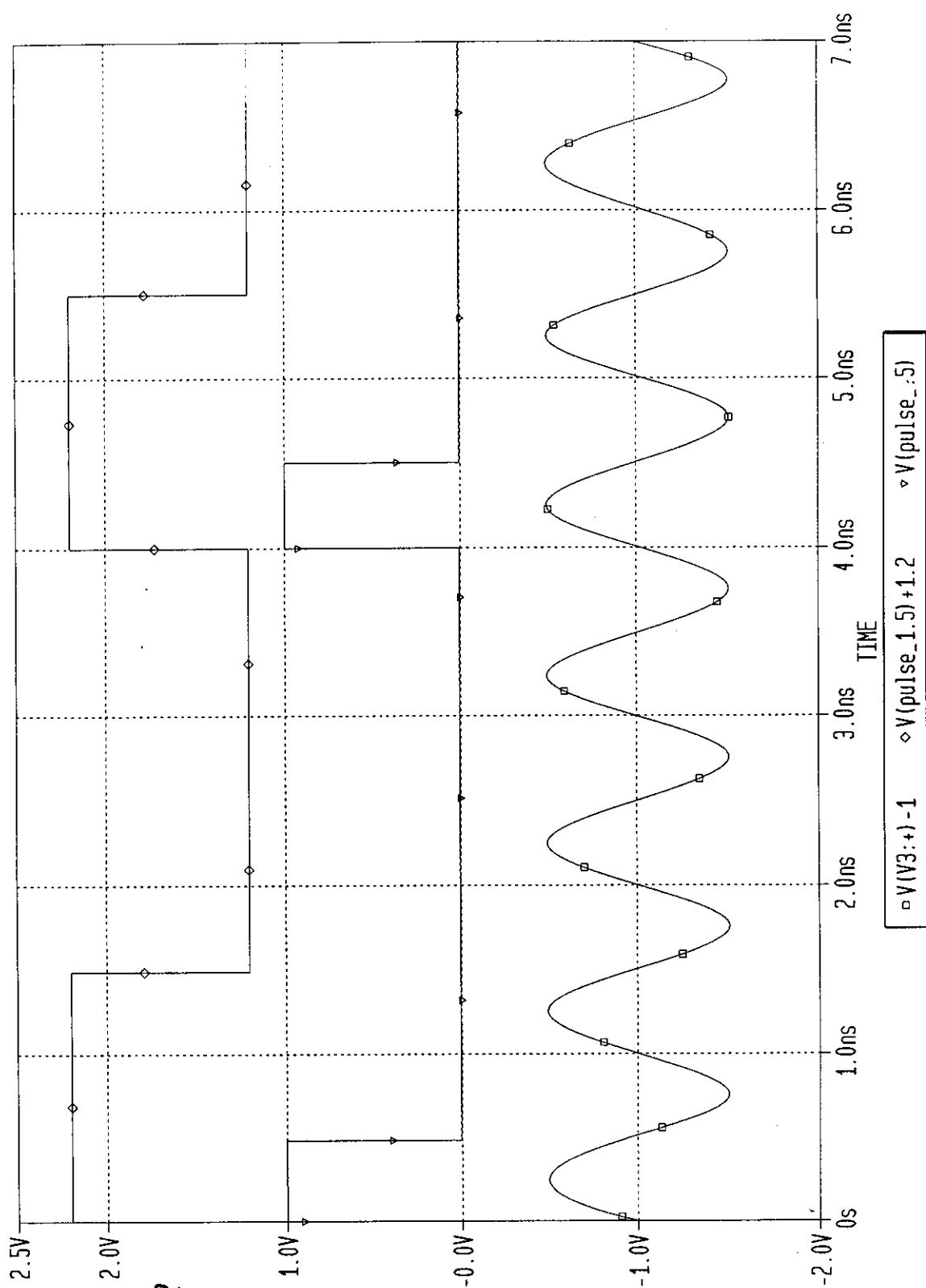
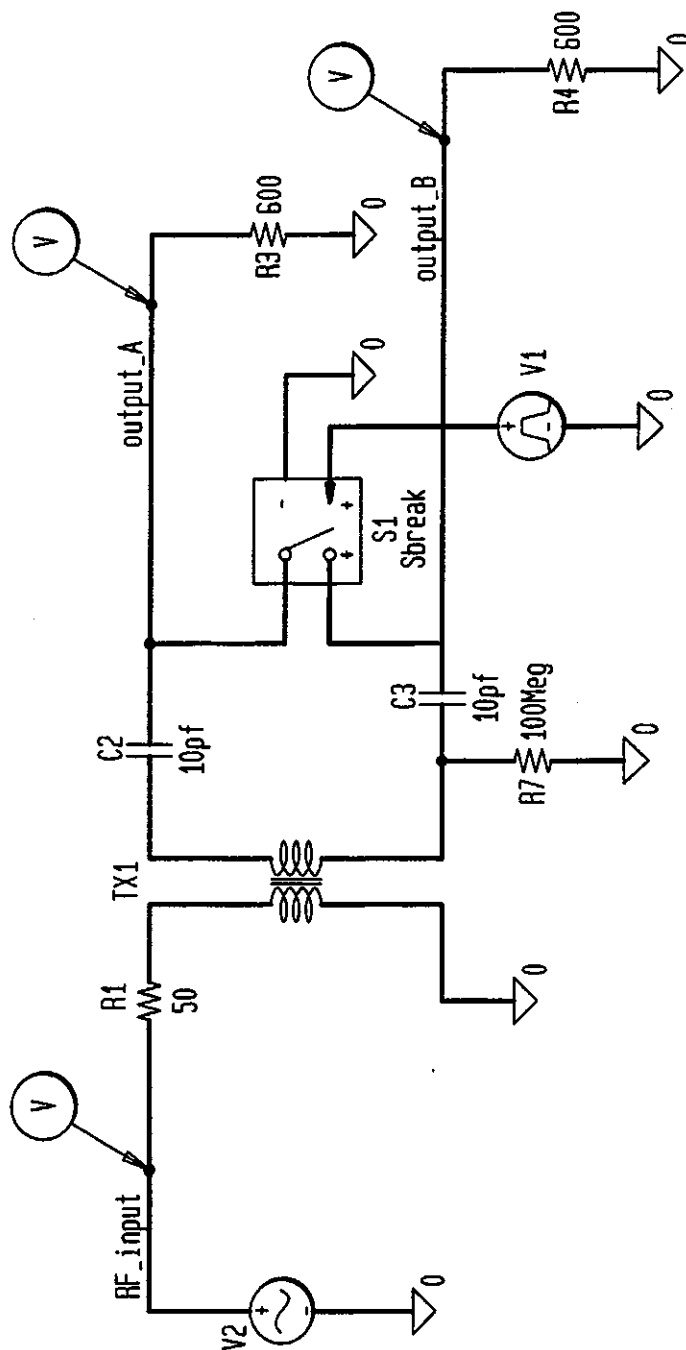
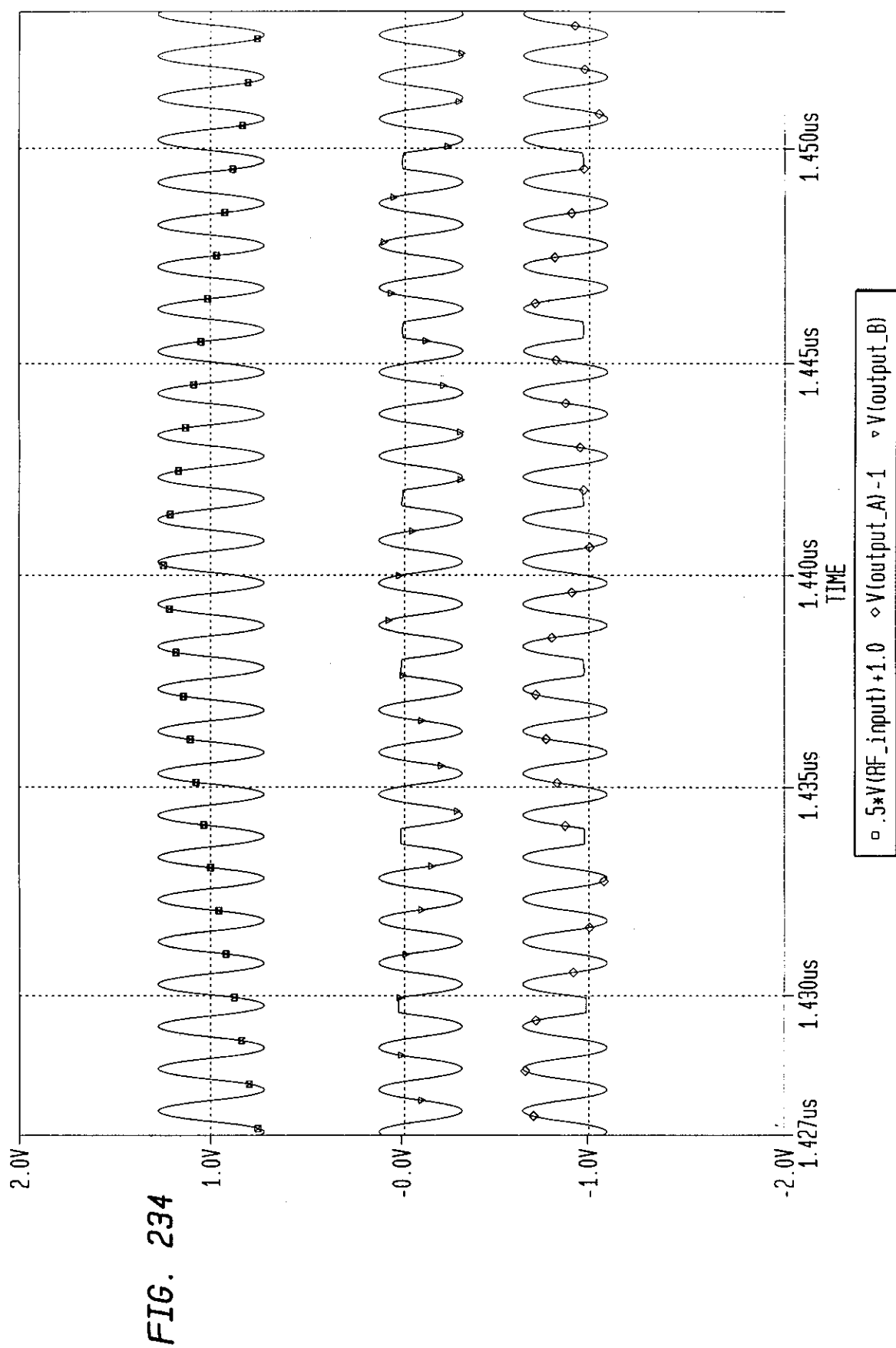


FIG. 233

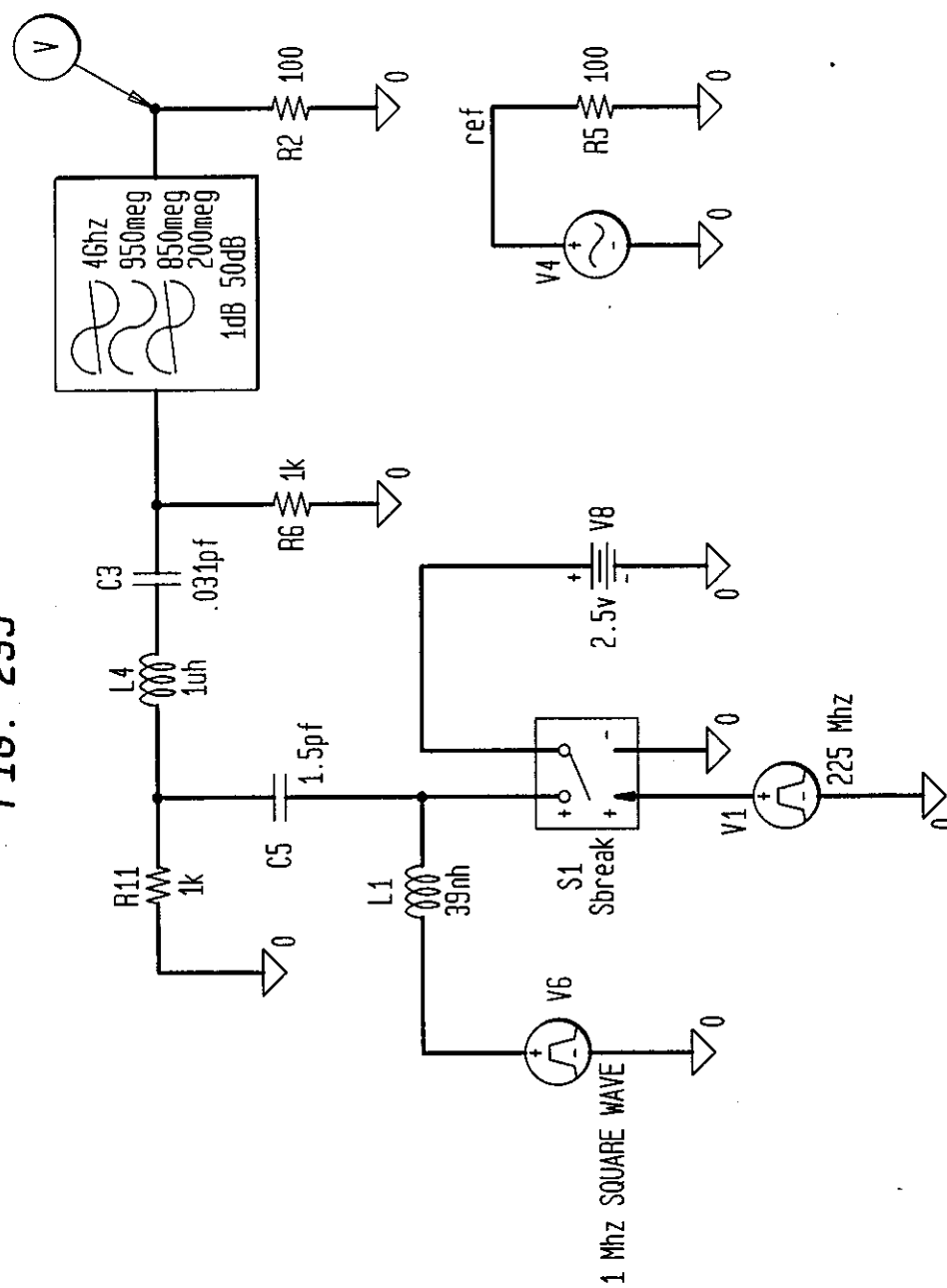


242/283

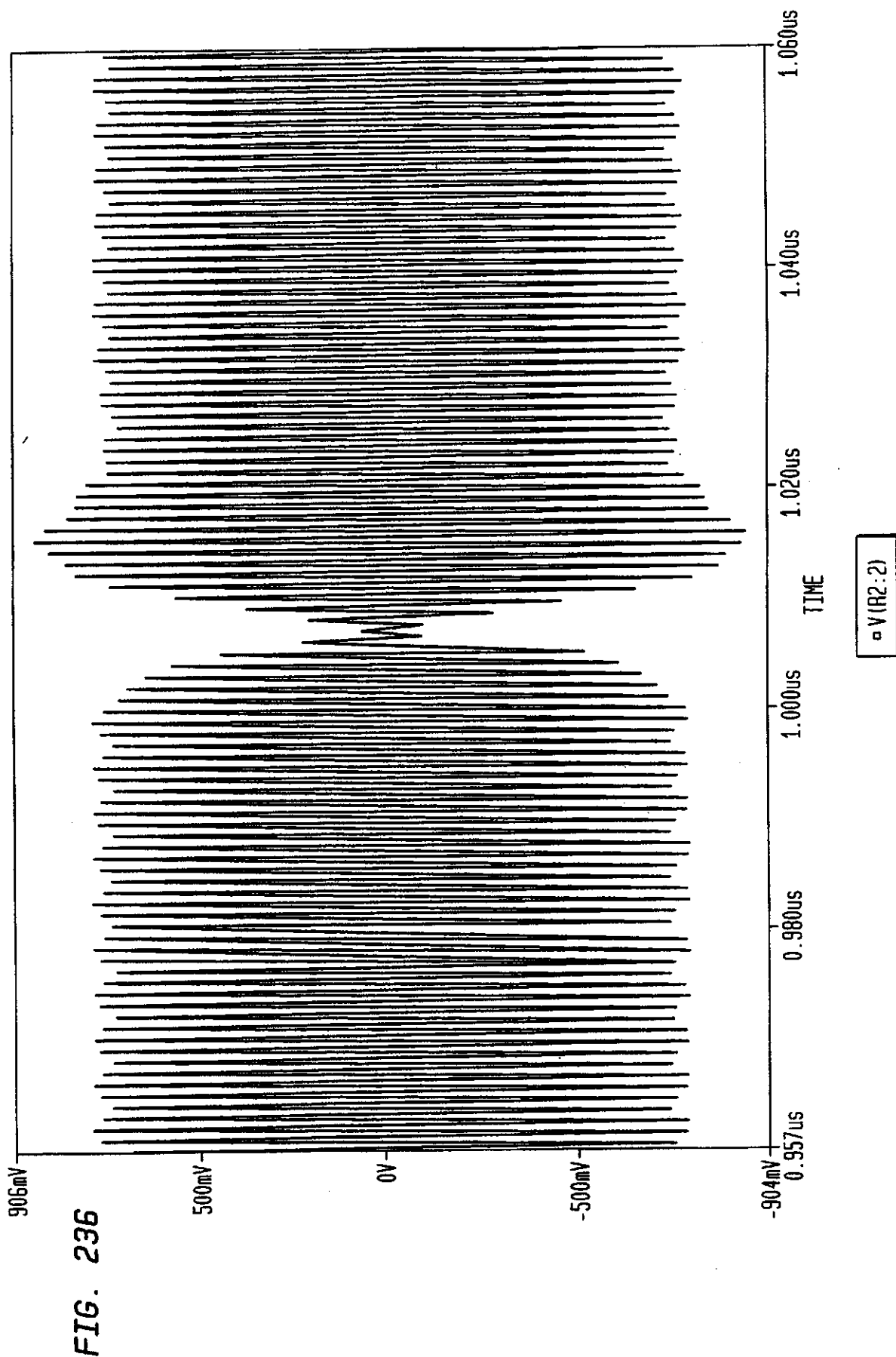


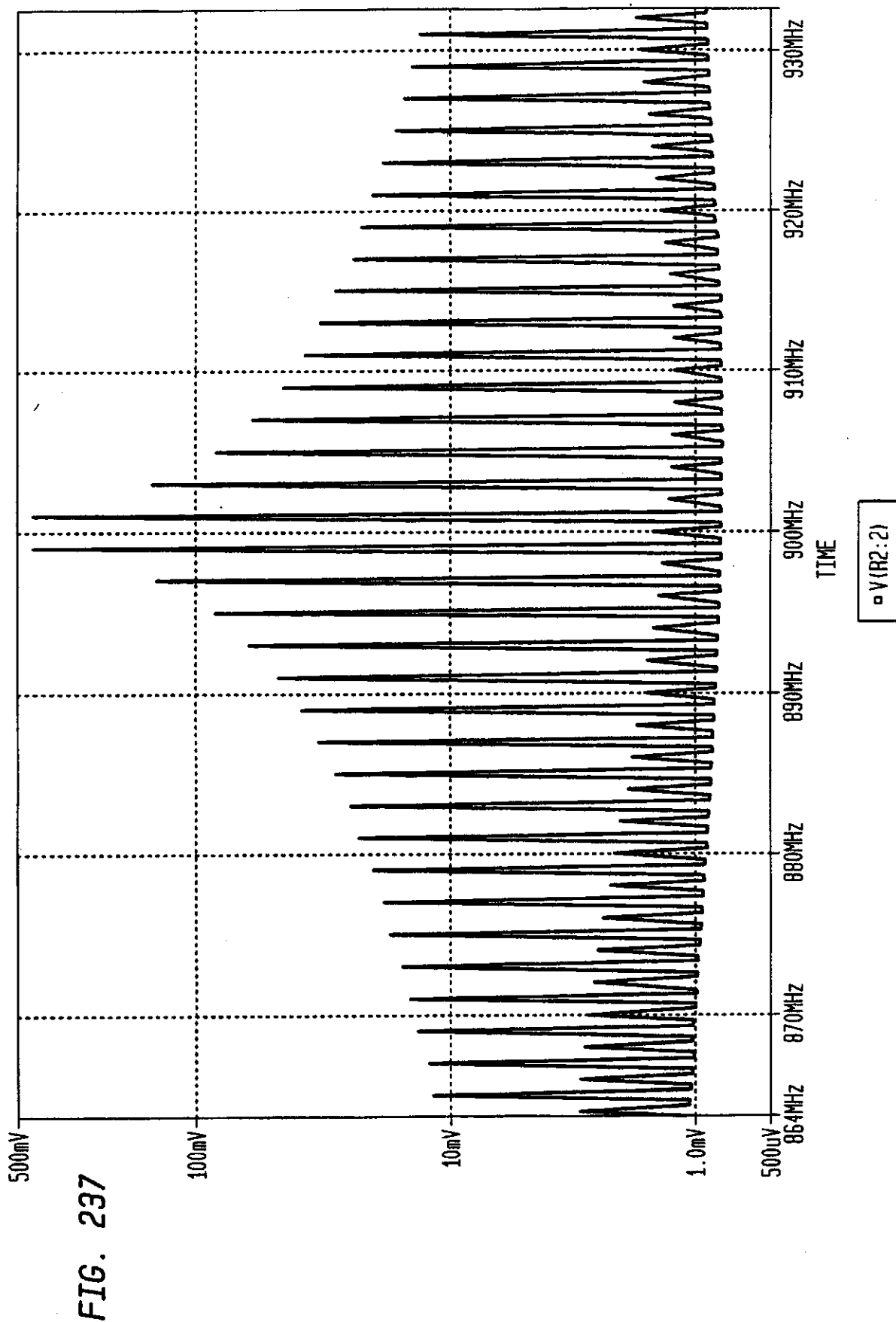
243/283

FIG. 235

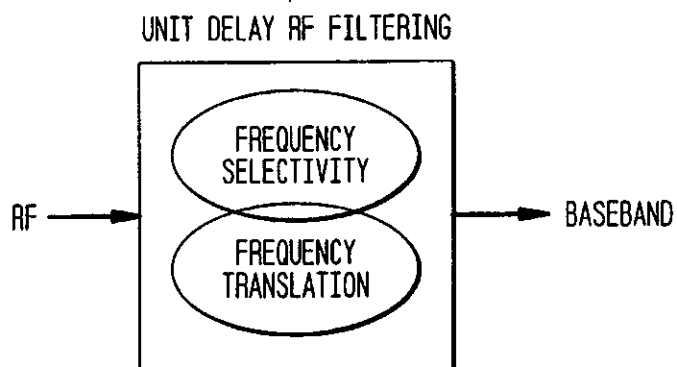
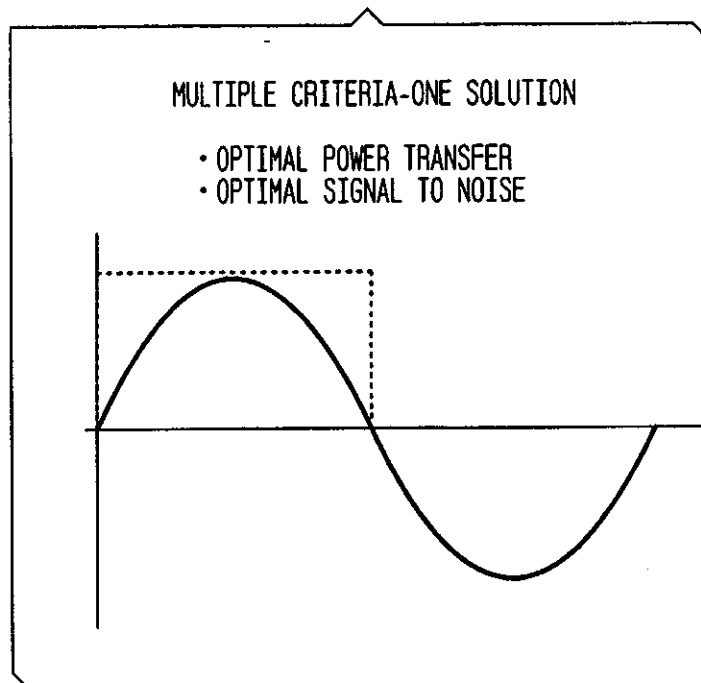


244/283





246/283

FIG. 238**FIG. 239**

247/283

FIG. 240

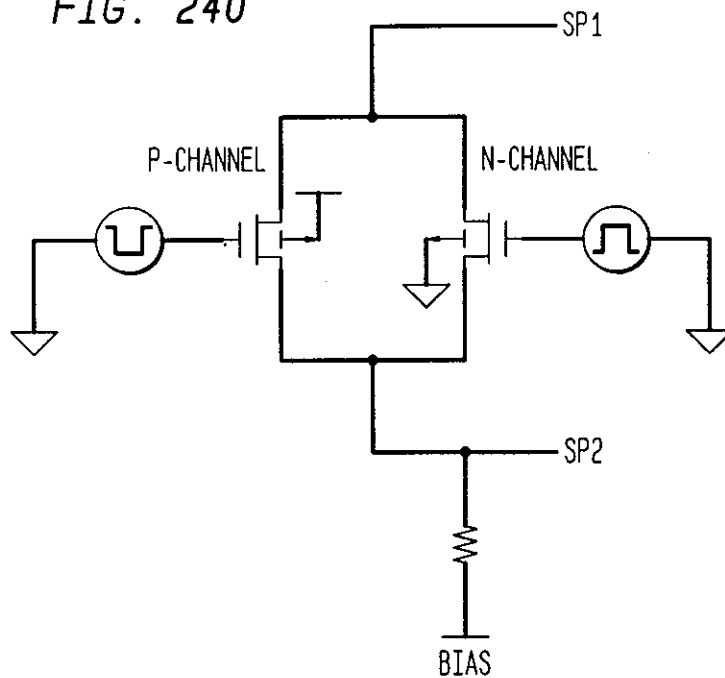


FIG. 241

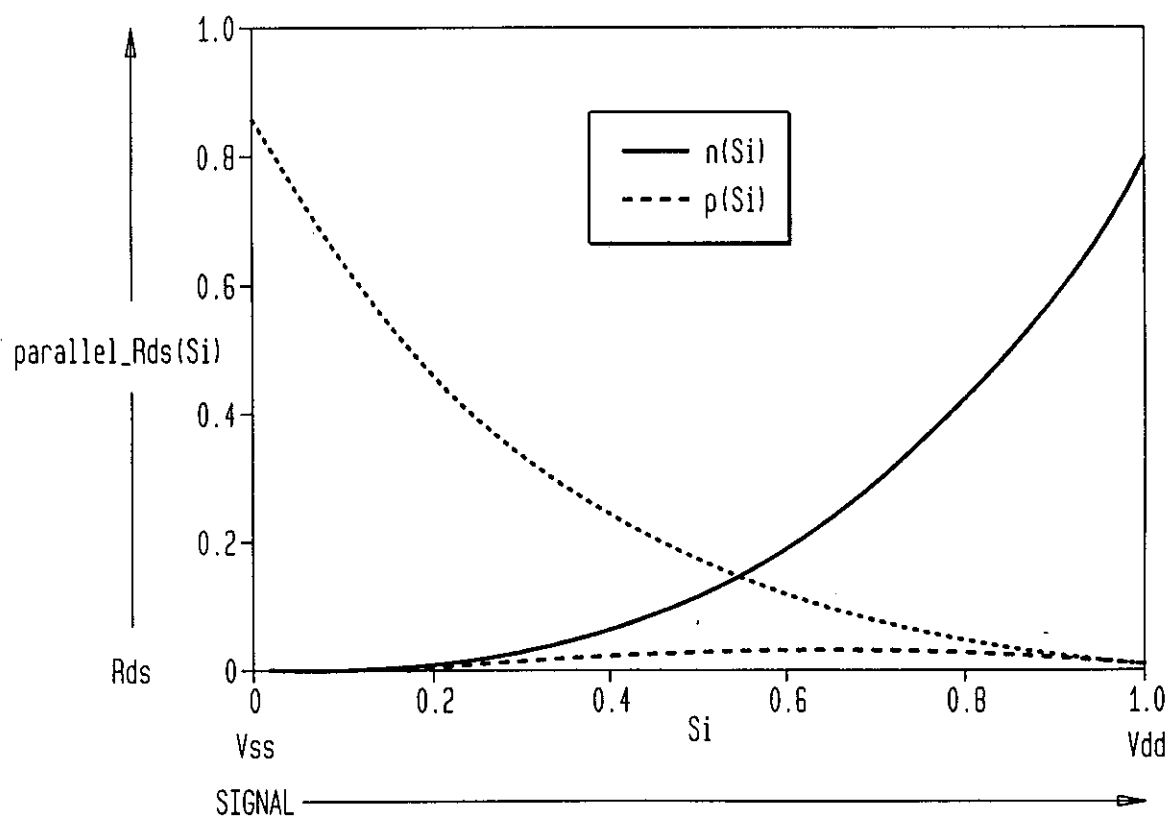
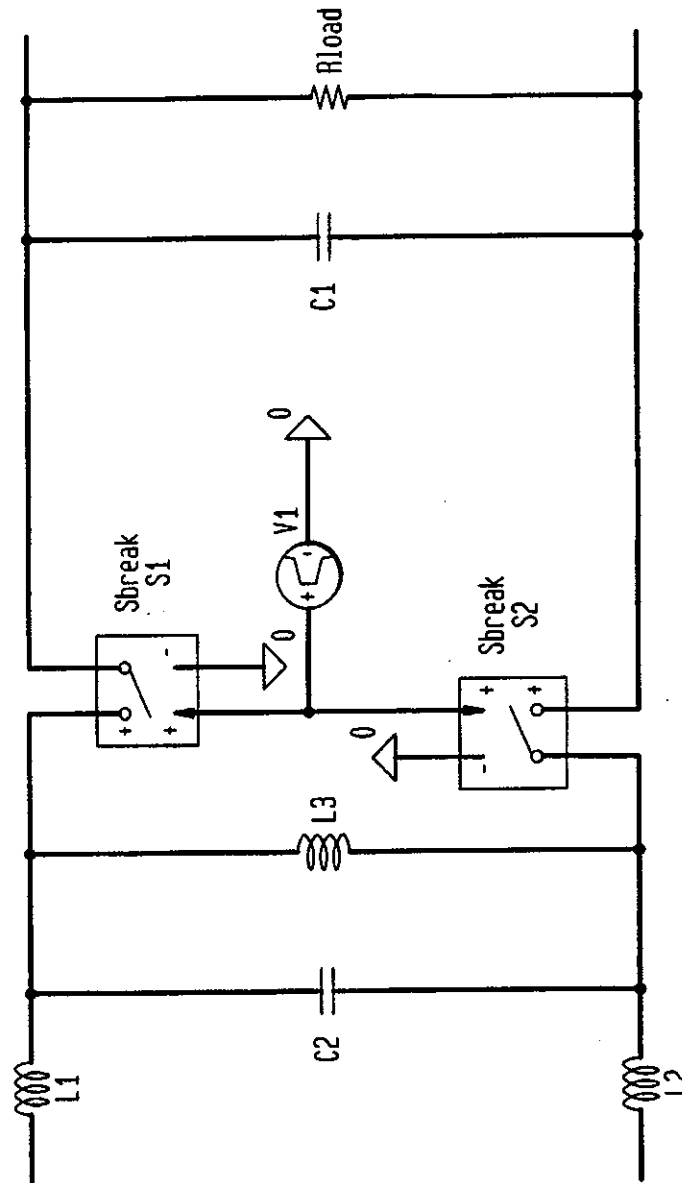


FIG. 242
DIFFERENTIAL CONFIGURATION



249/283

FIG. 243
UFD CLOCK SPREADING

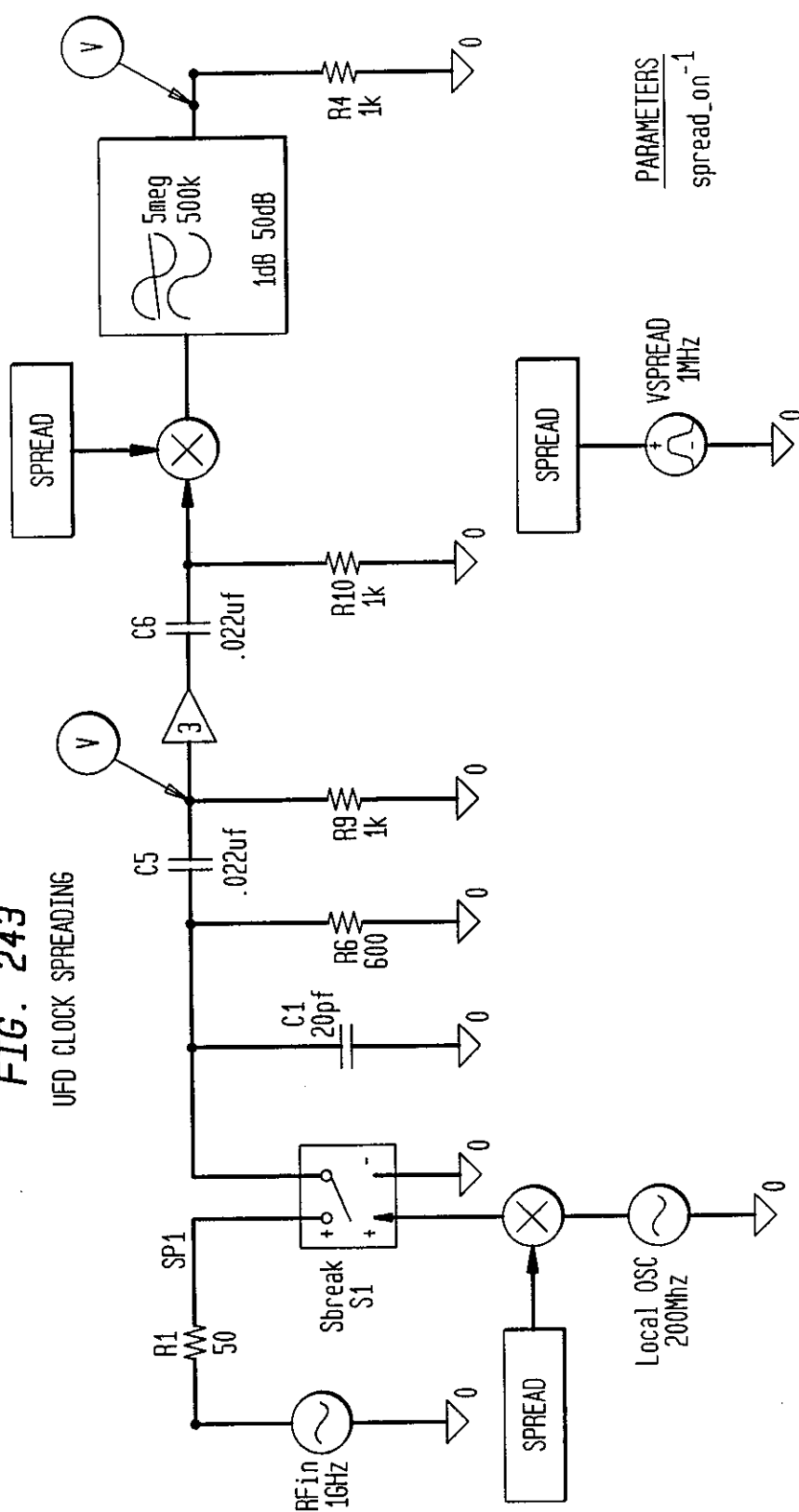


FIG. 244

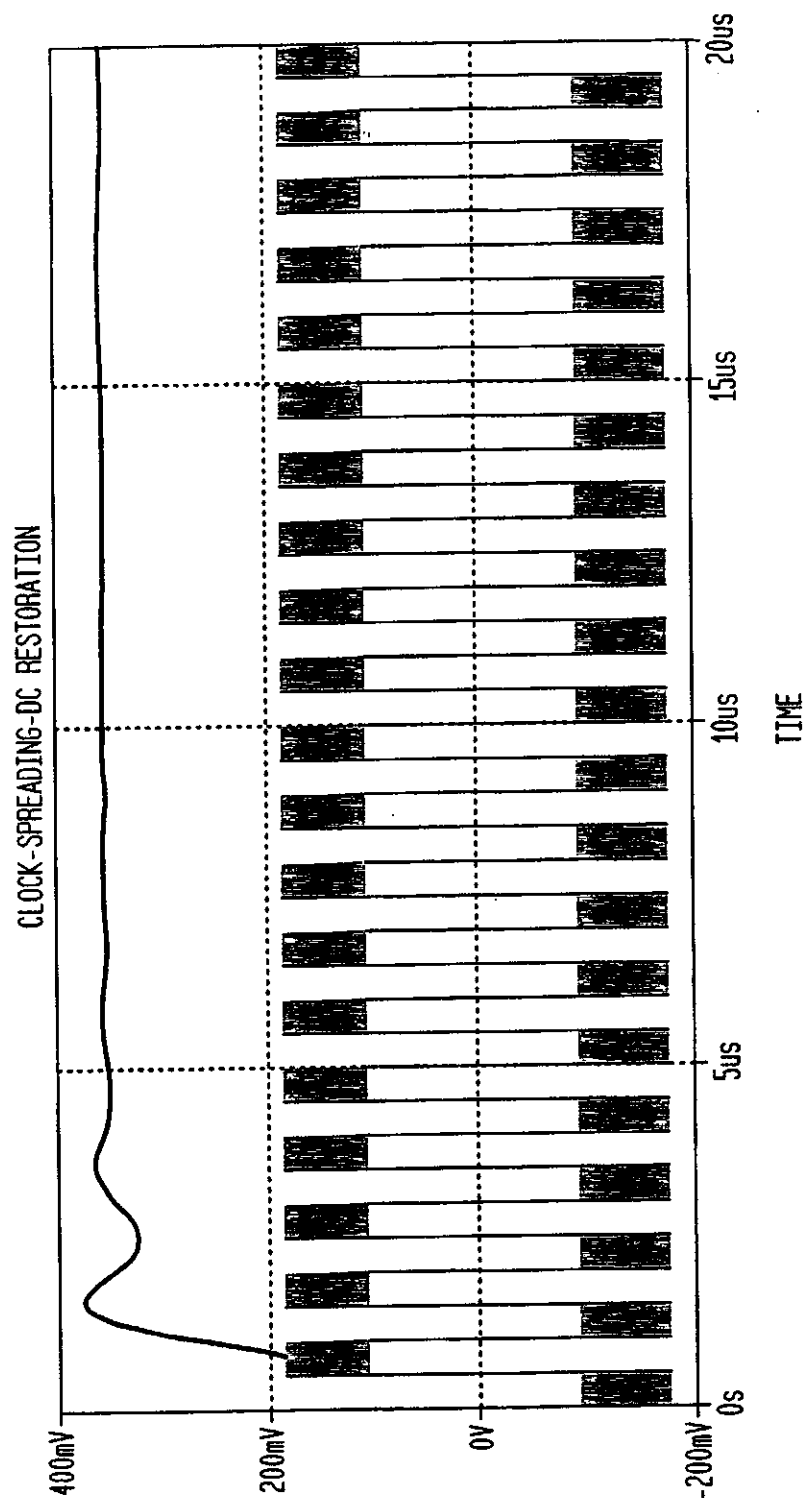
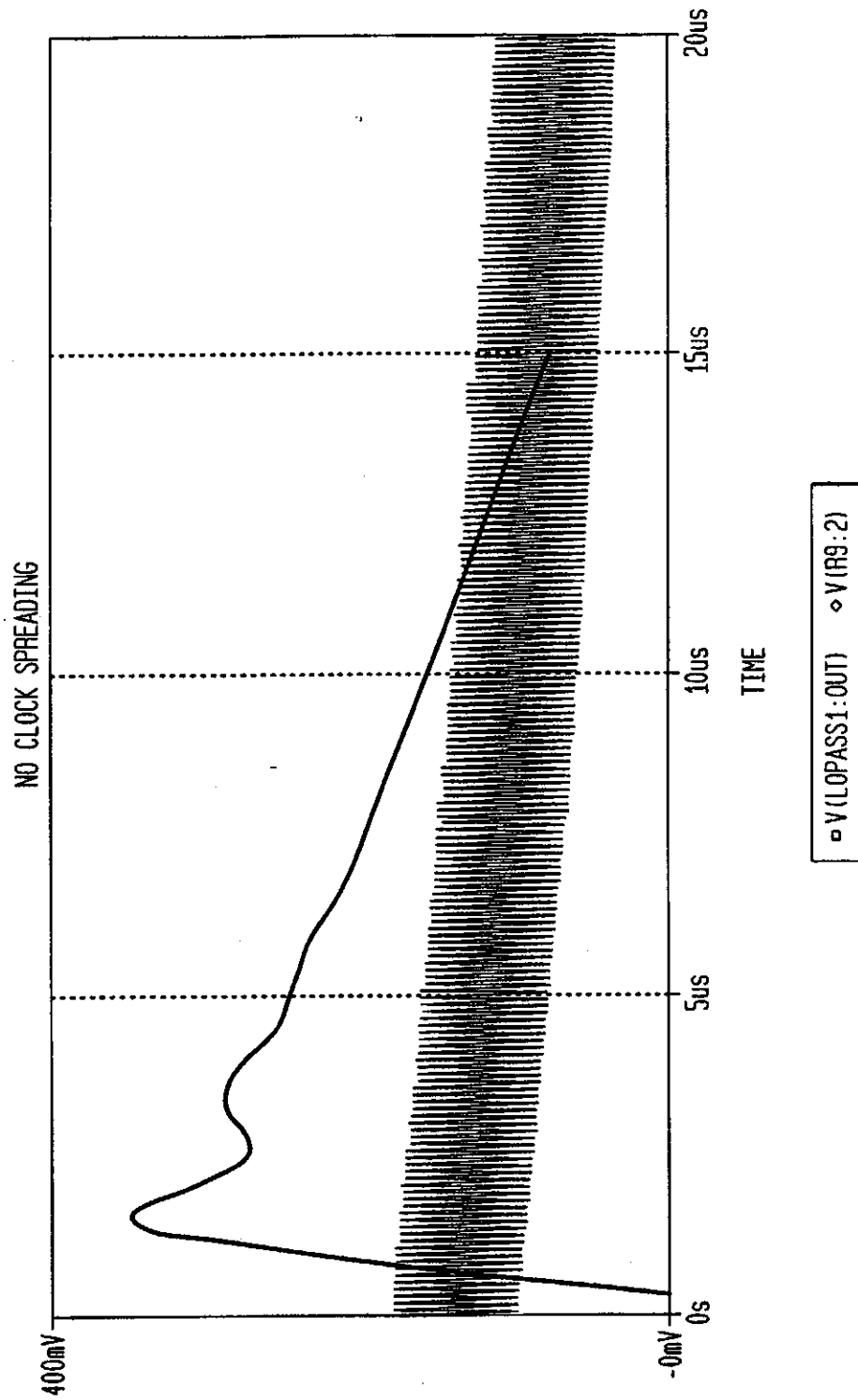
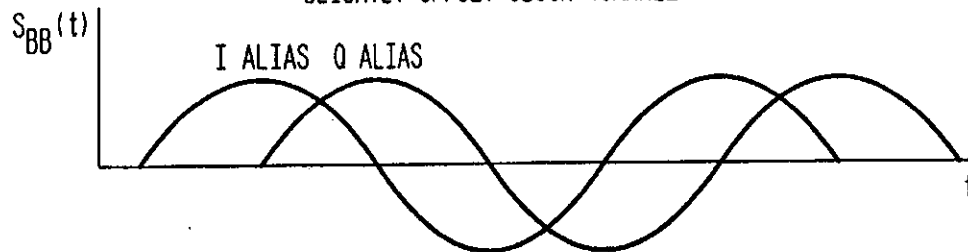


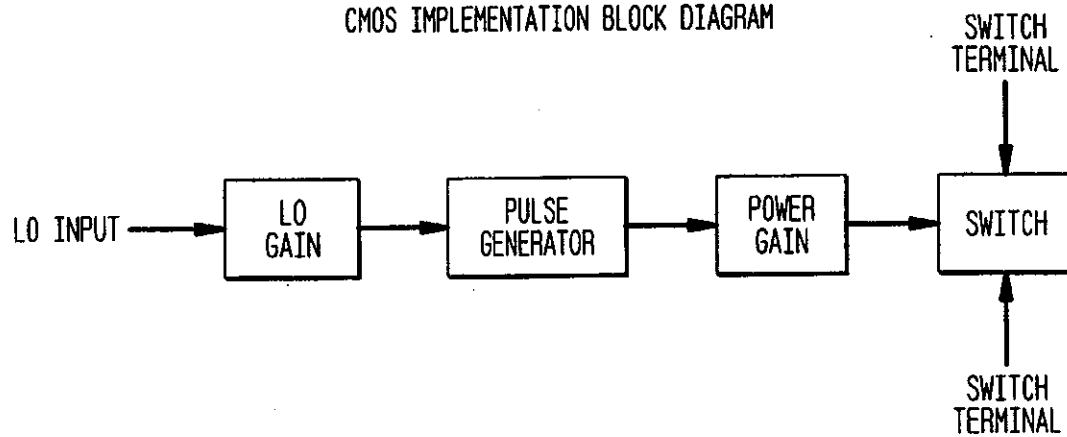
FIG. 245



252/283

FIG. 246B.B. RECOVERED I/Q WAVEFORMS WITH
SLIGHTLY OFFSET CLOCK (CARRIER)**FIG. 247**

CMOS IMPLEMENTATION BLOCK DIAGRAM

**FIG. 248**

LO GAIN BLOCK AT GATE LEVEL

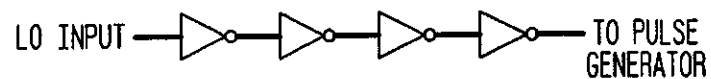
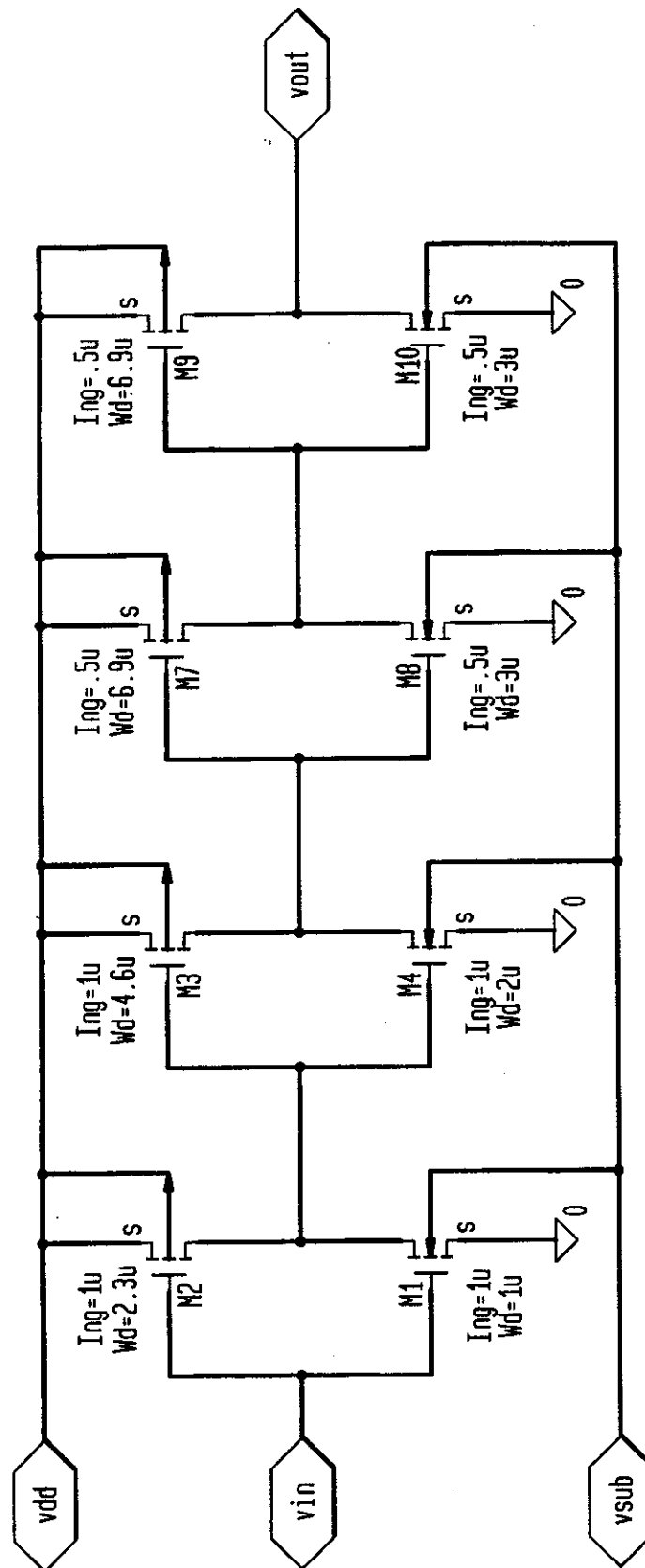


FIG. 249

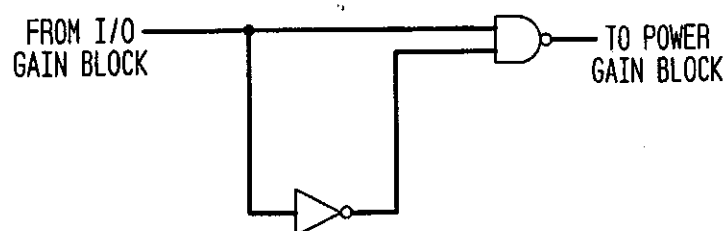
LO GAIN BLOCK AT TRANSISTOR LEVEL



254/283

FIG. 250

PULSE GENERATOR#1 AT GATE LEVEL

**FIG. 251**

PULSE GENERATOR#1 AT TRANSISTOR LEVEL

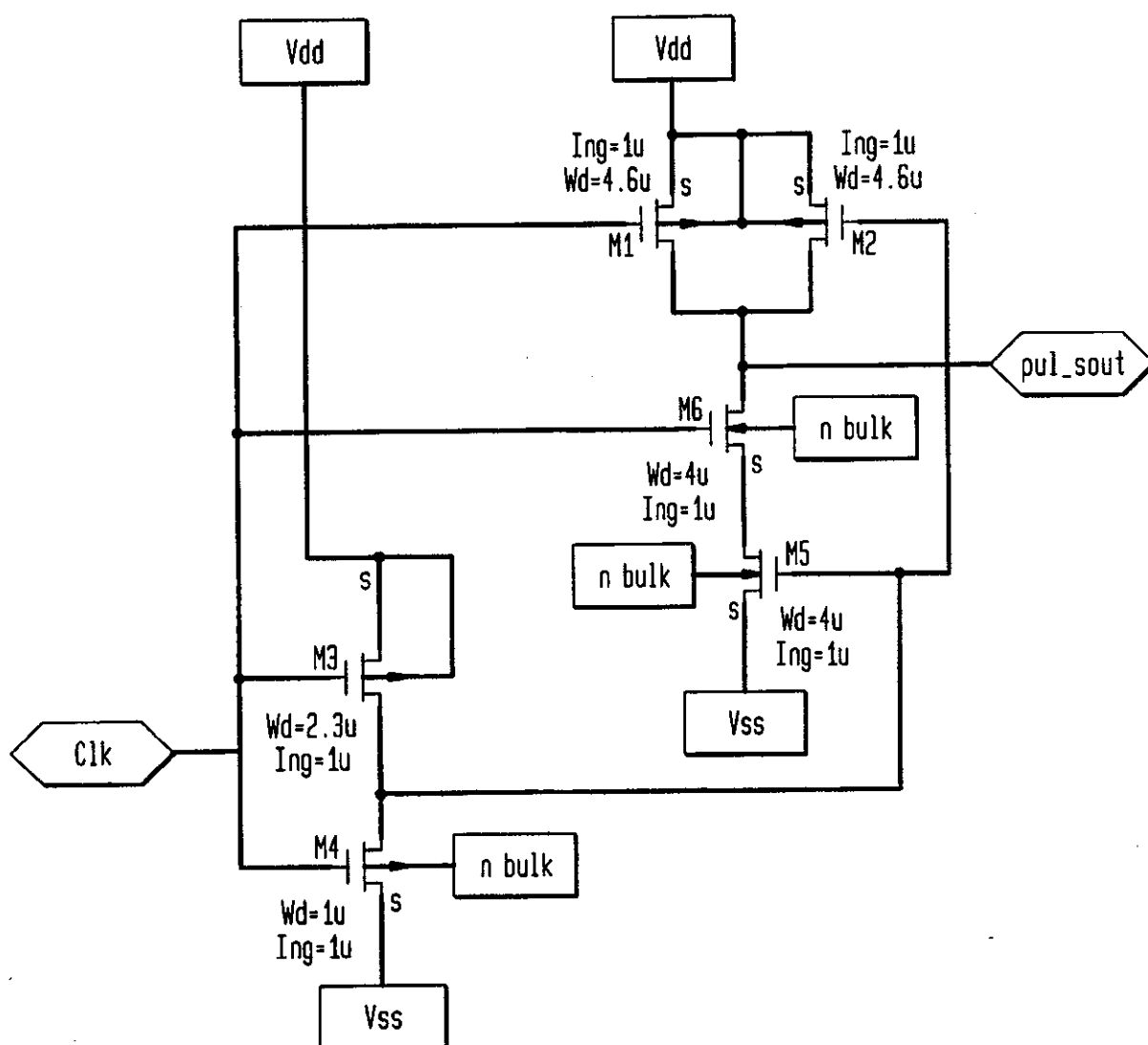


FIG. 252

POWER GAIN BLOCK AT GATE LEVEL

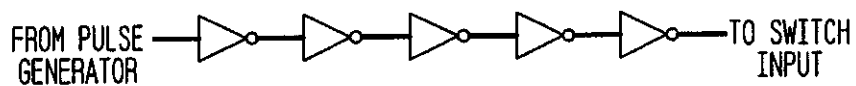
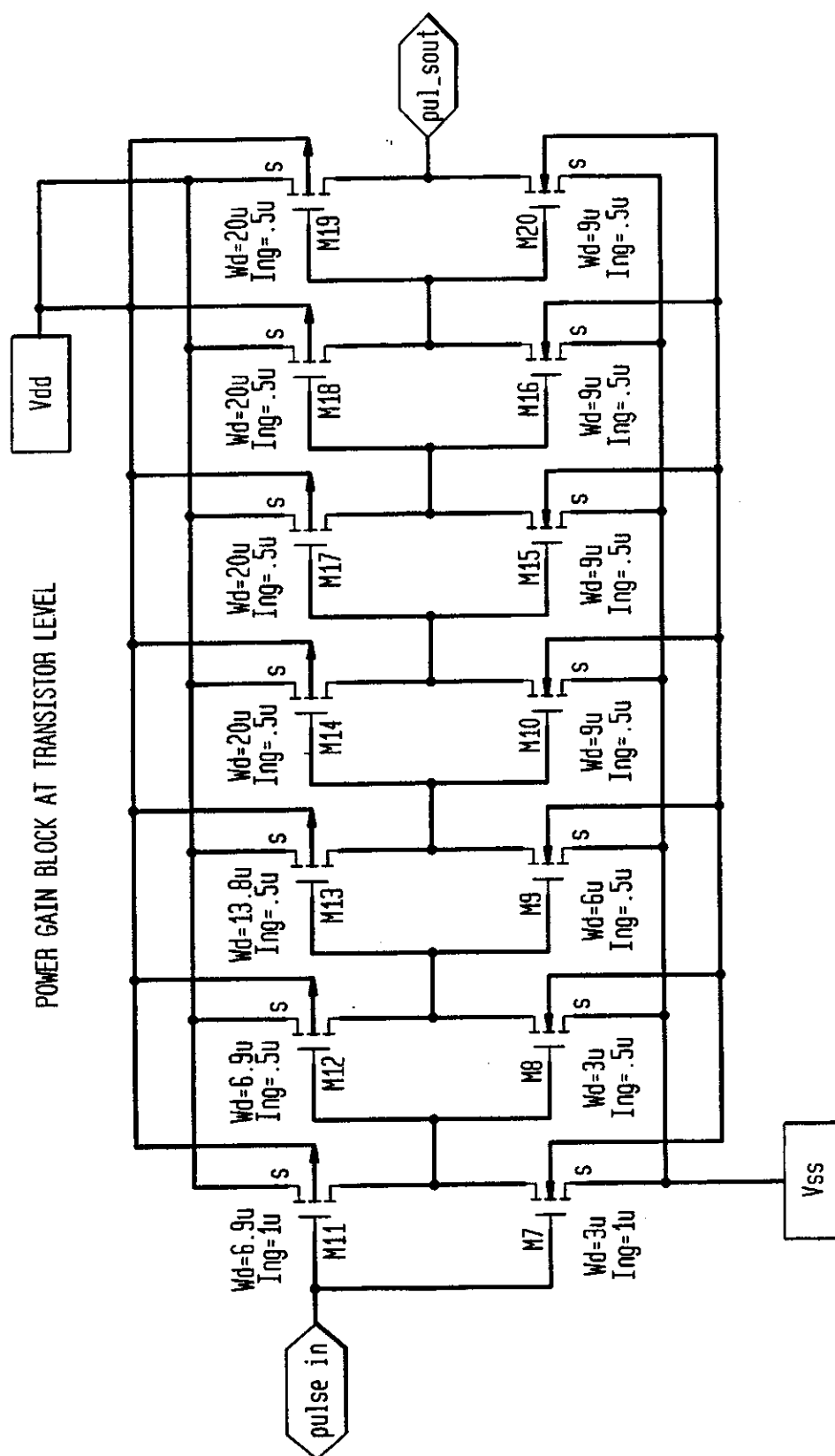


FIG. 253



257/283

FIG. 254

SWITCH AT TRANSISTOR LEVEL

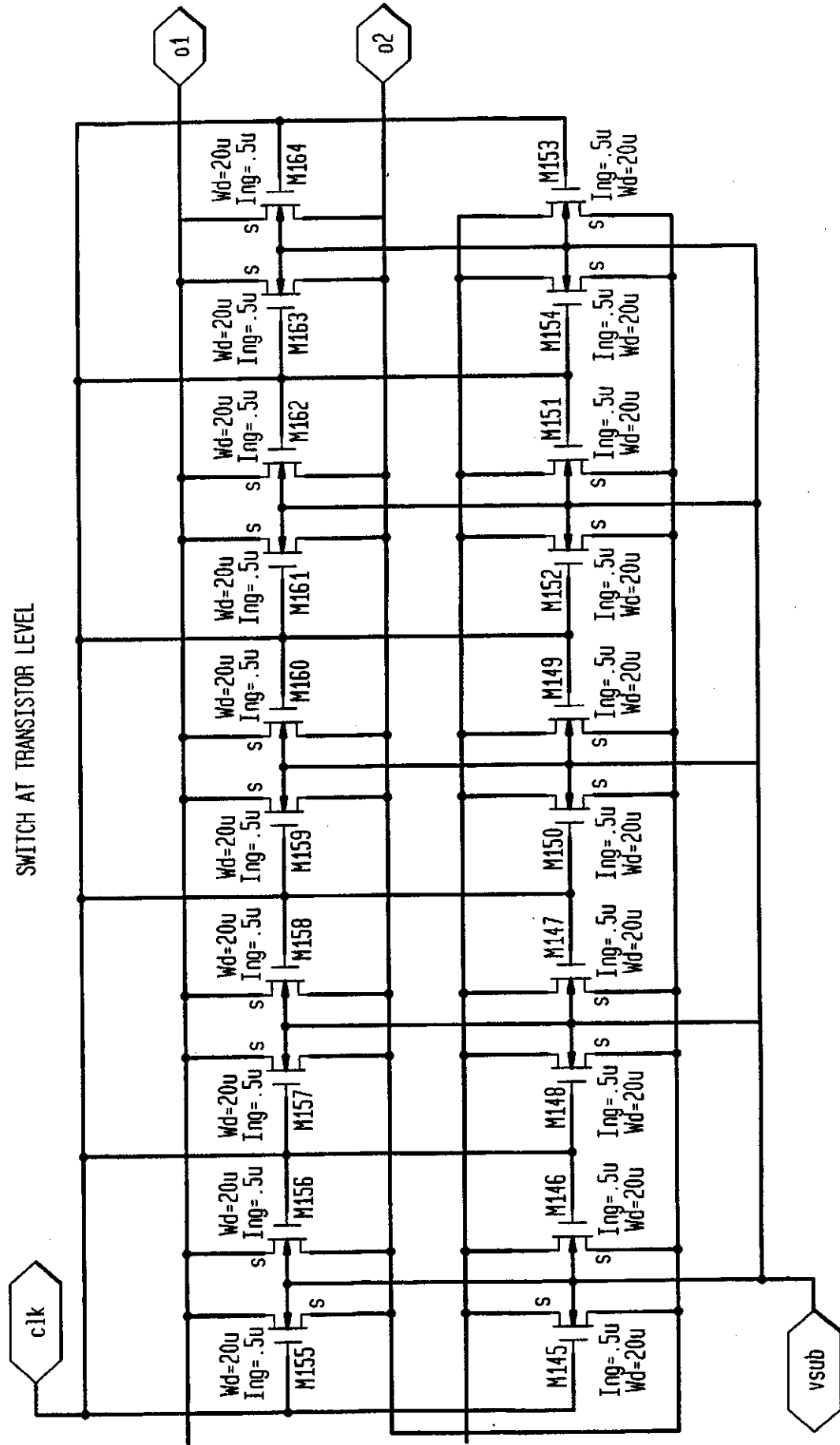


FIG. 255

CMOS "HOT CLOCK" BLOCK DIAGRAM

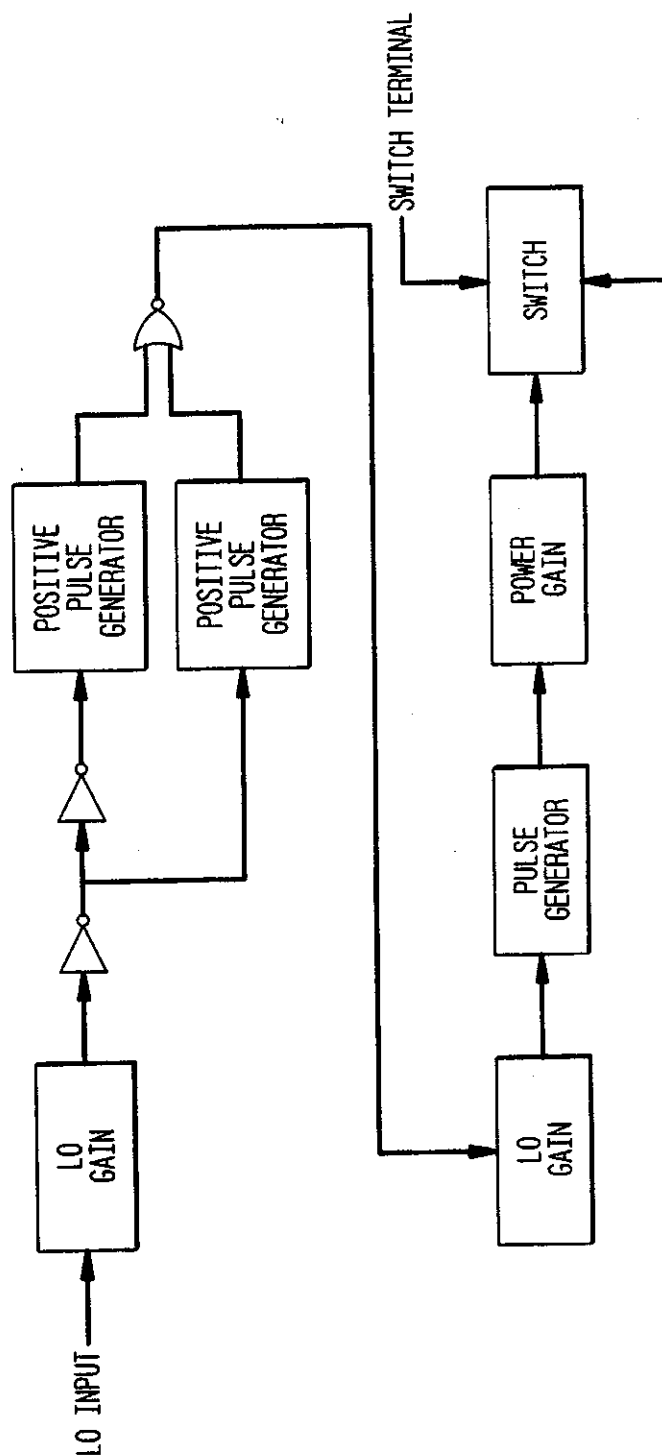
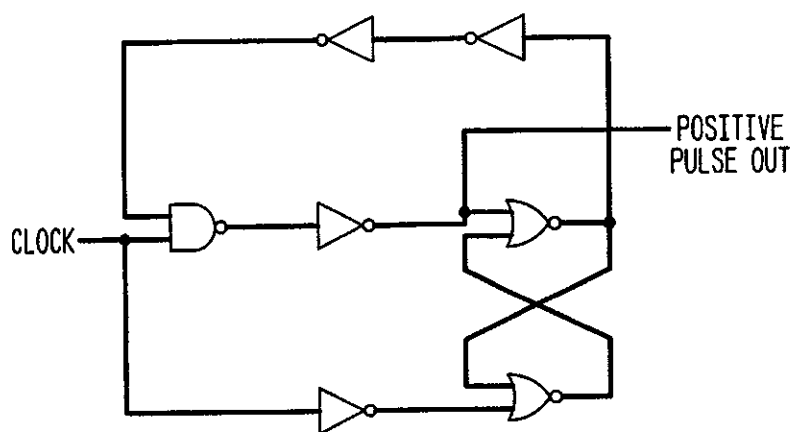


FIG. 256

POSITIVE PULSE GENERATOR AT GATE LEVEL



260/283

FIG. 257
POSITIVE PULSER AT TRANSISTOR LEVEL

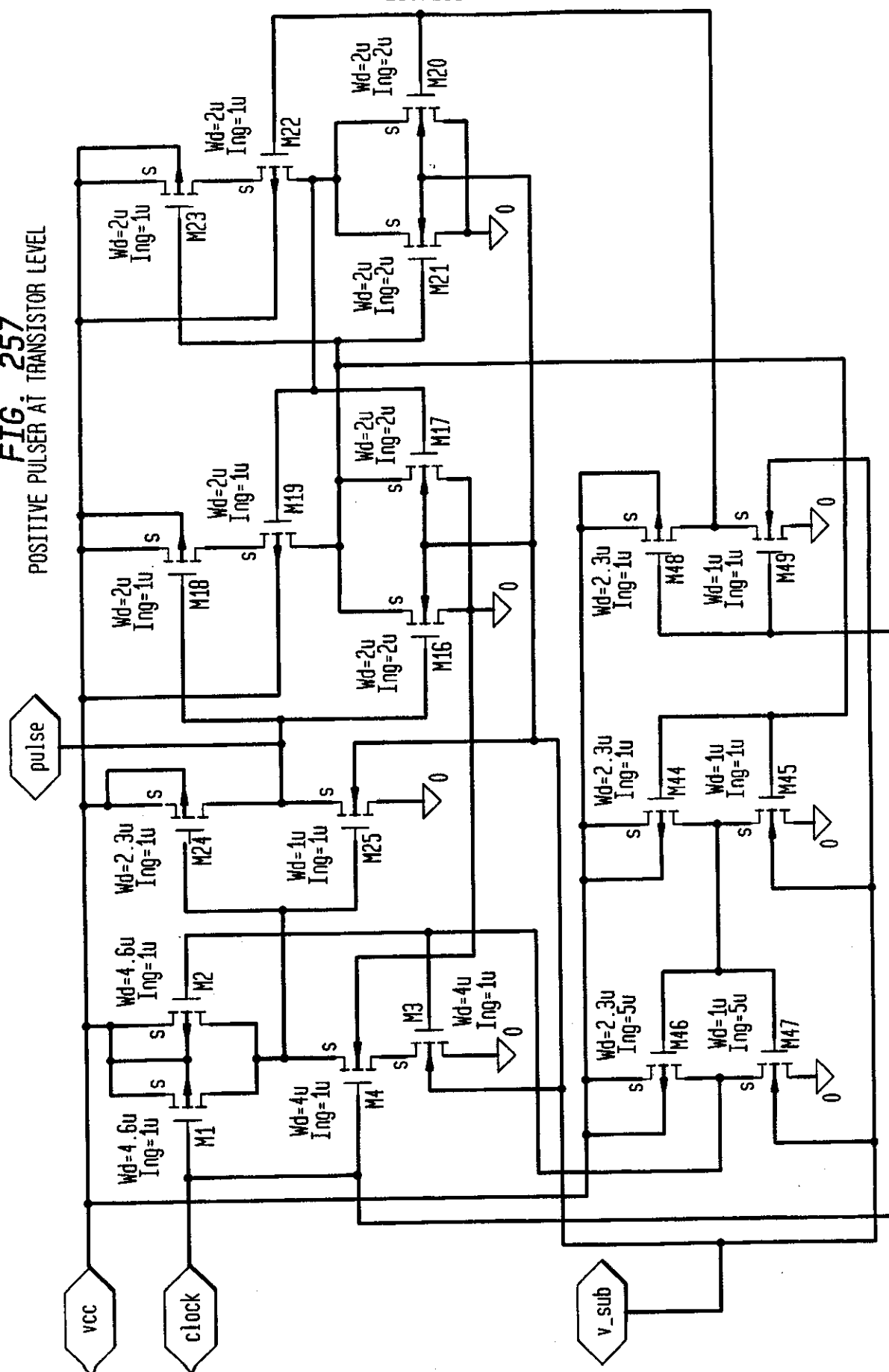
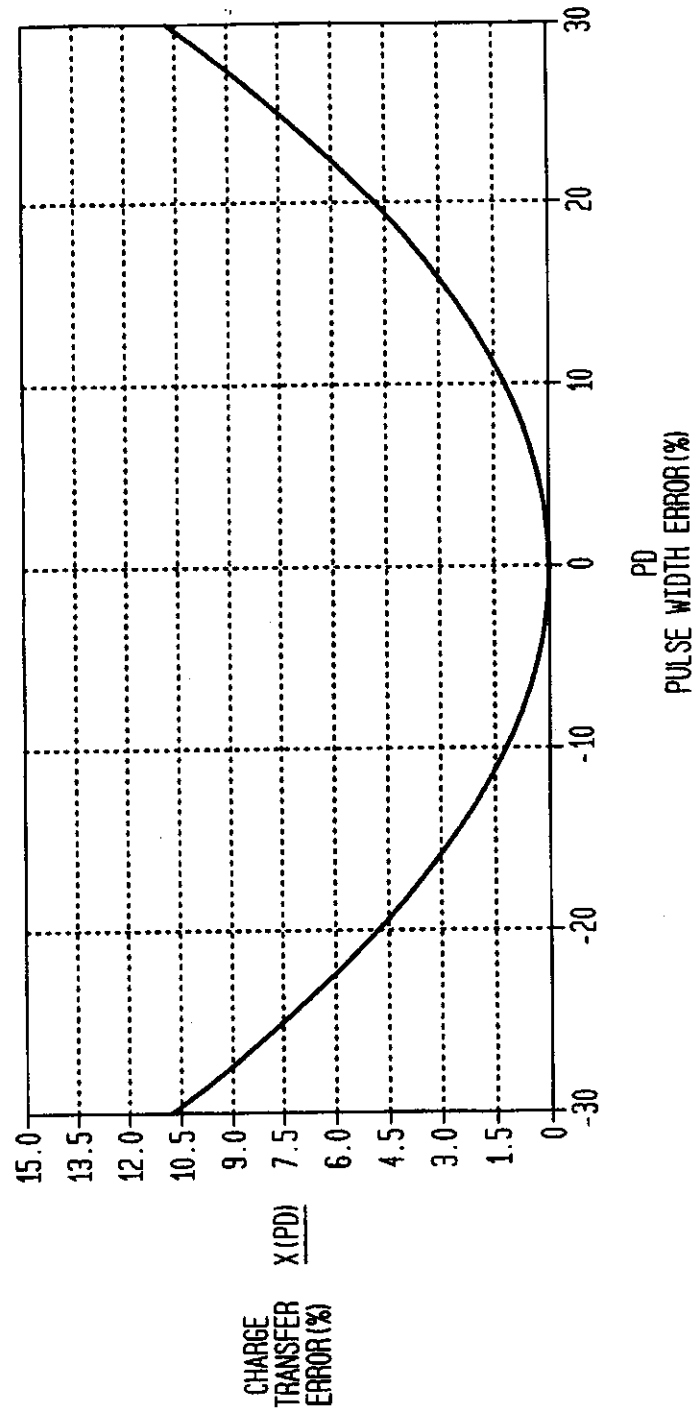


FIG. 258

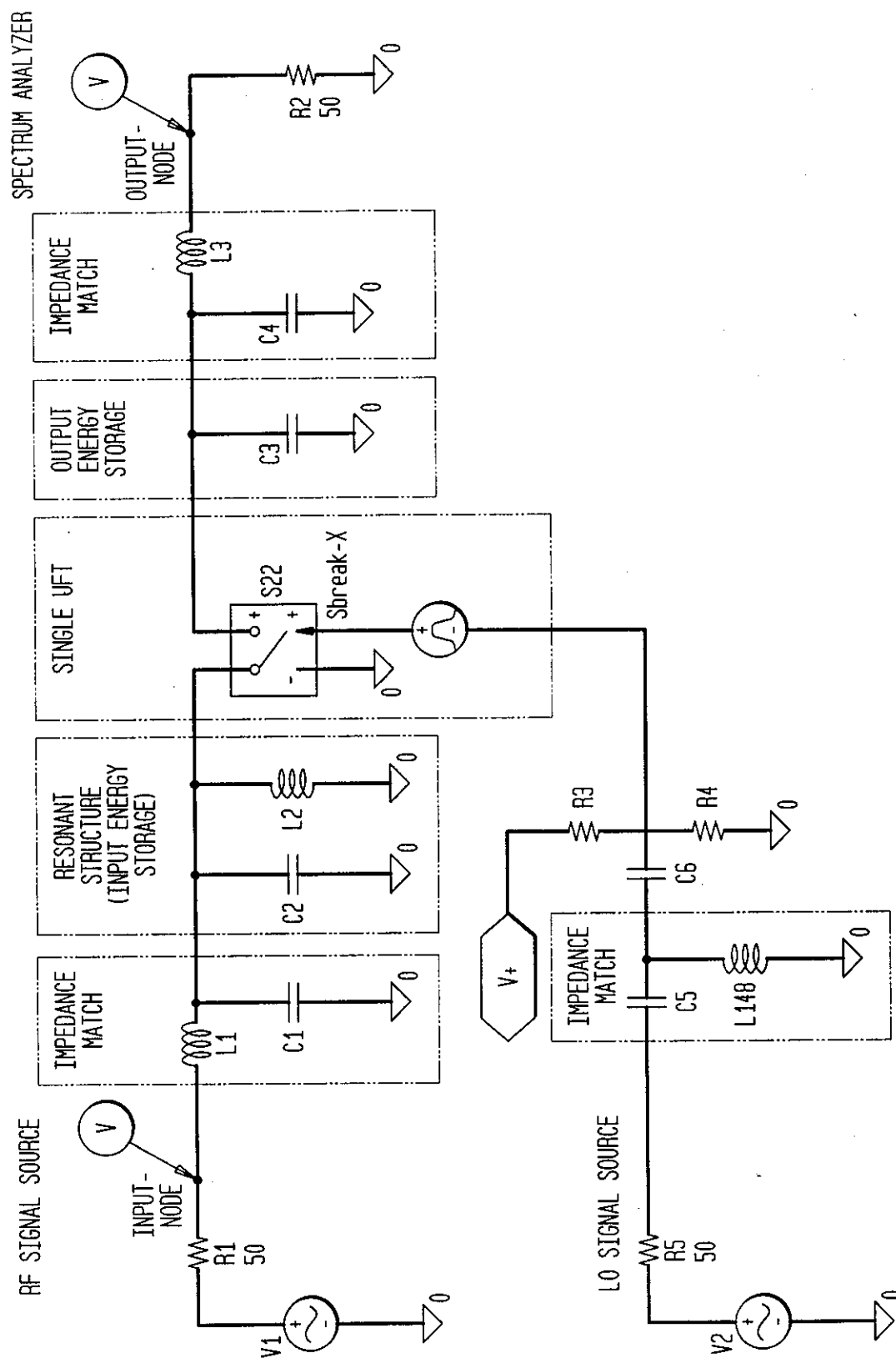
PULSE WIDTH ERROR EFFECT FOR 1/2 CYCLE



262/283

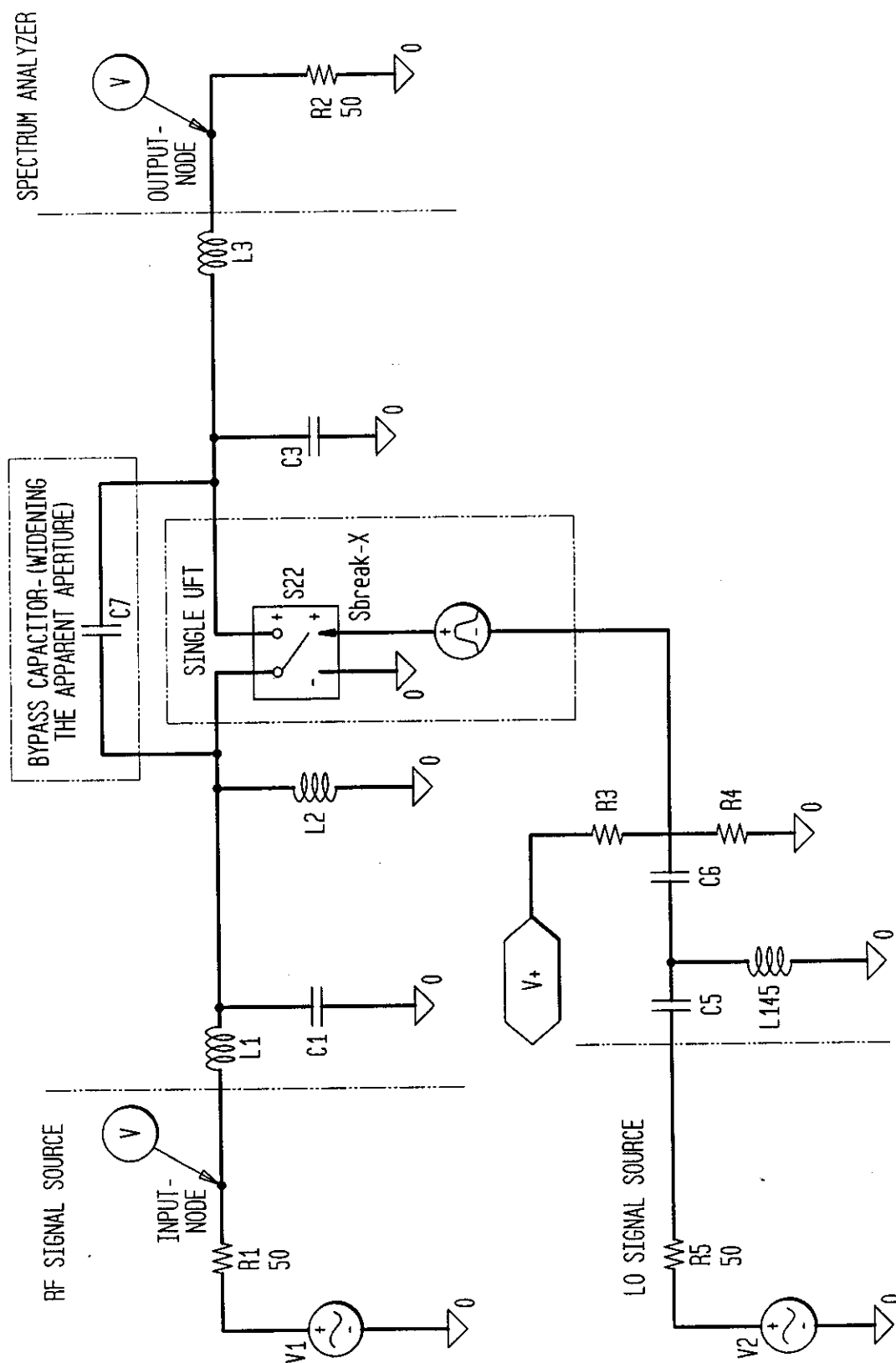
FIG. 259

SINGLE-ENDED UFD MODULE



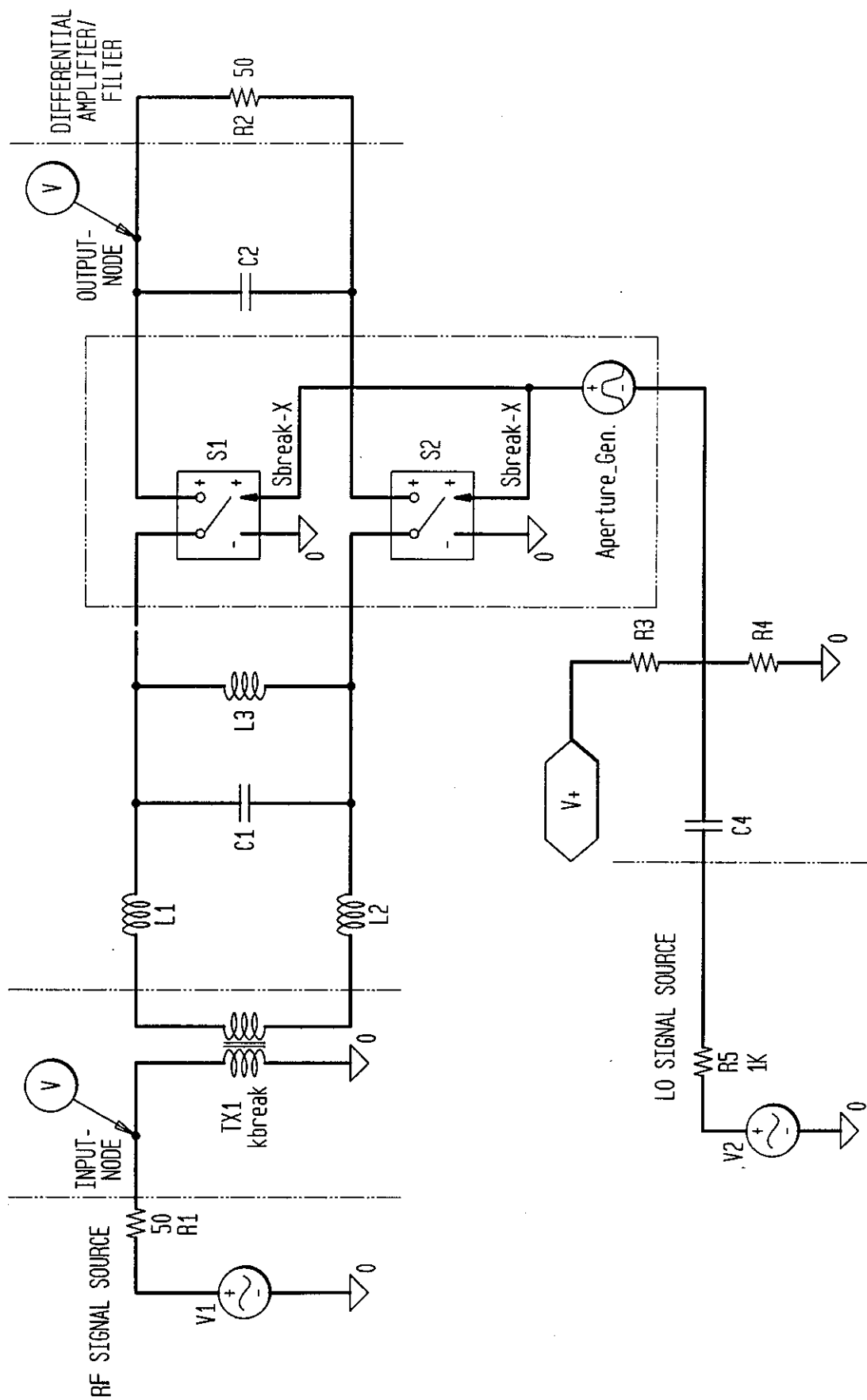
263/283

FIG. 260
SINGLE-ENDED UFD MODULE



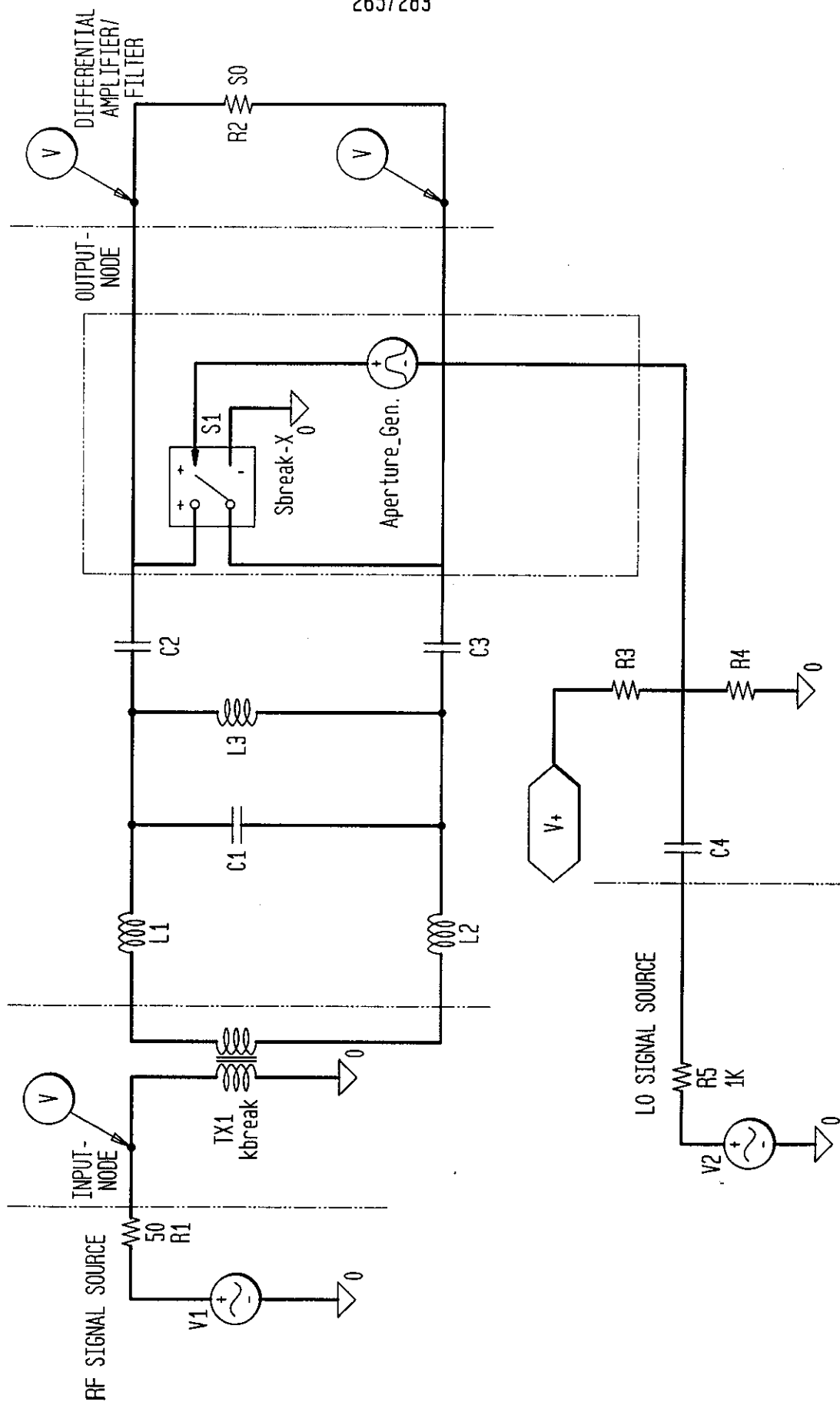
264/283

FIG. 261
FULL DIFFERENTIAL



265/283

FIG. 262
FULL DIFFERENTIAL



266/283

FIG. 263

SINGLE-ENDED, NEAR IDEAL SIMULATION

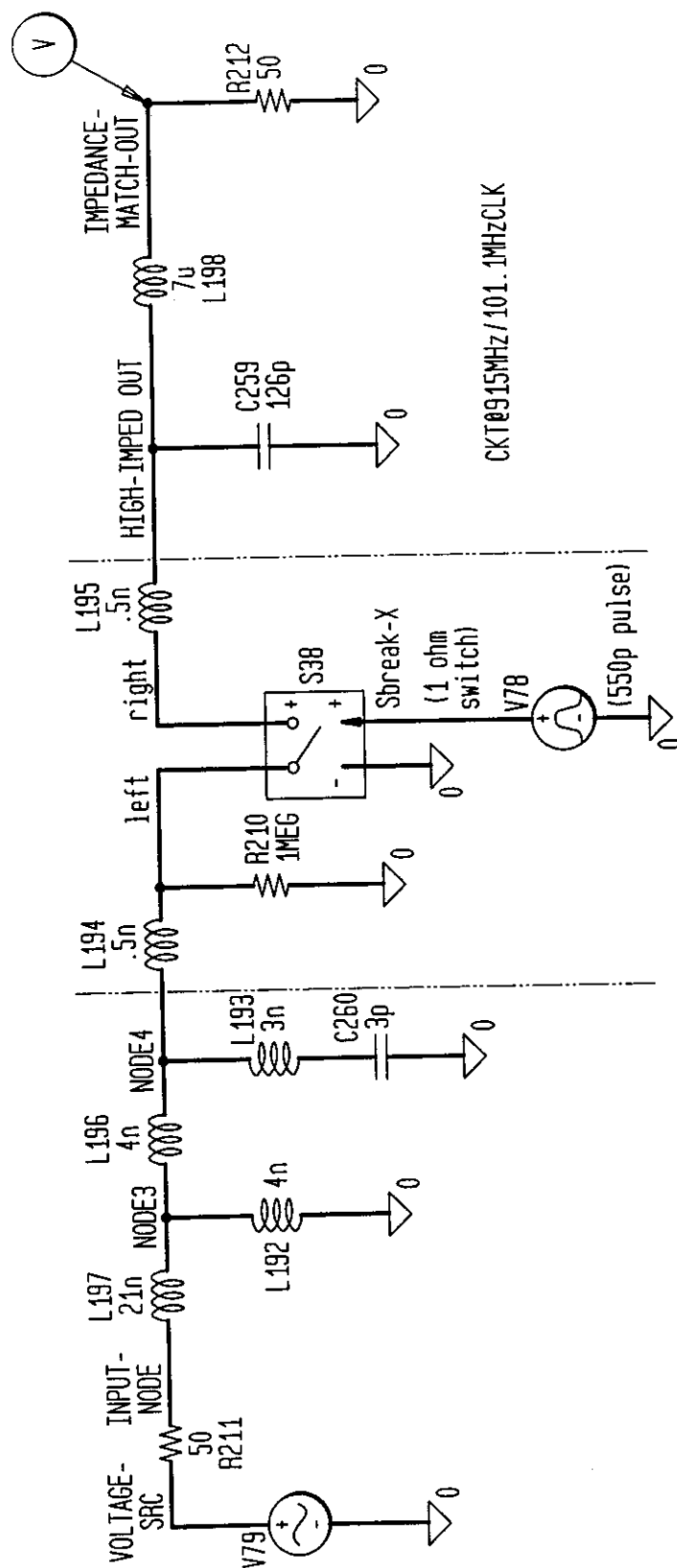


FIG. 264

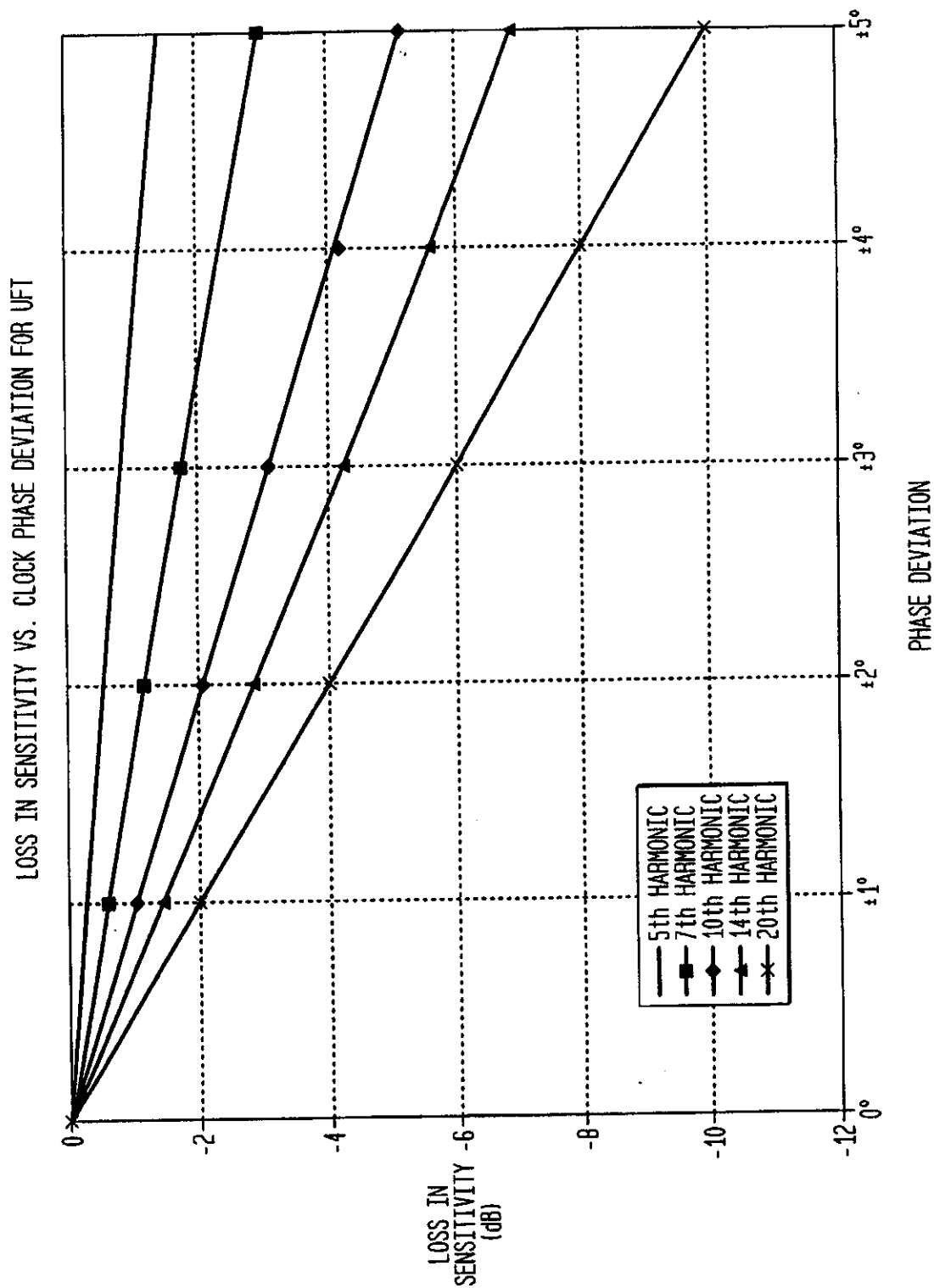
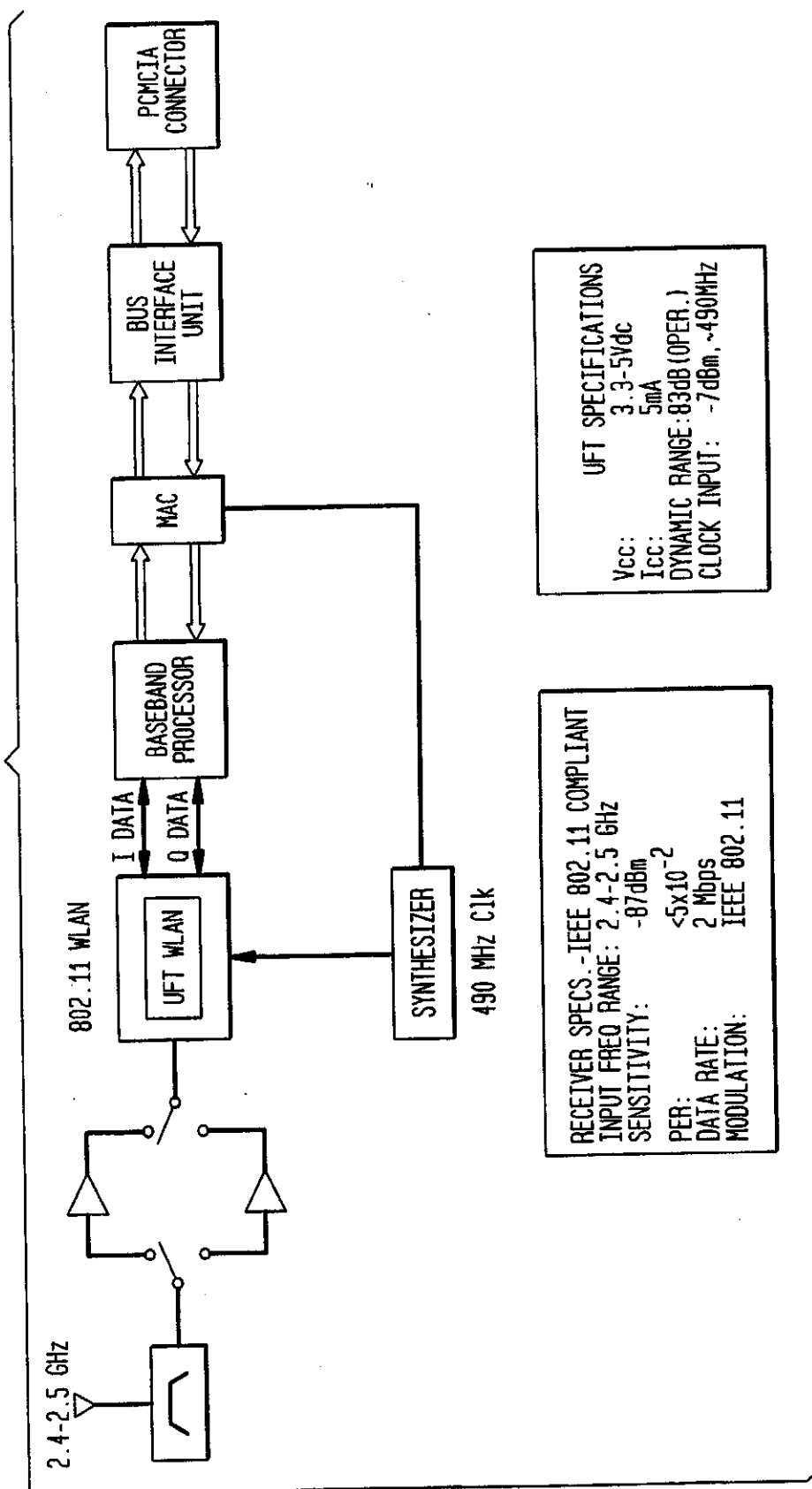


FIG. 265



269/283

802.11 WLAN-RECEIVER/TRANSMITTER

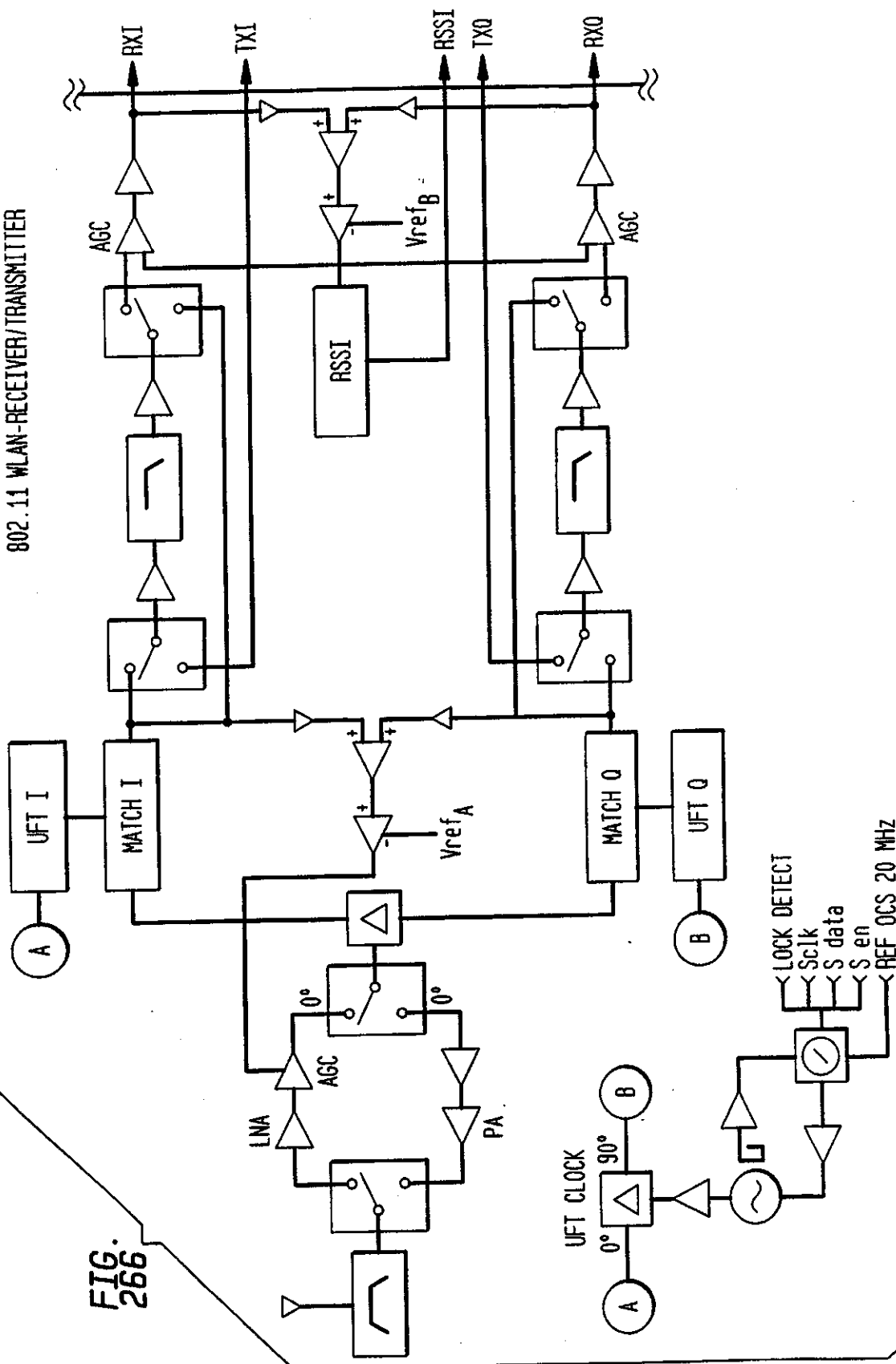


FIG. 267

PARAMETER	802.11 REQUIREMENT OR INDUSTRY PRACTICE	UFT MODULE BASED RX PERFORMANCE
OPERATING BAND	2.4-2.5 GHz	2.4-2.5 GHz
CHANNELS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS	2.402 TO 2.495 IN 1 MHz STEPS 2.412 TO 2.484 GHz IN 5 MHz STEPS
MODULATION	BPSK, QPSK, (BARKER, CCK)	BPSK, QPSK
TX SPECTRAL MASK	FIRST SIDELobe REJECT < -30, +15dBm SECOND SIDELobe REJECT < -50, +15dBm	-35 dBc, -55dBc
EYE OPENING	Verr < 35 FOR 1000 COMPLEX SAMPLES	< .3
OPERATIONAL DYNAMIC RANGE	76 dB (DERIVED)	83 dB
MAX. INPUT, θ , 0% PER	-4 dBm	-4 dBm
SENSITIVITY	-80 dBm θ < 8% PER	-87 dBm θ < 5% PER
ACQUISITION	802.11 DSS AND FH	802.11 DSS AND FH
IMAGE REJECTION	> 80 dB	> 80 dB
LO RERADIATION	< -50 dBm	< -50 dBm
ADJACENT CHANNEL REJECTION	> 35 dB θ 30 MHz OFFSET PER < 8%	> 35 dB θ 30 MHz OFFSET PER < 5%
POWER	3.3, 5V 1.5W (RX MODE)	3.3, 5V, 700mW

271/283

FIG. 268

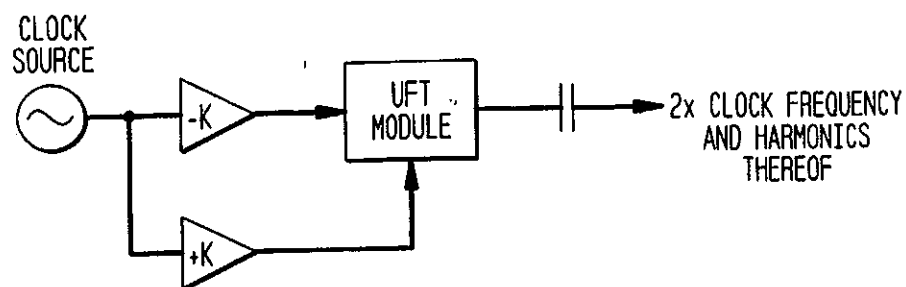


FIG. 269

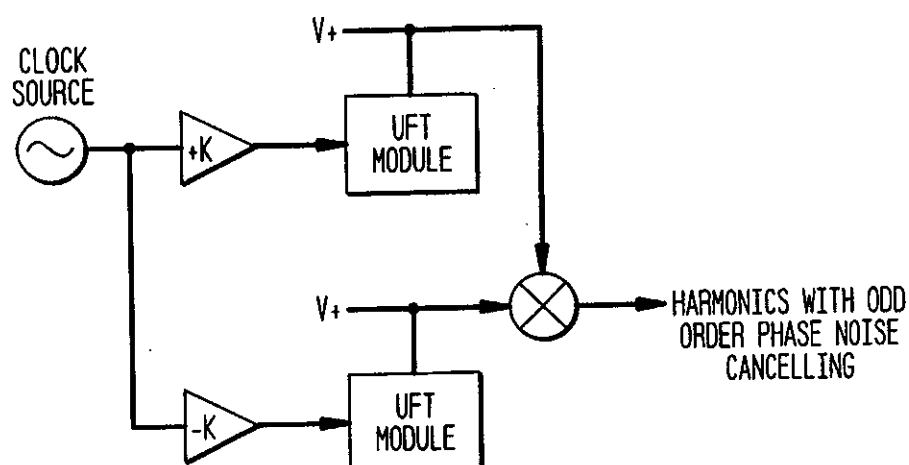
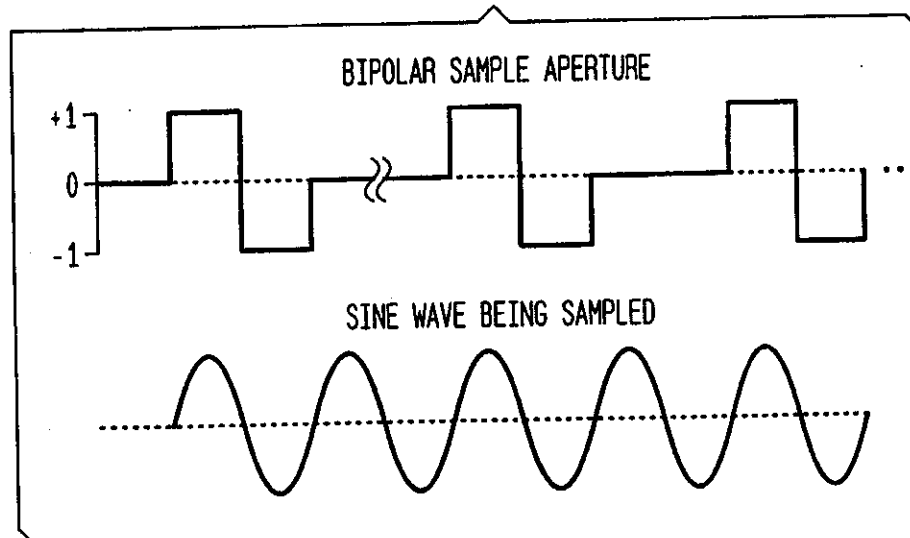


FIG. 270



272/283

FIG. 271

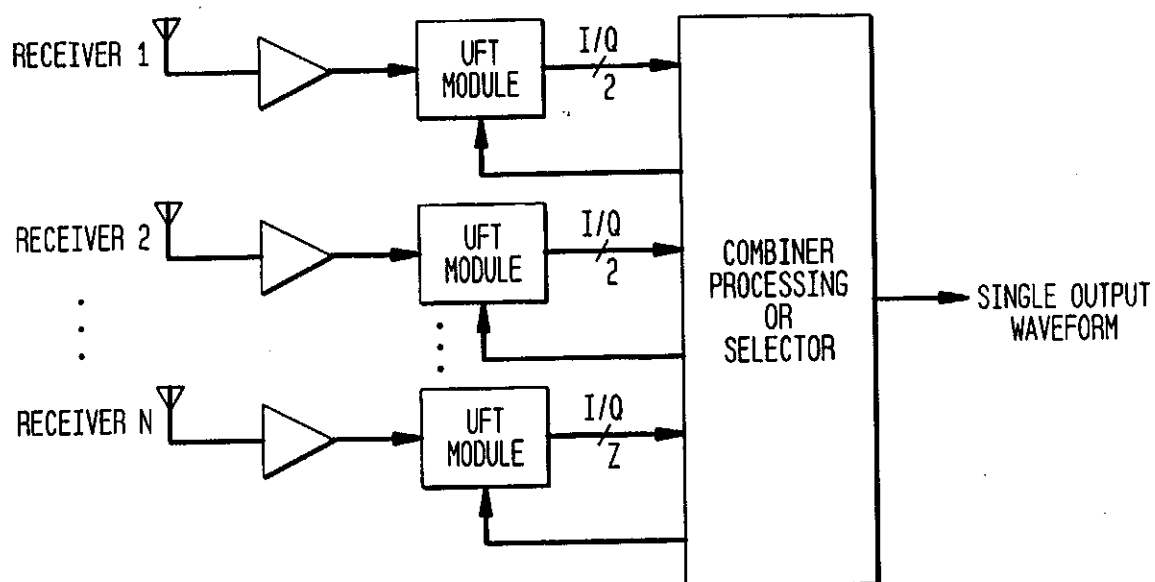
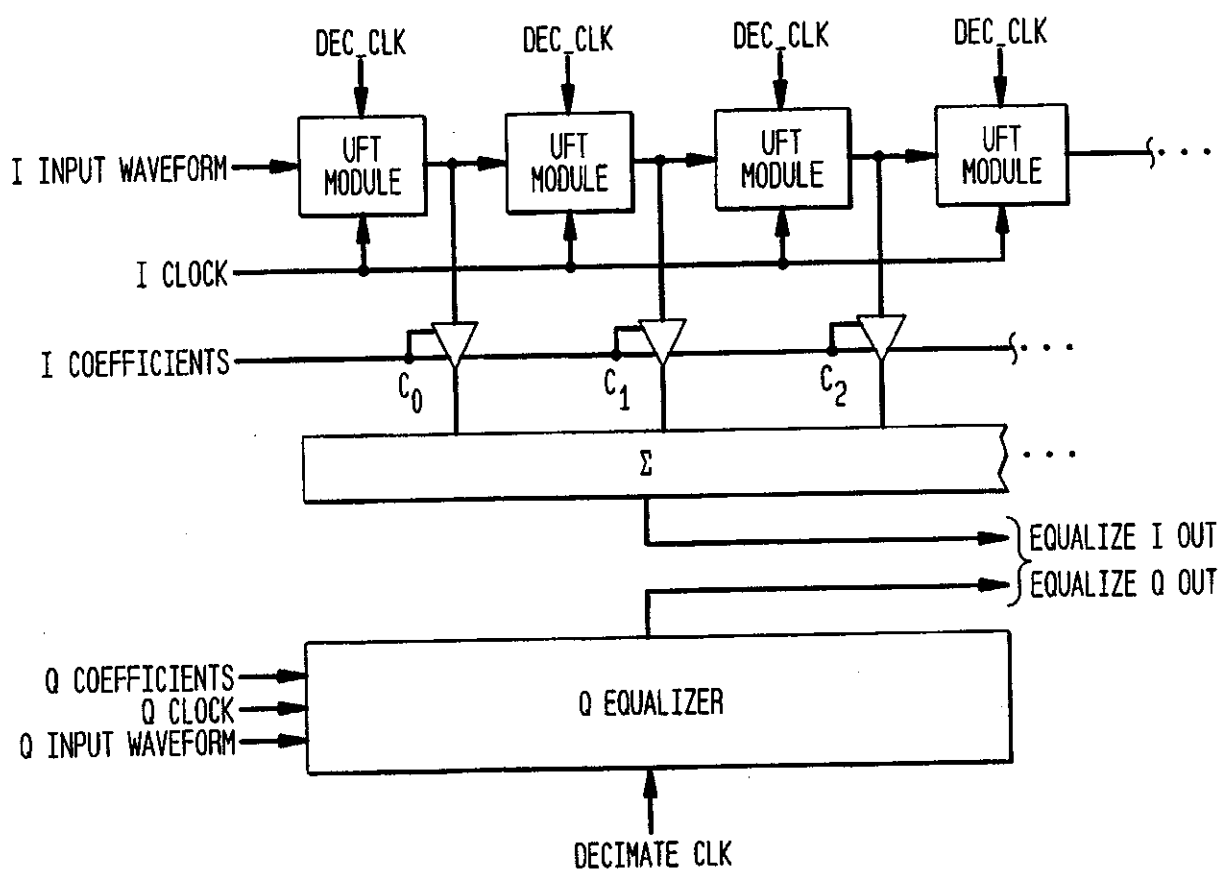


FIG. 272



273/283

FIG. 273

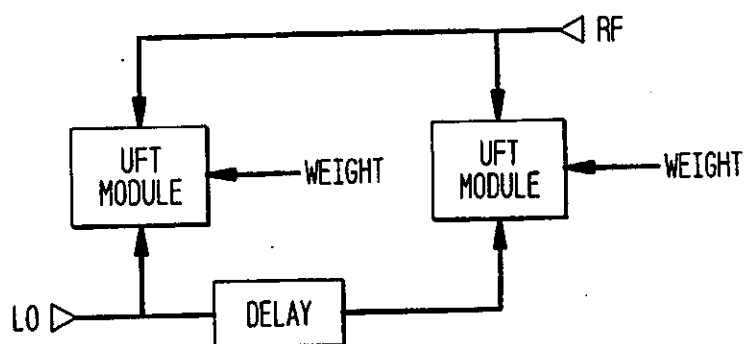
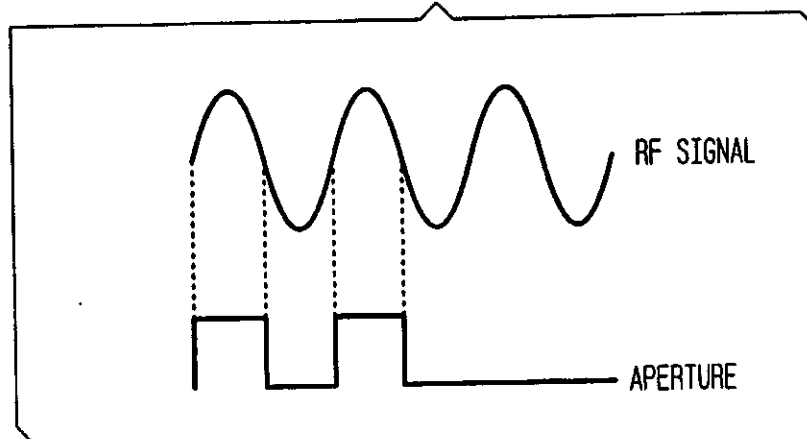


FIG. 274



274/283

FIG. 275

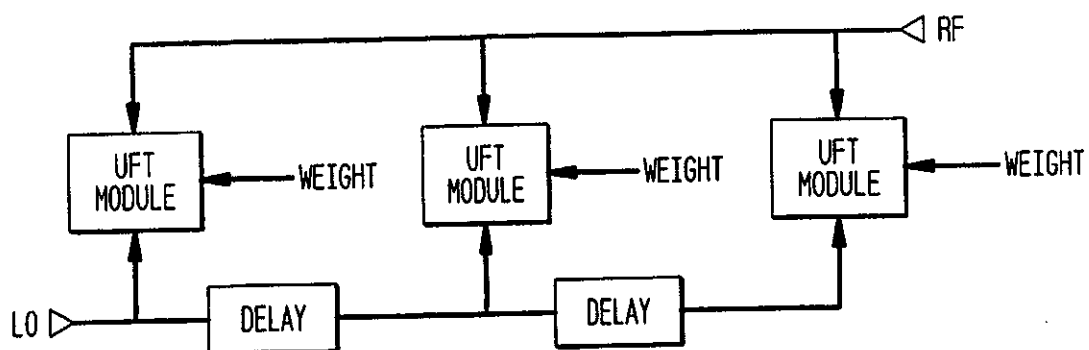


FIG. 276

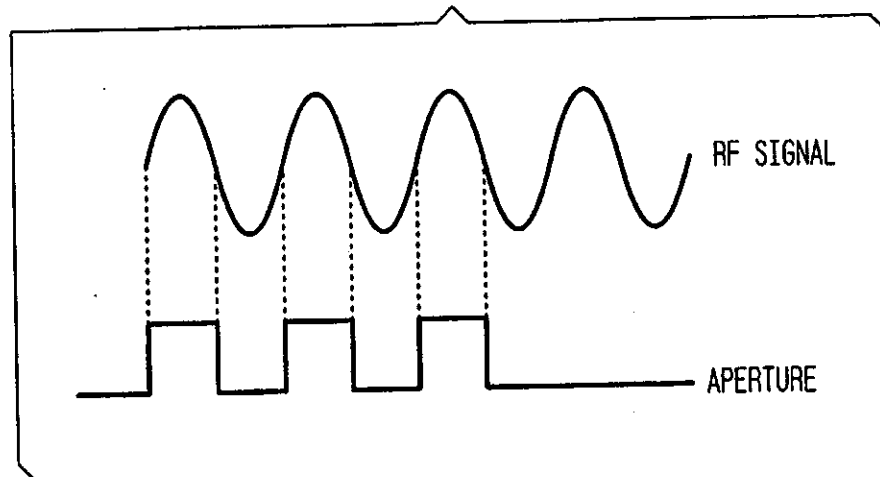
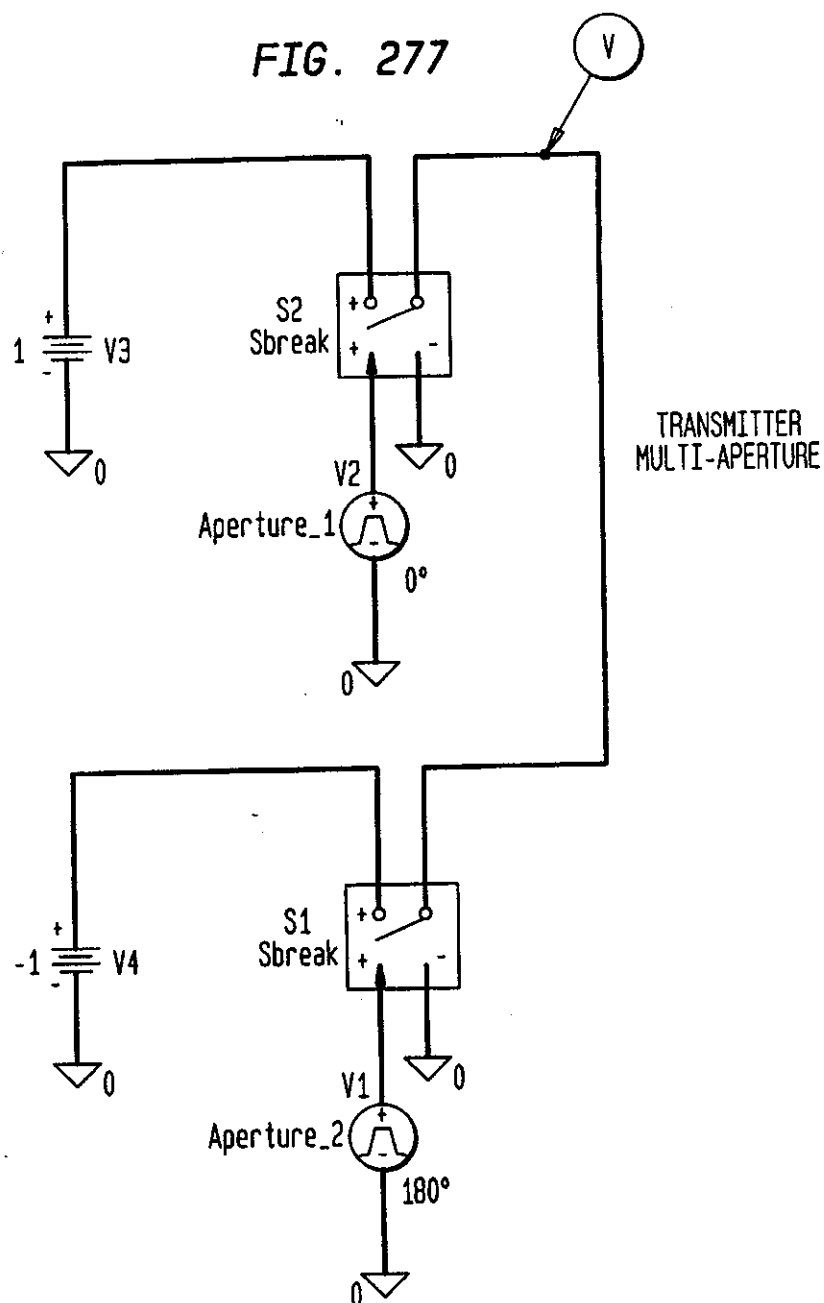
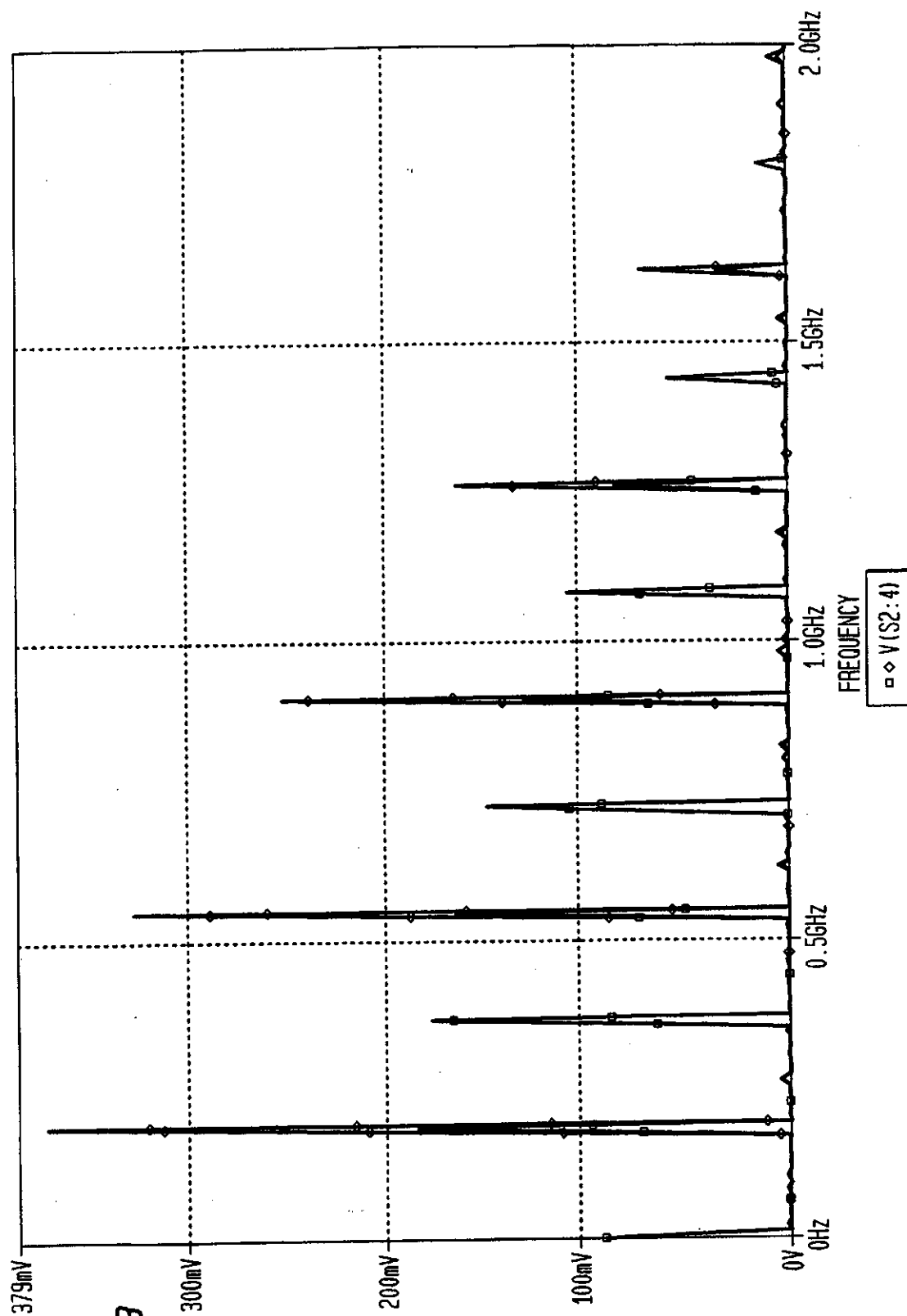
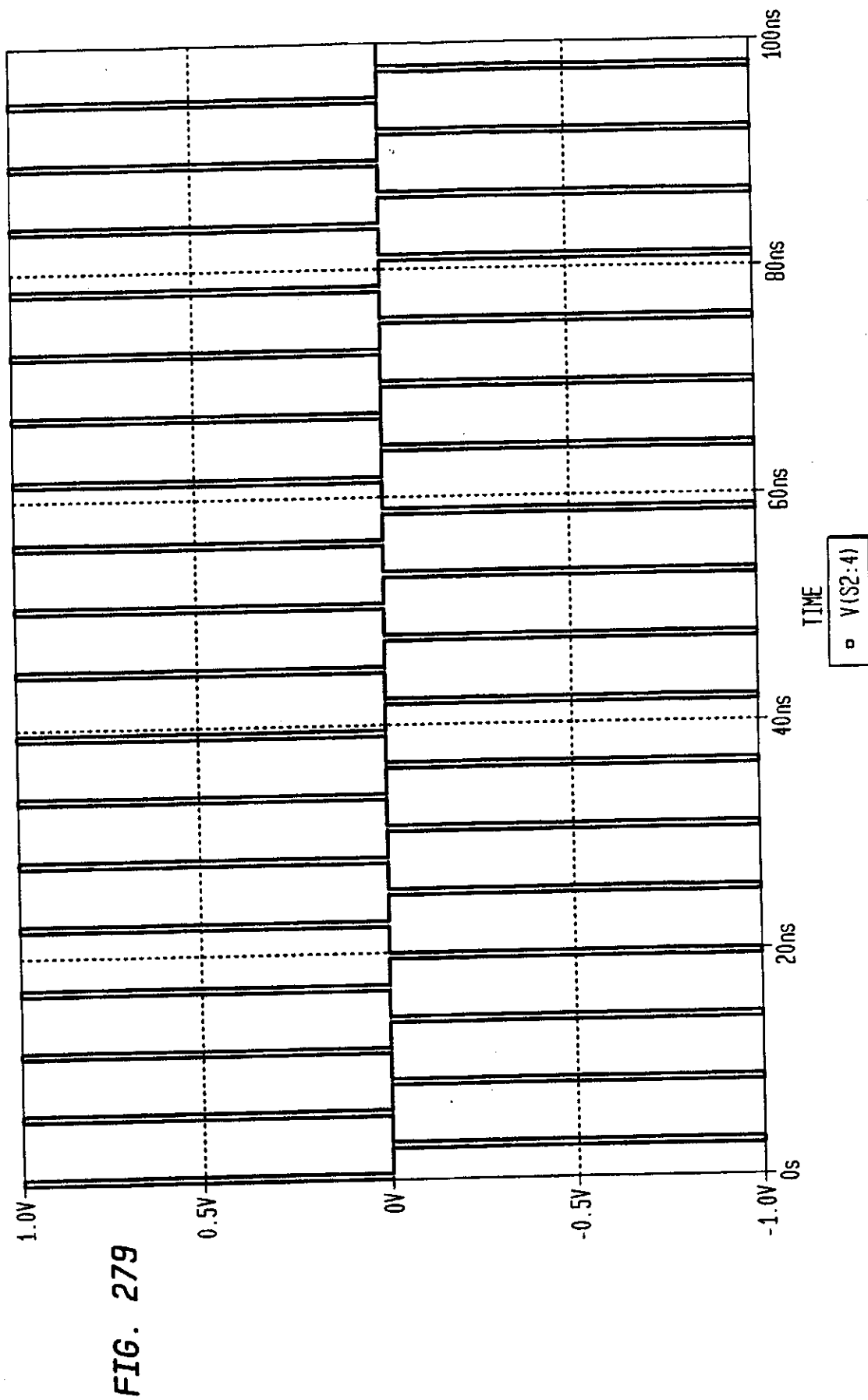


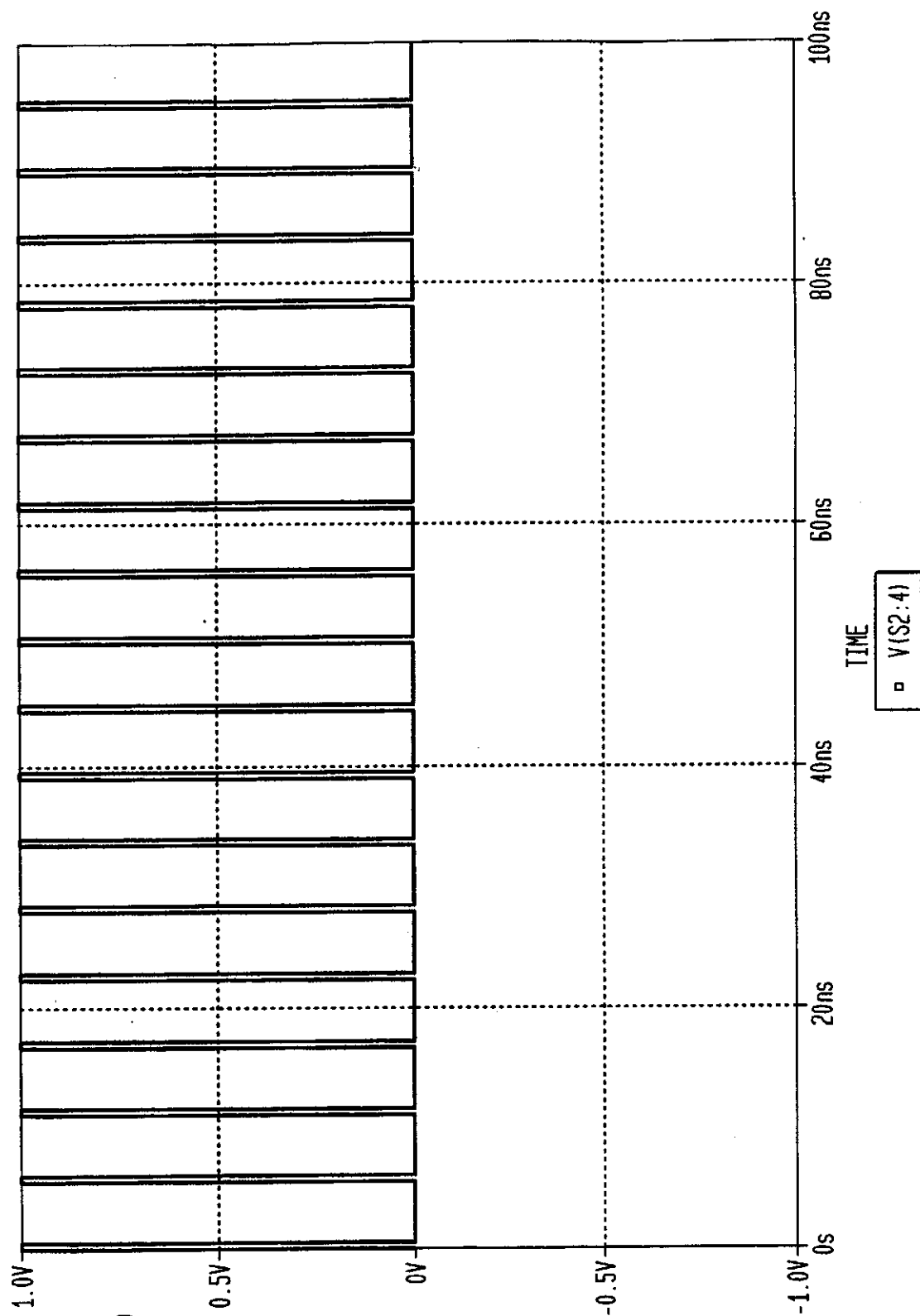
FIG. 277





277/283

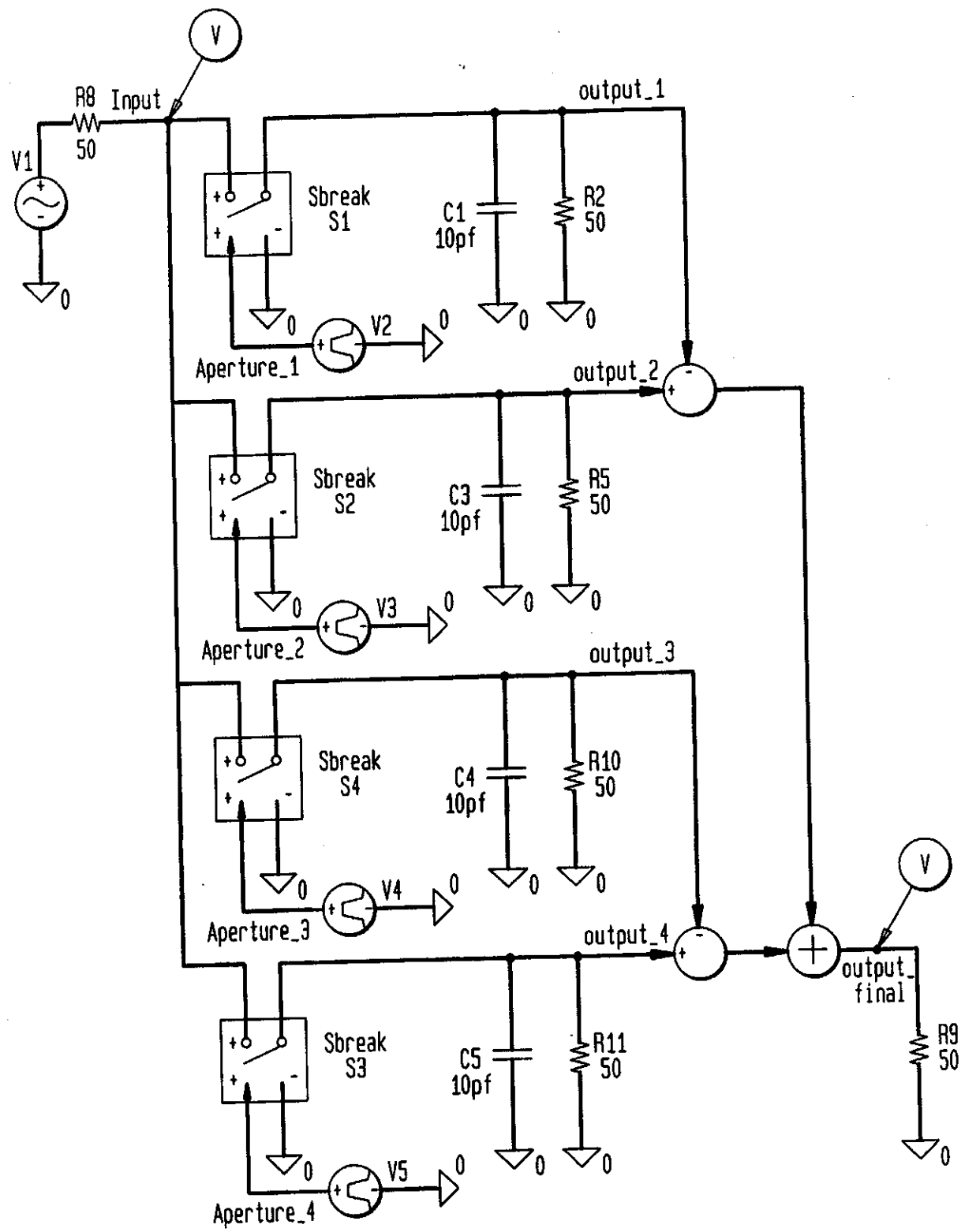




279/283

FIG. 281

MULTIPLE APERTURE RECEIVER IMPLEMENTATION



280/283

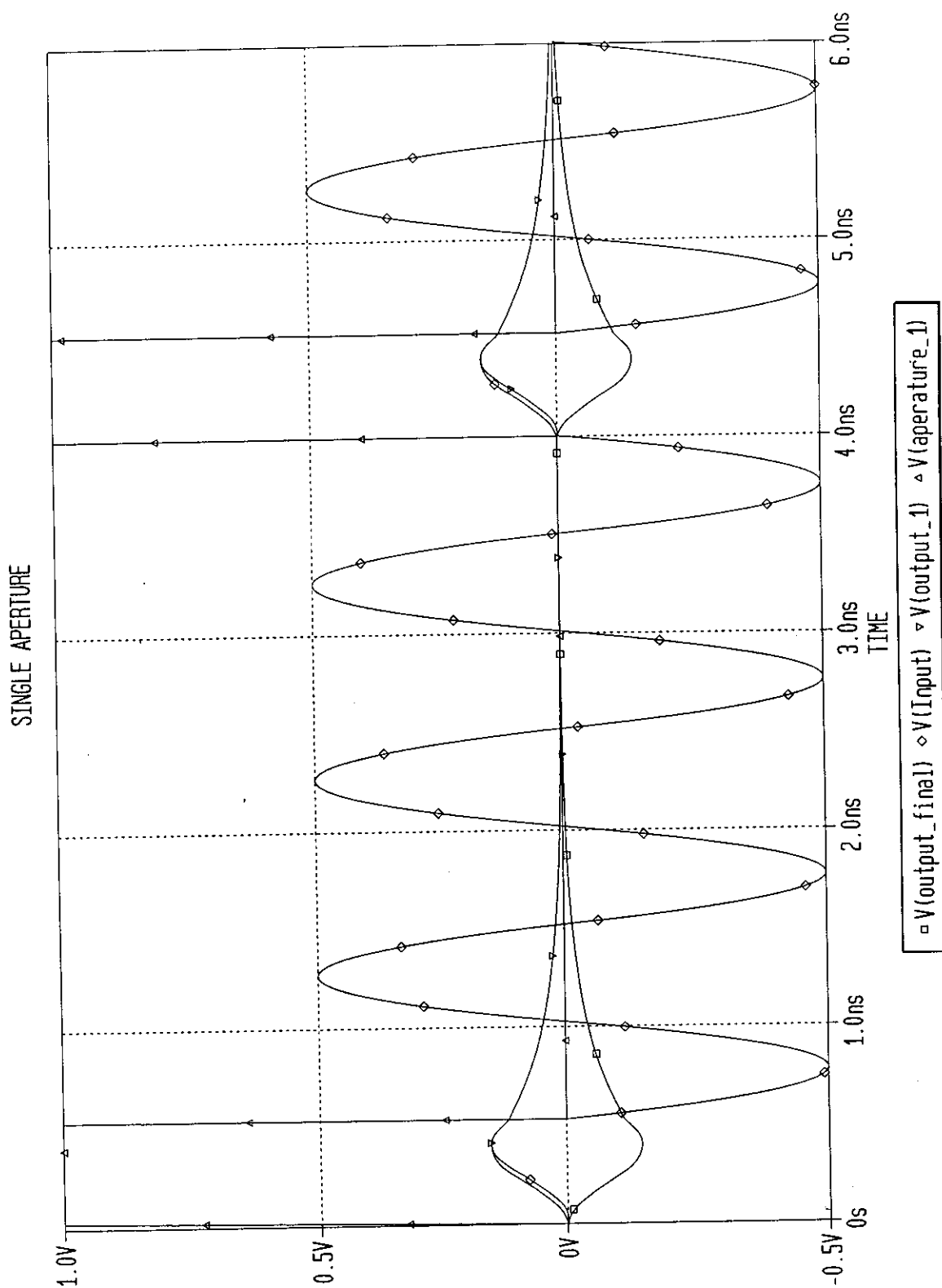
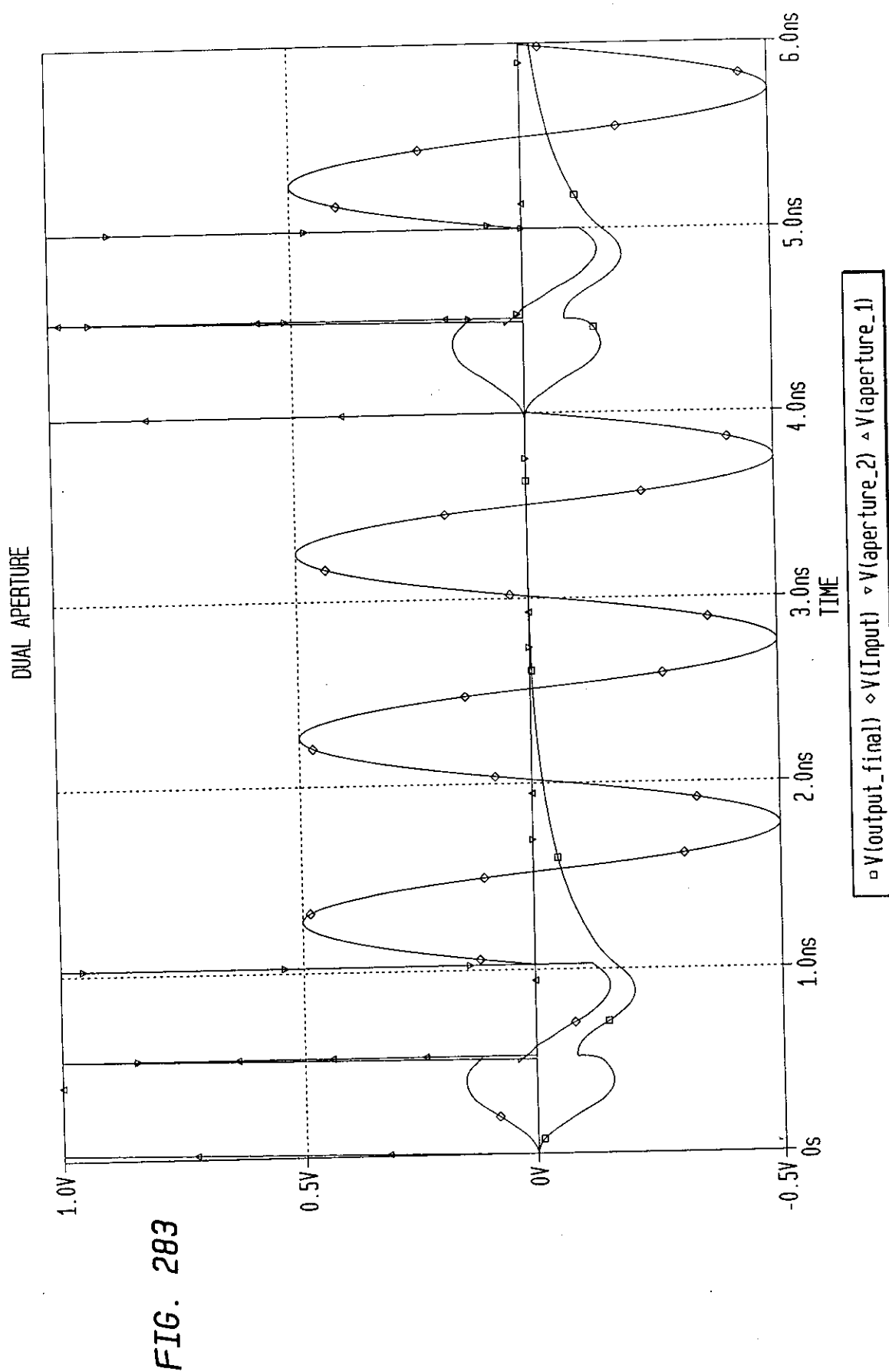


FIG. 282

281/283



282/283

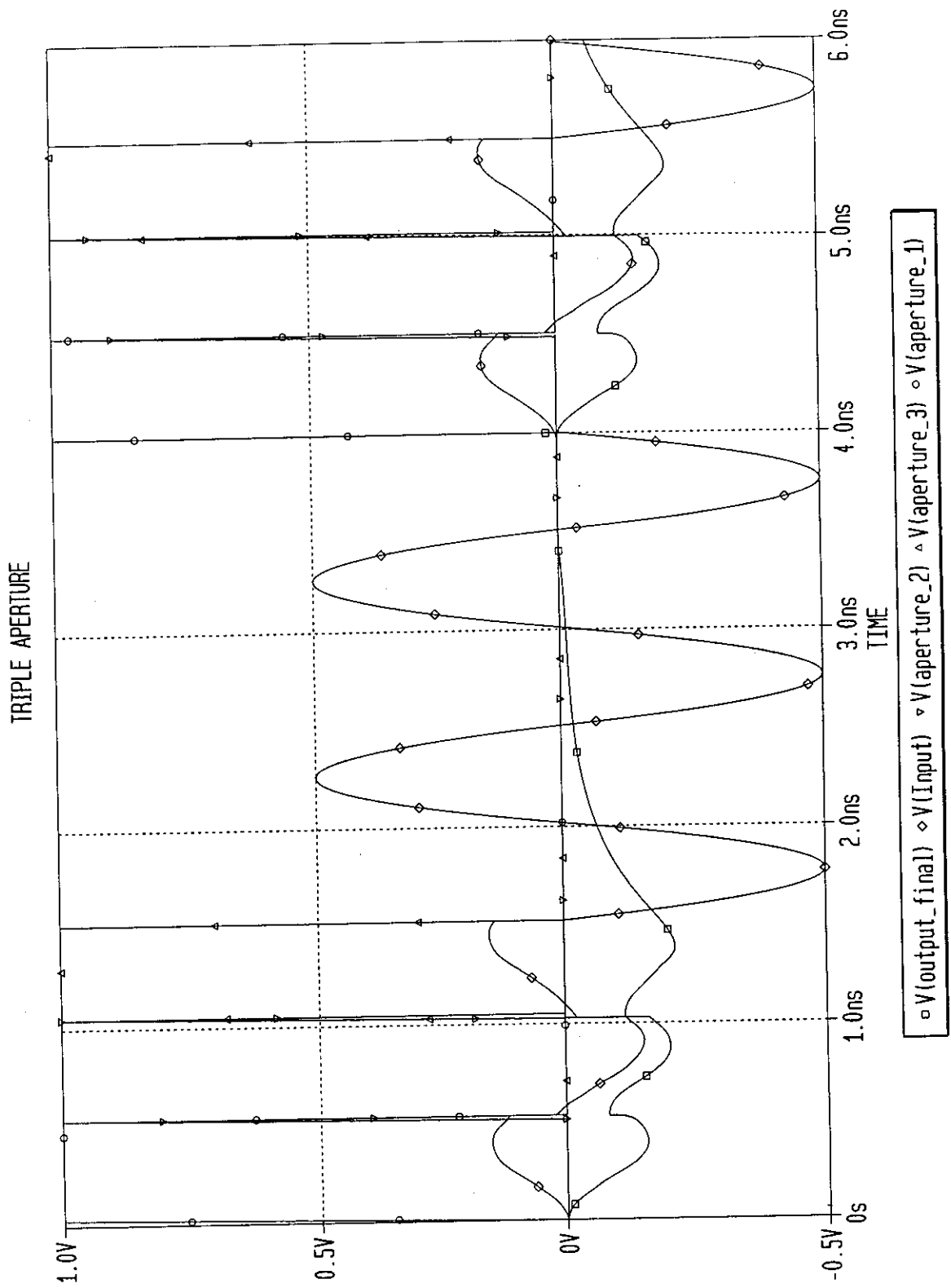


FIG. 284

283/283

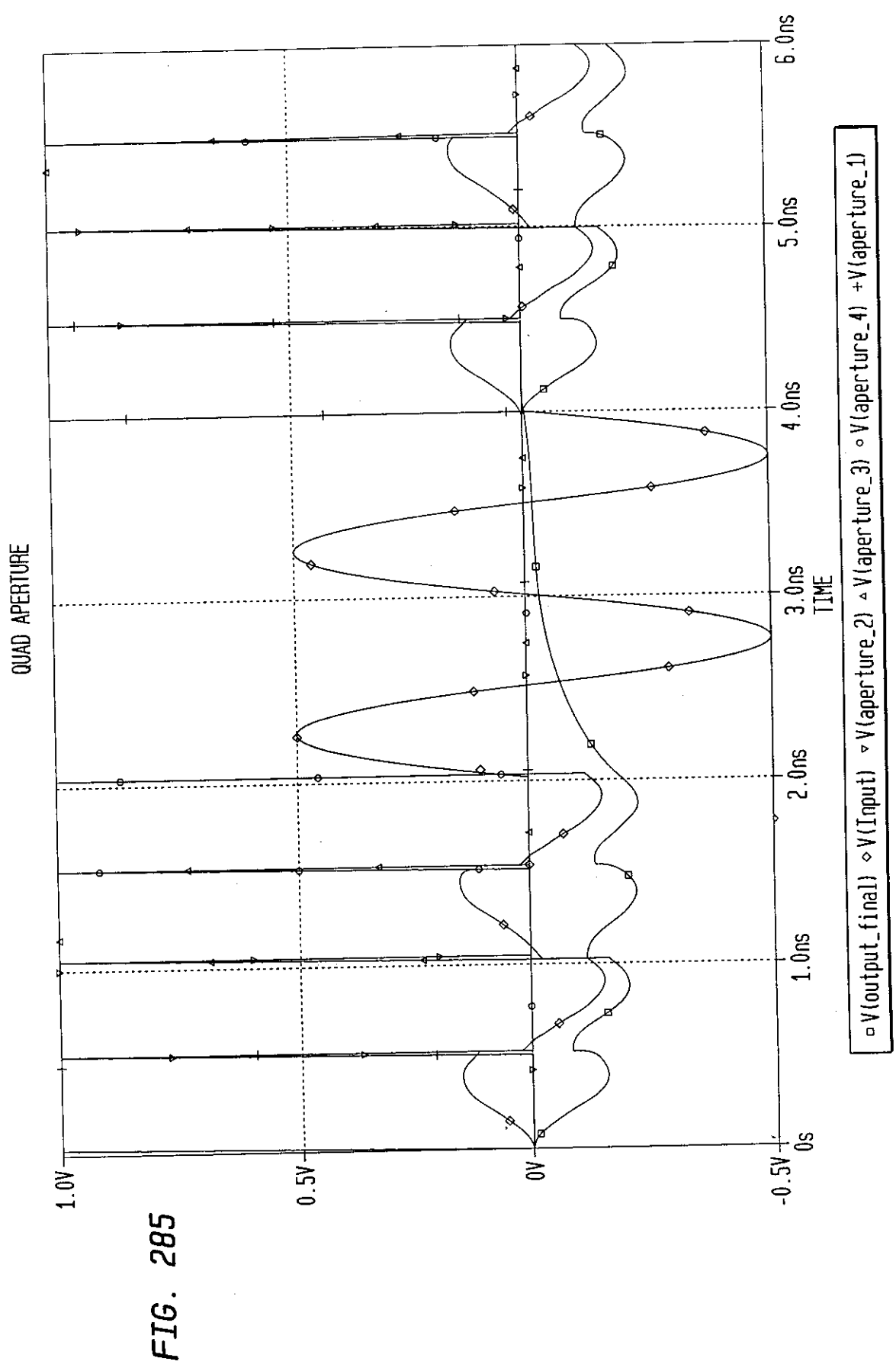


FIG. 285