

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) TRANSISTOR BIASING ARRANGEMENT

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a transistor biasing arrangement in which the quiescent collector current of a transistor in an amplifier stage is determined by the collector current of another transistor in a biasing portion. In particular, the invention provides such an arrangement in which the collector current of the biasing transistor is relatively low compared with that of the other transistor, so that the power dissipation in the biasing portion is relatively low. As will become clear hereinafter, the biasing arrangement of the invention is particularly suited for integrated circuit fabrication in that it comprises substantially only transistor and resistor functional components. The fabrication and interconnection of transistors and resistors in a monolithic chip can be achieved by techniques well known in the art.

According to the present invention there is provided a circuit arrangement in which the collector current of a first, biasing, transistor is determinative of the quiescent collector current of a second, amplifying, transistor, each transistor having base, emitter and collector electrodes. The collector-to-emitter path of the first transistor and a first resistor are serially connected for direct currents between a first common point connected to receive such current through a relatively high resistance and a second common point. The emitter electrode of the second transistor is coupled to said second common point, this coupling having a substantially lower impedance than said first resistor, and a second resistor is connected for direct currents from said first common point to the base electrode of said second transistor exclusive of said relatively high resistance, the

collector electrode of said second transistor being connected to receive an applied energizing potential. A third resistor is connected for direct currents from the collector electrode to the base electrode of said first transistor exclusive of said first resistor, this third resistor providing the sole source of bias to the base electrode of said first transistor and the overall arrangement being such that the second transistor is operative to develop a higher quiescent collector electrode current than the quiescent collector electrode current in the first transistor.

In the accompanying drawings:

FIGURE 1 is a schematic circuit diagram of a common emitter amplifier stage biased according to a prior art arrangement;

FIGURE 2 is a schematic circuit diagram of a prior art modification of the common emitter amplifier stage of FIGURE 1; and

FIGURE 3 is a schematic circuit diagram of a common emitter amplifier stage embodying the principles of the present invention.

Referring to FIGURE 1, there is shown a prior art common emitter amplifier stage of the type described in U.S. Patent 3,364,434, issued on January 16, 1968. The stage comprises an amplifier transistor 10 having emitter, base and collector electrodes 12, 14, and 16, respectively, and a biasing transistor 18 having corresponding electrodes 20, 22 and 24.

The base electrodes 14 and 22 are coupled to a first common voltage point 26 via resistors 28 and 30, while the emitter electrodes 12 and 20 are directly connected to a second common voltage point 32, which typically may be ground. The collector electrodes 16 and 24 are each coupled to a source of energizing potential, the collector electrode 16 by means of a resistor 34 and the collector electrode 24 by means of a resistor 36. The collector electrode 24 is further connected to the common voltage point 26, with the resistors 28 and 30 coupled thereto being of equal value. Input signals supplied to the base electrodes 14 and 22 will be amplified by the transistors 10 and 18 and will be developed as amplified at the collector elec-

trode 16. United States Patent 3,364,434 also discloses an alternative arrangement in which equal valued resistors may be inserted between the respective emitter electrodes 12 and 20 and the common voltage point 32.

Each of the above prior art common emitter amplifier stage configurations serves to provide a quiescent collector current for transistor 10 which is equal to that for transistor 18, independent of changes in transistor characteristics due to temperature variations which are common to both, as when the amplifier stage is fabricated by integrated circuit techniques. This provides matching of, and thermal coupling between, transistors 10 and 18. The value of resistor 28 is made equal to that of resistor 30. Thus, the collector currents of the transistors will be substantially identical as long as transistor 10 is not in saturation. This is true since both base electrodes 14 and 22 will be driven from the same source, namely, the common voltage point 26.

Such similarities of current can be disadvantageous, however, where the amplifier arrangement serves as the high current output stage of a signal channel incorporated on an integrated chip, for example. With energizing potential sources of similar value, it will be noted that the power dissipation in the biasing portion will be comparable to that in the amplifying portion—100 milliwatts or so, where the collector output current is 10 milliamps drawn from a 10 volt source. As will be well appreciated, this 100 milliwatts of dissipation in the biasing portion represents a substantial percentage of allowable dissipation on an integrated chip, and is unduly wasted.

One suggested way of reducing this unnecessary dissipation is to vary the ratio between resistors 28 and 30, so as to cause related, but not equal, collector currents to flow in the transistors 10 and 18. By selecting resistor 30 to be twice the resistance value of resistor 28, for instance, the collector current in the biasing portion of the amplifier arrangement can be shown to be reduced. However, the collector current in the amplifying portion would then become undesirably dependent upon the forward current gains (betas) of the two transistors and would tend to vary from chip to chip.

A second suggested way, shown in FIGURE 2, effectively uses the biasing portion to bias several amplifying portions connected in parallel.

For ten output transistors, represented in parallel connection, the resistance ratio between the collector electrode resistors 40 and 42 would be 10:1, and the same ratio would substantially hold for the base electrode coupling resistors 44 and 46. Such an arrangement is disadvantageous, however, because it requires appreciable area on the chip.

According to the principles of the present invention, the power dissipation in the biasing portion can be substantially reduced, without depending on the forward current gains of the transistors or requiring any appreciable additional chip area. A common emitter amplifier embodying the principles of this invention is illustrated in FIGURE 3 and, as shown, adds to the FIGURE 1 configuration, a resistor 50 between the emitter electrode 20 and the common voltage point 32, the emitter electrode 12 remaining directly connected to that point. A mathematical analysis of this circuit follows:

a) the voltage at the common point 26 is given by the expression:

$$V_{BE_{18}} + I_{B_{18}} R_{50} + I_{B_{18}} R_{30} = V_{BE_{10}} + I_{B_{10}} R_{28} \quad (1)$$

where $V_{BE_{10}}$ and $V_{BE_{18}}$ are the forward base-to-emitter voltage drops of transistors 10 and 18 respectively, $I_{B_{10}}$ and $I_{B_{18}}$ are the respective base currents of those two transistors, $I_{E_{18}}$ is the emitter current of transistor 18, and R_{50} , R_{28} and R_{30} are the resistance values of resistors 50, 28 and 30.

b) by substituting the fraction $\frac{kT}{q} \log_e \left(\frac{I_o}{I_s} \right)$ for the V_{BE} term and the following relationships in expression (1)

$$I_{B_{18}} = \frac{I_o_{18}}{\beta_{18}}; I_{B_{10}} = \frac{I_o_{10}}{\beta_{10}}; I_o_{18} = \frac{\beta_{18} I_{B_{18}}}{\beta_{18} + 1}$$

expression (1) becomes upon re-arranging:

$$\frac{kT}{q} \log_e \left(\frac{I_o_{18}}{I_{s_{18}}} \right) + I_{B_{10}} \left(\frac{(\beta_{18} + 1) R_{50}}{\beta_{18}} + \frac{R_{30}}{\beta_{18}} \right) = \frac{kT}{q} \log_e \left(\frac{I_o_{10}}{I_{s_{10}}} \right) + I_{B_{10}} \frac{R_{28}}{\beta_{10}} \quad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, q is the unit charge upon an electron, I_o_{10} and I_o_{18} are the collector currents of transistors 10 and 18 respectively, $I_{s_{10}}$ and $I_{s_{18}}$ are the respective leakage currents of

transistors 10 and 18 respectively, $I_{s_{10}}$ and $I_{s_{18}}$ are the respective leakage currents of

those two transistors, and β_{10} and β_{18} are the forward current gains of transistors 10 and 18.

- c) assuming that $\beta_{10} = \beta_{18}$ and $I_{B10} = I_{B18}$, as they should be in an integrated circuit environment, and that β_{10} is large, then expression (2) can be re-written as:

$$I_{010} \left(R_{s0} + \frac{R_{s0} - mR_{28}}{\beta_{10}} \right) = \frac{kT}{q} \log_e m \quad (3)$$

where m is the fraction $\frac{I_{010}}{I_{018}}$

- 10 This latter expression essentially comprises the defining design equation for the common-emitter amplifier arrangement of FIGURE 3. With the same assumptions as in (c) above, it can be shown that the corresponding defining design equation for the prior art arrangement of FIGURE 1 is given by the expression:

$$I_{018} \left(\frac{R_{s0} - mR_{28}}{\beta_{10}} \right) = \frac{kT}{q} \log_e m \quad (4)$$

the same definitions of terms being used throughout.

- 20 Furthermore, the equations for the collector current flow in transistor 18 in the FIGURES 1 and 3 configurations can be respectively represented as:

$$V - V_{BE18} = I_{B18} R_{s0}$$

$$I_{018} = \frac{R_{s0}}{R_{s0} - I_{B18} R_{s0}} \quad (5)$$

25 and

$$V - V_{BE18} = I_{B18} R_{s0} - I_{B18} R_{28}$$

$$I_{018} = \frac{R_{s0}}{R_{s0} - I_{B18} R_{28}} \quad (6)$$

- 30 where V is the voltage value of the energizing potential source for the transistor 18 and R_{s0} is the resistance value of the resistor 36. Noting that the I_{B18} and R_{s0} terms are small and that

V_{BE18} approximates 0.75 volts for an integrated circuit transistor, equations (5) and (6) can each be approximated by:

$$I_{018} = \frac{V - 0.75}{R_{s0}} \quad (7)$$

It can be seen from expressions (4) and (7) describing the arrangement of FIGURE 1 that with selected values for V and R_{s0} to give a predetermined I_{018} current flow, in order to

provide an I_{010} current flow which is m times

greater, the resistance ratio selected for R_{28} and R_{s0} would have to be varied as β_{10} varied, such as, for example, from chip to chip (except for the unique case where $m=1$ and $R_{s0}=R_{28}$). From expressions (3) and (7) describing the FIGURE 3 configuration, on the other hand, it can be seen that the effect of β_{10} variation is decreased due to the presence of the R_{s0} term. Indeed, R_{s0} may be made equal to mR_{28} , thereby avoiding the dependence of the ratio m upon β_{10} variations for any value of m . Consider the following illustrations:

- a) V is selected to be 10 volts and R_{s0} to be 9.1 kilohms so as to give an I_{018} current

flow of 1 milliamp; I_{010} is desired to be

10 milliamps ($m=10$), R_{28} is chosen as

500 ohms, and $\frac{q}{kT}$ has the value 33

millivolts per milliamp at room temperature; for an assumed β_{10} of 50, R_{s0} in the FIGURE 1 configuration [expression (4)] is calculated to be 8.5 kilohms; but in a different integrated chip environment where β_{10} is 60 instead of 50 due to tolerance variations in the manufacturing processes, R_{s0} would have to be 9.2 kilohms in order to maintain the same 10:1 current ratio—a change of 8.2%.

- b) V , R_{s0} , m , R_{28} and $\frac{q}{kT}$ are as in (a) above,

with R_{s0} in the FIGURE 3 arrangement selected to be 50 ohms; for an assumed β_{10} of 50, R_{s0} is calculated to be 6.0K [expression (3)], while R_{s0} is calculated to be 6.2K in the environment where β_{10} is 60—a change of 3.3%.

- c) V , R_{s0} , m , R_{28} and $\frac{q}{kT}$ are as in (a)

above, with R_{s0} in the FIGURE 3 arrangement selected to be 70 ohms; for an assumed β_{10} of 50, R_{s0} is calculated as 5.0K, the same value as in the environment where β_{10} is 60—indicating freedom from β_{10} variations.

the following table shows the comparative decrease in β_{10} dependency for the common-emitter amplifier stage of FIGURE 3 as contrasted with that of FIGURE 1:

	V volts	R ₈₆ KΩ	m	R ₂₈ Ω	$\frac{q}{KT}$	β ₁₀	R ₅₀ Ω	R ₃₀ KΩ	% change
Figure 1	10	9.1	10	500	33	50	—	8.5	
						60	—	9.2	8.2
Figure 3						50	20	7.5	
						60	20	8.0	6.7
						50	30	7.0	
						60	30	7.4	5.7
						50	40	6.5	
						60	40	6.8	4.6
						50	50	6.0	
						60	50	6.2	3.3
						50	60	5.5	
						60	60	5.6	1.8
						50	70	5.0	
						60	70	5.0	0

A preferred embodiment of the invention will thus be seen to be that where the resistance value of R₃₀ equals m times the resistance value of R₂₈, where there is zero percentage change (i.e., no dependency upon forward current gain). In general, however, improved performance will measurably be obtained whenever the expression

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$$\frac{R_{30} - mR_{28}}{\beta_{10}}$$

is less than R₅₀. In those instances where the current gains of transistors 10 and 18 are not equal, a preferred embodiment of the invention can be shown to be one where

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$$\frac{R_{30}}{\beta_{18}} = \frac{mR_{28}}{\beta_{10}}$$

Improved performance will again be measurably obtained, in general, whenever

$$\frac{R_{30}}{\beta_{18}} - \frac{mR_{28}}{\beta_{10}}$$

is less than R₅₀.

WHAT WE CLAIM IS:—

1. A circuit arrangement in which the collector current of a first, biasing, transistor is determinative of the quiescent collector current of a second, amplifying, transistor, each transistor having base, emitter and collector electrodes, wherein: the collector-to-emitter path of said first transistor and a first resistor are serially connected for direct currents between a first common point connected to receive such current through a relatively high resistance and a second common point, the emitter electrode of said second transistor is coupled to said second common point, this coupling having a substantially lower impedance than said first resistor, a second resistor is connected for direct currents from said first common point to the base electrode of said second transistor exclusive of said relatively high resistance, the collector electrode of said second transistor being connected to receive an applied energizing potential, and a third resistor is connected for direct currents from the collector electrode to the base electrode of said first transistor exclusive of said first resistor, said third resistor providing the sole source of bias to the base electrode of said first transistor, the arrangement being such that the second transistor is operative to develop a higher quiescent collector electrode current than the quiescent col-

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	V volts	R_{36} K Ω	m	R_{28} Ω	$\frac{q}{KT}$	β_{10}	R_{50} Ω	R_{30} K Ω	% change
Figure 1	10	9.1	10	500	33	50	—	8.5	
						60	—	9.2	8.2
Figure 3						50	20	7.5	
						60	20	8.0	6.7
						50	30	7.0	
						60	30	7.4	5.7
						50	40	6.5	
						60	40	6.8	4.6
						50	50	6.0	
						60	50	6.2	3.3
						50	60	5.5	
						60	60	5.6	1.8
						50	70	5.0	
						60	70	5.0	0

5 A preferred embodiment of the invention will thus be seen to be that where the resistance value of R_{30} equals m times the resistance value of R_{28} , where there is zero percentage change (i.e., no dependency upon forward current gain). In general, however, improved performance will measurably be obtained whenever the expression

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$$\frac{R_{30} - mR_{28}}{\beta_{10}}$$

is less than R_{50} . In those instances where the current gains of transistors 10 and 18 are not equal, a preferred embodiment of the invention can be shown to be one where

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$$\frac{R_{30} - mR_{28}}{\beta_{18}} = \frac{mR_{28}}{\beta_{10}}$$

Improved performance will again be measurably obtained, in general, whenever

$$\frac{R_{30}}{\beta_{18}} - \frac{mR_{28}}{\beta_{10}}$$

is less than R_{50} .

WHAT WE CLAIM IS:—

20 1. A circuit arrangement in which the collector current of a first, biasing, transistor is determinative of the quiescent collector current of a second, amplifying, transistor, each transistor having base, emitter and collector electrodes, wherein: the collector-to-emitter path of said first transistor and a first resistor are serially connected for direct currents between a first common point connected to receive such current through a relatively high resistance and a second common point, the emitter electrode of said second transistor is coupled to said second common point, this coupling having a substantially lower impedance than said first resistor, a second resistor is connected for direct currents from said first common point to the base electrode of said second transistor exclusive of said relatively high resistance, the collector electrode of said second transistor being connected to receive an applied energizing potential, and a third resistor is connected for direct currents from the collector electrode to the base electrode of said first transistor exclusive of said first resistor, said third resistor providing the sole source of bias to the base electrode of said first transistor, the arrangement being such that the second transistor is operative to develop a higher quiescent collector electrode current than the quiescent col-

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lector electrode current in the first transistor.

2. Circuit arrangement as claimed in Claim 1 wherein the connection of the emitter electrode of said second transistor to said second common point is a direct current connection of substantially zero impedance.

3. Circuit arrangement as claimed in Claim 1 wherein said first resistor has a resistance value greater than the expression

$$\frac{R_2}{\beta_1} - \frac{mR_2}{\beta_2}$$

where R_2 and R_3 are the respective resistance values of said second and third resistors, m is the ratio between the collector electrode current in said second transistor to the collector electrode current in said first transistor, and β_1 and β_2 are the forward current gains of said first and second transistors respectively.

4. Circuit arrangement as claimed in Claim 1, Claim 2 or Claim 3 wherein the following equation is satisfied:

$$\frac{R_2}{\beta_1} - \frac{mR_2}{\beta_2}$$

where R_2 and R_3 are the respective resistance values of said second and third resistors, m is the ratio between the collector electrode current in said second transistor to the collector electrode current in said first transistor, and β_1 and β_2 are the forward current gains of said first and second transistors, respectively.

5. Circuit arrangement as claimed in Claim 4 wherein said first and second transistors are of the same conductivity type with matched forward current gains, and $R_3 = mR_2$.

6. A transistor circuit arrangement substantially as hereinbefore described with reference to Figure 3 of the accompanying drawing.

7. A transistor circuit arrangement as claimed in any preceding claim fabricated in an integrated circuit.

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