



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11C 8/00	A1	(11) International Publication Number: WO 99/30324 (43) International Publication Date: 17 June 1999 (17.06.99)
(21) International Application Number: PCT/US98/25775 (22) International Filing Date: 4 December 1998 (04.12.98) (30) Priority Data: 08/986,506 8 December 1997 (08.12.97) US (71) Applicant: ATMEL CORPORATION [US/US]; 2325 Orchard Parkway, San Jose, CA 95131 (US). (72) Inventors: RAMAMURTHY, Srinivas; 1079 Gruwell Place, San Jose, CA 95129 (US). TAM, Jinglun; 1530 Hemmingway Road, San Jose, CA 95132 (US). GONGWER, Geoffrey, S.; 1148 McBain Avenue, Campbell, CA 95008 (US). FAHEY, James; 26 bis, rue de la Paix, F-13100 Aix en Provence (FR). VERGER, Neal; 10200 Miller Avenue, Cupertino, CA 95014 (US). SAIKI, William; 2325 Orchard Parkway, San Jose, CA 95131 (US). (74) Agent: SCHNECK, Thomas; Law Offices of Thomas Schneck, P.O. Box 2-E, San Jose, CA 95109-0005 (US).		(81) Designated States: CA, CN, JP, KP, KR, NO, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: **INTEGRATED CIRCUIT WITH FLAG REGISTER FOR BLOCK SELECTION OF NONVOLATILE CELLS FOR BULK OPERATIONS**

(57) Abstract

Bulk operation logic circuitry (fig. 1) for use in carrying out bulk program, erase, verify and margining operations on nonvolatile memory cells of a PLD, FPGA, flash-based microcontroller, EEPROM, flash memory device or other integrated circuit containing such cells includes a flag register (31) for designating one or more selected blocks of cells to which the bulk operation will be limited. The bulk operation circuitry includes a controller (11), with a state machine (13) and associated control logic (17, 19), that distributes system clock signals and provides control signals to an instruction register (21), the flag register (31), an address register (33) and one or more data registers (35) to control loading of instructions and data into those registers through a serial input (SDI). The state machine is responsive to a mode signal (MODE) for switching it from a normal user state into a bulk operation state. The use of a flag register (31) allows simplification of the instruction set (Fig. 4) to register load instructions and basic bulk operation instructions (and a flow through operation using a serial output from the registers), while providing a wide variety of possible block selections for the different bulk operations.

