

CLAIMS

1. A method for forming a semiconductor device, the method comprising:
forming a nanosheet stack over a substrate, the nanosheet stack comprising alternating semiconductor layers and sacrificial layers;
forming a sacrificial liner over the nanosheet stack;
forming a dielectric gate structure over the nanosheet stack and the sacrificial liner;
forming a first inner spacer on a sidewall of the sacrificial layers;
forming a gate over channel regions of the nanosheet stack, the gate comprising a conductive bridge that extends over the substrate in a direction orthogonal to the nanosheet stack; and
forming a second inner spacer on a sidewall of the gate.
2. The method of claim 1, wherein forming the gate further comprises removing a portion of the nanosheet stack and the dielectric gate structure to expose sidewalls of the sacrificial layers.
3. The method of claim 2, wherein forming the gate further comprises removing the sacrificial liner and the sacrificial layers.
4. The method of claim 1, wherein forming the first inner spacer comprises recessing the sacrificial layers.
5. The method of claim 1, wherein forming the gate further comprises:
forming a gate dielectric;
forming a conductive region over the gate dielectric; and
removing exposed portions of the gate dielectric.
6. The method of claim 1 further comprising forming a first source or drain region on a sidewall of the first inner spacer and forming a second source or drain region on a sidewall of the second inner spacer.
7. The method of claim 1 further comprising forming a gate contact on a surface of the conductive bridge.
8. A semiconductor device comprising:
a nanosheet stack over a substrate;
a gate over channel regions of the nanosheet stack, the gate comprising a conductive bridge that extends over the substrate in a direction orthogonal to the nanosheet stack;
a dielectric gate structure over the nanosheet stack and the gate;
a first inner spacer on a first end of the nanosheet stack; and
a second inner spacer on a second end of the nanosheet stack;
wherein a gate dielectric extends between the first inner spacer and the gate but not between the second

inner spacer and the gate.

9. The semiconductor device of claim 8 further comprising a first source or drain region on a sidewall of the first inner spacer.

10. The semiconductor device of claim 9 further comprising a second source or drain region on a sidewall of the second inner spacer.

11. The semiconductor device of claim 8 further comprising a gate contact on a surface of the conductive bridge.

12. The semiconductor device of claim 11, wherein the dielectric gate structure is positioned between the nanosheet stack and the gate contact.