

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
07 November 2024 (07.11.2024)



(10) International Publication Number
WO 2024/229066 A1

(51) International Patent Classification:

H01L 23/047 (2006.01) H01L 23/495 (2006.01)
H01L 23/24 (2006.01) H01L 23/00 (2006.01)
H01L 23/31 (2006.01)

(21) International Application Number:

PCT/US2024/027146

(22) International Filing Date:

01 May 2024 (01.05.2024)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

18/311,100 02 May 2023 (02.05.2023) US

(71) Applicant: SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC [US/US]; 5701 N. Pima Road, Scottsdale, Arizona 85250 (US).

(72) Inventors: LIU, Yong; 1 Ebb Tide Drive, Cumberland Foreside, Maine 04110 (US). CHEN, Liangbiao; 23 Col-

by Dr., Scarborough, Maine 04074 (US). CHEW, Chee Hiong; 302, S2 A7/4, Green Street Home, Seremban Two, Seremban, 70300 (MY).

(74) Agent: LEIJA, Javier M.; Onsemi, 5701 N. Pima Road, Scottsdale, Arizona 85250 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, CV,

(54) Title: POWER SEMICONDUCTOR PACKAGE WITH MOLDING CAVITY

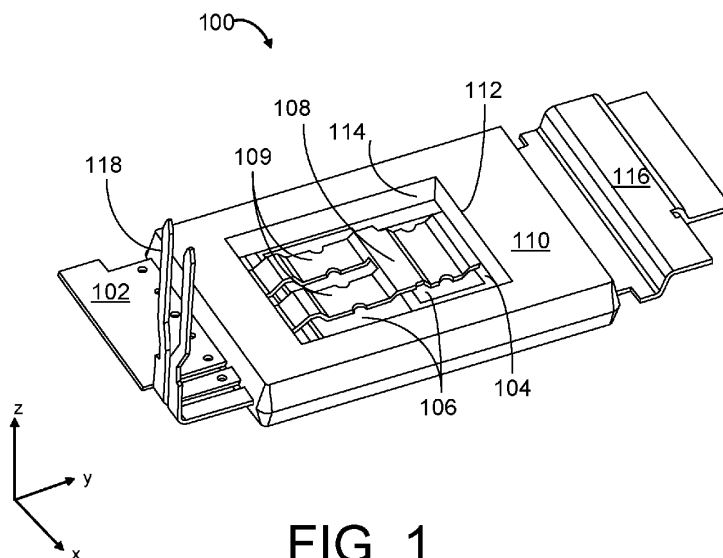


FIG. 1

(57) Abstract: A high-power semiconductor device module (100) is implemented with a cavity (112) in the molding package (110). The cavity (112) reduces a volume of the molding compound, preventing an accumulation of stress in the module (100), and associated warpage of the molding package (110). Chip assemblies (106) within the module (100) are designed to fit within the cavity (112), so that semiconductor dies, and sensing devices (204) therein are protected from damage during a sintering process in which the module (100) is mounted to a heat sink. After the sintering process, the cavity (112) can be sealed with a gel material (114). The molding package (110) described herein can also enhance reliability of the module (100) during operation, ensuring that the product is robust for electric and hybrid electric vehicle applications.

[Continued on next page]

GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))