

Claims

1. An epitaxially coated semiconductor wafer of monocrystalline silicon, comprising a p⁺-doped substrate wafer, where an oxygen concentration of the substrate wafer is not less than 5.3×10^{17} atoms/cm³ and not more than 6.0×10^{17} atoms/cm³ and a resistivity of the substrate wafer is not less than 5 mΩcm and not more than 10 mΩcm; and a p-doped epitaxial layer of monocrystalline silicon which covers an upper side face of the substrate wafer,
 - wherein the substrate wafer is configured to form BMDs (bulk microdefects) after a two-stage heat treatment is performed on the epitaxially coated semiconductor wafer, where the density of BMDs has a maximum of not less than 2×10^{10} /cm³, the distance of the maximum from a front side of the epitaxially coated semiconductor wafer is not greater than 20 μm, and the ratio of the densities of BMDs at a distance of 20 μm and at a distance of 60 μm from the front side of the epitaxially coated semiconductor wafer is not less than 5, and the two-stage heat treatment is effected at 850°C over a period of one hour in oxygen and at 1000°C over a period of one hour in oxygen.
2. The epitaxially coated semiconductor wafer as claimed in claim 1, wherein the epitaxial layer has a thickness of not less than 1 μm and not more than 5 μm.
3. The epitaxially coated semiconductor wafer as claimed in claim 1 or claim 2, characterized by a denuded zone having a thickness of not less than 3 μm and not more than 7 μm.
4. A method of producing a p/p⁺ epitaxially coated semiconductor wafer of monocrystalline silicon, comprising:
 - the pulling of a single crystal of silicon at a pulling rate from a melt doped with boron and present in a crucible, where the concentration of oxygen in an envisaged section of the single crystal is not less than 5.3×10^{17} atoms/cm³ and not more than

6.0×10^{17} atoms/cm³ and the resistivity of the single crystal is not less than 5 mΩcm and not more than 10 mΩcm;

the cooling of the single crystal within a temperature range from 600°C to 500°C,

where the dwell time within the temperature range is not less than 353 min and not

5 more than 642 min, and the cooling of the single crystal within a further temperature range from 500°C to 400°C, where the dwell time within the further temperature range is not less than 493 min and not more than 948 min;

the dividing of a substrate wafer from the envisaged section of the cooled single crystal; and

10 the depositing of a p-doped epitaxial layer of monocrystalline silicon on a polished upper side face of the substrate wafer.

5. The method as claimed in claim 4, comprising the pulling of the single crystal at a pulling rate of not less than 0.4 mm/min and not more than 1.8 mm/min.

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6. The method as claimed in claim 4 or claim 5, comprising subjecting the melt to a magnetic field.

7. The method as claimed in claim 4 or claim 5, comprising the omission of the

20 deliberate addition of carbon or of nitrogen or of carbon and of nitrogen to the melt.

8. The method as claimed in claim 4 or claim 5, comprising the cooling of the single crystal in the presence of a water-cooled cooler.

25 9. The method as claimed in claim 4 or claim 5, wherein the deposition of the epitaxial layer is a first heat treatment of the substrate wafer, which is effected at a temperature of more than 700°C.