substrate 176 or 206 is 10 I/O per mm^2, and the I/O density of the PCB is 4 I/O per mm^2, giving a fan-out ratio of 10/4 = 2.5. The I/O density conversion structure 222 relaxes layout design rules for the PCB conductive layers to reduce I/O density and simplify routing for the lower I/O density tier 223 to reduce cost.

FIG. 16a shows extended semiconductor device 174 with fan-out interconnect structure 170 positioned over for mounting to substrate 176. Substrate 176 with bumps 226 is positioned over for mounting to PCB 50. FIG. 16b shows semiconductor device 174 mounted to substrate 176 and substrate 176 mounted to PCB 50. The higher I/O density of semiconductor die 124 is translated through fan-out interconnect structure 170 to the lower I/O density of substrate 176. Likewise, substrate 176 can translate its I/O density to a lower I/O density of PCB 50. In each case, the I/O density conversion structure between each tier relaxes layout design rules for the lower tier conductive layers to reduce I/O density and simplify routing for the lower I/O density tier to reduce cost.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making an extended semiconductor device, comprising:

providing a semiconductor wafer having a plurality of semiconductor die with a plurality of contact pads formed on a surface of the semiconductor die;

separating the semiconductor die to form a peripheral region around the semiconductor die;

depositing an insulating material in the peripheral region around the semiconductor die;

forming an interconnect structure over the semiconductor die and insulating material, the interconnect structure having an input/output (I/O) density less than an I/O density of the contact pads on the semiconductor die;

providing a substrate having an I/O density consistent with the I/O density of the interconnect structure; and

mounting the semiconductor die to the substrate with the interconnect structure electrically connecting the contact pads of the semiconductor die to the first conductive layer of the substrate.

2. The method of claim 1, wherein forming the interconnect structure includes:

forming a first insulating layer over the semiconductor die and insulating material in the peripheral region;

forming a second conductive layer over the first insulating layer and contact pads of the semiconductor die; and

~~forming a second insulating layer over the second conductive layer.~~

1. A semiconductor device, comprising:

a first semiconductor die;

an insulating material deposited in a peripheral region around the first semiconductor die;

an interconnect structure formed over the first semiconductor die and including,

(a) a first conductive layer extending from a contact pad of the first semiconductor die over a surface of the insulating material, and

(b) a plurality of bumps formed over the first conductive layer; and

a substrate including a second conductive layer, wherein the first semiconductor die is mounted to the substrate with the bumps contacting the second conductive layer and a fan-out ratio (FR) of an I/O density of the first semiconductor die to an I/O density of the substrate is given as FR = $p^2*(N/d^2)$, where p is package pitch, N is number of non-redundant I/O per die, and d is die size.

2. The semiconductor device of claim 1, wherein the I/O density of the substrate is less than the I/O density of the first semiconductor die.

3. The method of claim ~~2~~1, wherein ~~forming~~ the interconnect structure further includes ~~forming~~ a plurality of conductive columns ~~over the second~~ formed between the bumps and first conductive layer.

4. ~~The method of claim 1, further including disposing a discrete electrical component in the peripheral region adjacent~~ The semiconductor device of claim 1, further including a second semiconductor die disposed over the interconnect structure adjacent to the first ~~to the~~ semiconductor die.

~~5. The method of claim 1, further including mounting a plurality of semiconductor die each with the interconnect structure over the substrate.~~

~~6. A method of making an extended semiconductor device, comprising:~~

~~providing a first tier device having a first I/O density;~~

~~forming an input/output (I/O) density conversion structure over the first tier device;~~

~~providing a second tier device having a second I/O density less than the first I/O density; and~~

~~mounting the first tier device to the second tier device with the I/O density conversion structure electrically connecting the first tier device to the second tier device.~~

~~7. The method of claim 6, wherein the first tier device includes providing a semiconductor die having a plurality of contact pads formed on a surface of the semiconductor die with the first I/O density.~~

8. The method of claim 7, wherein forming the I/O density conversion structure includes:

depositing an insulating material in a peripheral region around the semiconductor die; and

forming an interconnect structure over the semiconductor die and insulating material, the interconnect structure having an output density less than a density of the contact pads on the semiconductor die.

9. The method of claim 8, wherein forming the interconnect structure further includes:

forming a plurality of conductive columns over the interconnect structure; and

forming a plurality of bumps over the conductive columns.

10. The method of claim 8, wherein the second tier device includes providing a substrate with a conductive layer having an I/O density less than an I/O density of the contact pads on the semiconductor die.

11. The method of claim 10, wherein mounting the first tier device to the second tier device includes mounting the semiconductor die to the substrate with the interconnect structure electrically connecting the contact pads of the semiconductor die to the conductive layer of the substrate.

12. The method of claim 8, further including mounting a plurality of semiconductor die each with the interconnect structure over the substrate.

13. An extended semiconductor device, comprising:

~~a semiconductor die having a plurality of contact pads formed on a surface of the semiconductor die;~~

~~an insulating material deposited in a peripheral region around the semiconductor die; and~~

~~an interconnect structure formed over the semiconductor die and insulating material, the interconnect structure having an input/output (I/O) density less than an I/O density of the contact pads on the semiconductor die.~~

~~14. The extended semiconductor device of claim 13, further including a substrate having an I/O density consistent with the I/O density of the interconnect structure, wherein the semiconductor die is mounted to the substrate with the interconnect structure electrically connecting the contact pads of the semiconductor die to the conductive layer of the substrate.~~

~~15. The extended semiconductor device of claim 13, wherein the interconnect structure includes:~~

~~a first insulating layer formed over the semiconductor die and insulating material in the peripheral region;~~

~~a conductive layer formed over the first insulating layer and contact pads of the semiconductor die; and~~

~~a second insulating layer formed over the conductive layer.~~

~~16. The extended semiconductor device of claim 15, wherein the interconnect structure further includes a plurality of conductive columns formed over the conductive layer.~~

~~17. The extended semiconductor device of claim 13, further including a plurality of semiconductor die each with the interconnect structure mounted over the substrate.~~

5. The semiconductor device of claim 4, wherein an I/O density of the second semiconductor die is greater than the I/O density of the first semiconductor die.

6. The semiconductor device of claim 1, wherein the surface of the insulating material is coplanar with an active surface of the first semiconductor die.

7. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed in a peripheral region around the first semiconductor die;

a first input/output (I/O) density conversion structure formed over the first semiconductor die and including,

(a) a conductive layer formed over the first semiconductor die and a surface of the insulating material, and

(b) a plurality of interconnect structures formed over the conductive layer and surface of the insulating material; and

a second I/O density conversion structure disposed over the first I/O density conversion structure, wherein the first I/O density conversion structure translates an I/O density of the first semiconductor die to a second I/O density and the second I/O density conversion structure translates the second I/O density to a third I/O density, wherein a fan-out ratio (FR) of the first I/O density to the second I/O density is given as FR = $p^2*(N/d^2)$, where p is package pitch, N is number of non-redundant I/O per die, and d is die size.

8. The semiconductor device of claim 7, further including a second semiconductor die disposed over the second I/O density conversion structure.

9. The semiconductor device of claim 7, wherein the plurality of interconnect structures includes a conductive column.

10. The semiconductor device of claim 7, further including a second semiconductor die disposed over the first I/O density conversion structure.

11. The semiconductor device of claim 10, wherein the second semiconductor die includes an I/O density different from the I/O density of the first semiconductor die.

12. The semiconductor device of claim 7, further including a discrete component disposed adjacent to the first semiconductor die.

13. The semiconductor device of claim 7, wherein the FR is less than or equal to 10.

14. The semiconductor device of claim 7, wherein the surface of the insulating material is coplanar with an active surface of the first semiconductor die.

15. A semiconductor device, comprising:

a first semiconductor die;

a second semiconductor die, wherein a first I/O density of the first semiconductor die is different from a second I/O density of the second semiconductor die;

an insulating material disposed in a peripheral region around the first semiconductor die and second semiconductor die;

a first input/output (I/O) density conversion structure disposed over the first semiconductor die and second semiconductor die and including,

(a) a conductive layer formed over the first semiconductor die and second semiconductor die and insulating material, and

(b) a plurality of interconnect structures formed over the conductive layer and insulating material, wherein the first I/O density conversion structure translates the first I/O density of the first semiconductor die and the second I/O density of the second semiconductor die to a third I/O density; and

a second I/O density conversion structure disposed over the first I/O density conversion structure, wherein the second I/O density conversion structure translates the third I/O density to a fourth I/O density, wherein a fan-out ratio (FR) of the third I/O density to the fourth I/O density is given as $FR = p^2*(N/d^2)$, where p is package pitch, N is number of non-redundant I/O per die, and d is die size.

16. The semiconductor device of claim 15, wherein the plurality of interconnect structures includes:

a conductive column; and

a bump formed over the conductive column.

17. The semiconductor device of claim 15, wherein the FR is less than or equal to 10.