

CLAIMS

What is claimed is:

1. An apparatus comprising:

an input node;

a charge-sharing node;

a filter-sampling network including a capacitor and a first switch, the first switch coupled between the input node and the capacitor, the filter-sampling network configured to connect or disconnect the capacitor to or from the input node via the first switch;

a digital-to-analog converter including a capacitor array and a second switch, the second switch coupled between the input node and the capacitor array, the capacitor array coupled between the second switch and the charge-sharing node, the digital-to-analog converter configured to connect or disconnect the capacitor array to or from the input node via the second switch; and

a charge-sharing switch coupled between the charge-sharing node and the capacitor, the charge-sharing switch configured to connect or disconnect the capacitor to or from the digital-to-analog converter.

2. The apparatus of claim 1, wherein:

the input node is configured to accept an analog signal;

the filter-sampling network is configured to sample, based on a connection of the capacitor to the input node via the first switch, a first voltage of the analog signal using the capacitor, the first voltage representative of a first sample of the analog signal;

the digital-to-analog converter is configured to sample, based on a connection of the capacitor array to the input node via the second switch, a second voltage of the analog signal using the capacitor array, the second voltage representative of a second sample of the analog signal; and

the charge-sharing switch is configured to produce, based on a connection of the capacitor to the capacitor array, an average voltage at the charge-sharing node, the average voltage representative of an average of the first sample and the second sample.

3. The apparatus of claim 2, wherein the filter-sampling network, the digital-to-analog converter, and the charge-sharing switch are configured to jointly provide alias rejection at the charge-sharing node based on the average voltage.

4. The apparatus of claim 2, wherein the analog signal comprises one signal of a pair of differential analog signals.

5. The apparatus of claim 2, wherein:

a capacitance of the capacitor differs from another capacitance of the capacitor array; and

the charge-sharing switch is configured to produce, based on the connection of the capacitor to the capacitor array, a weighted-average voltage as the average voltage at the charge-sharing node, the weighted-average voltage representative of a weighted average of the first sample and the second sample based on the capacitance of the capacitor and the other capacitance of the capacitor array.

6. The apparatus of claim 1, further comprising a processor coupled to the filter-sampling network, wherein:

the capacitor comprises a programmable capacitor; and

the processor is configured to adjust a capacitance of the programmable capacitor.

7. The apparatus of claim 1, further comprising:

a comparator coupled to the charge-sharing node; and

a successive approximation register coupled between the comparator and the digital-to-analog converter, wherein:

the digital-to-analog converter, the comparator, and the successive approximation register are jointly configured to:

perform a binary search to approximate an average voltage at the charge-sharing node; and

produce, based on the binary search, a binary number that is representative of the average voltage at the charge-sharing node.

8. The apparatus of claim 7, wherein:

the digital-to-analog converter, the comparator, and the successive approximation register are jointly configured to perform the binary search based on a conversion-phase signal; and

the filter-sampling network is configured to connect the capacitor to the input node via the first switch during a portion of time that the conversion-phase signal is indicative of the binary search being performed on a previous average voltage.

9. The apparatus of claim 7, further comprising an analog-to-digital converter, wherein:

the analog-to-digital converter includes the input node, the charge-sharing node, the filter-sampling network, the digital-to-analog converter, the charge-sharing switch, the comparator, and the successive approximation register;

the analog-to-digital converter is configured to sample an analog signal at the input node according to an overall sampling period;

the filter-sampling network is configured to connect or disconnect the capacitor to or from the input node via the first switch based on a first sampling-phase signal;

the digital-to-analog converter is configured to connect or disconnect the capacitor array to or from the input node via the second switch based on a second sampling-phase signal;

the charge-sharing switch is configured to connect or disconnect the capacitor to or from the capacitor array based on a charge-sharing phase signal; and

the first sampling-phase signal, the second sampling-phase signal, and the charge-sharing phase signal respectively close the first switch, the second switch, and the charge-sharing switch at different times within the overall sampling period.

10. The apparatus of claim 1, further comprising:

another filter-sampling network, the other filter-sampling network including another capacitor and a third switch, the third switch coupled between the input node and the other capacitor, the other capacitor coupled between the third switch and the charge-sharing switch, the filter-sampling network configured to connect or disconnect the other capacitor to or from the input node via the third switch; and

the charge-sharing switch is configured to connect or disconnect both the capacitor and the other capacitor to or from the capacitor array.

11. The apparatus of claim 1, wherein:

the digital-to-analog converter includes another capacitor array and a third switch, the third switch coupled between the input node and the other capacitor array, the other capacitor array coupled between the third switch and the charge-sharing node, the digital-to-analog converter configured to connect or disconnect the other capacitor array to or from the input node via the third switch; and

the charge-sharing switch is configured to connect or disconnect the capacitor to or from both the capacitor array and the other capacitor array.

12. The apparatus of claim 1, wherein:

the first switch is coupled to a bottom plate of the capacitor;

the second switch comprises multiple switches that are respectively coupled to bottom plates of multiple capacitors of the capacitor array;

the charge-sharing node is coupled to top plates of the multiple capacitors of the capacitor array; and

the charge-sharing switch is coupled between a top plate of the capacitor and the charge-sharing node.

13. The apparatus of claim 1, wherein:
the first switch is coupled to a top plate of the capacitor;
the second switch comprises multiple switches that are respectively coupled to top plates of multiple capacitors of the capacitor array;
the charge-sharing node is coupled to bottom plates of the multiple capacitors of the capacitor array; and
the charge-sharing switch is coupled between a bottom plate of the capacitor and the charge-sharing node.

14. An apparatus comprising:
an input node configured to accept an analog signal;
a charge-sharing node;
filter-sampling means for collecting one or more samples of the analog signal, the filter-sampling means coupled to the input node;
a digital-to-analog converter including a capacitor array and a switch, the switch coupled between the input node and the capacitor array, the capacitor array coupled between the switch and the charge-sharing node, the digital-to-analog converter configured to collect, via the capacitor array and the switch, another sample of the analog signal; and
charge-sharing means for averaging multiple samples, the charge-sharing means coupled between the charge-sharing node and the filter-sampling means, the charge-sharing means configured to produce, at the charge-sharing node, an average sample of the analog signal based on the one or more samples and the other sample.

15. The apparatus of claim 14, wherein the filter-sampling means comprises:
capacitive means for storing the one or more samples; and
switch means for connecting or disconnecting the capacitive means to or from the input node.

16. The apparatus of claim 15, further comprising a processor coupled to the capacitive means, the processor configured to adjust a capacitance of the capacitive means based on a specified frequency of a jammer to cause the jammer to be attenuated at the charge-sharing node.

17. The apparatus of claim 15, wherein:
the capacitive means comprises weighted means for storing the one or more samples with one or more weights to collect one or more weighted samples;
the digital-to-analog converter is configured to store the other sample with another weight to collect another weighted sample, the other weight and the one or more weights comprising at least two different weights; and
the charge-sharing means is configured to produce, at the charge-sharing node, a weighted-average sample of the analog signal based on the one or more weighted samples and the other weighted sample.

18. The apparatus of claim 14, wherein:
the filter-sampling means is configured to collect the one or more samples of the analog signal based on one or more sampling-phase signals;
the digital-to-analog converter is configured to collect the other sample of the analog signal based on another sampling-phase signal;
the charge-sharing means is configured to connect the filter-sampling means to the charge-sharing node based on a charge-sharing phase signal;
the one or more sampling-phase signals and the other sampling-phase signal are indicative of the one or more samples and the other sample being collected at different times; and
the charge-sharing phase signal is indicative of the average sample being produced after the one or more samples and the other sample are collected.

19. The apparatus of claim 14, further comprising:
a comparator coupled to the charge-sharing node; and
a successive approximation register coupled between the comparator and the digital-to-analog converter,
wherein the digital-to-analog converter, the comparator, and the successive approximation register are jointly configured to:
perform a binary search to approximate the average sample at the charge-sharing node; and
produce, based on the binary search, a binary number that is representative of the average sample at the charge-sharing node.

20. The apparatus of claim 19, wherein the filter-sampling means is configured to produce the one or more samples during a portion of time that the binary search is performed on a previous average sample.

21. A method for alias rejection through charge sharing, the method comprising:
connecting a capacitor to an input node to collect a first sample of an analog signal at the input node;
connecting a capacitor array of a digital-to-analog converter to the input node to collect a second sample of the analog signal;
connecting, at a charge-sharing node, the capacitor to the digital-to-analog converter to produce an average voltage at the charge-sharing node, the average voltage representative of an average of the first sample and the second sample; and
generating a digital representation of the average voltage.

22. The method of claim 21, further comprising connecting another capacitor to the input node to collect a third sample of the analog signal,

wherein the connecting of the capacitor and the connecting of the digital-to-analog converter further comprise connecting the capacitor, the digital-to-analog converter, and the other capacitor together to produce the average voltage at the charge-sharing node, the average voltage representative of an average of the first sample, the second sample, and the third sample.

23. The method of claim 22, further comprising:

connecting another capacitor array of the digital-to-analog converter to the input node to collect a fourth sample of the analog signal; and

producing the average voltage at the charge-sharing node based on the connecting of the capacitor, the digital-to-analog converter, and the other capacitor together, the average voltage representative of an average of the first sample, the second sample, the third sample, and the fourth sample.

24. The method of claim 21, further comprising performing a binary search on a previous average voltage at the charge-sharing node,

wherein the connecting of the capacitor to the input node occurs during a portion of time that the binary search is performed.

25. The method of claim 21, wherein the average voltage is representative of a weighted average of the first sample and the second sample.

26. An apparatus comprising:
- an input node;
 - a charge-sharing node;
 - a comparator including an input and an output, the input of the comparator coupled to the charge-sharing node;
 - a successive approximation register coupled to the output of the comparator;
 - a filter-sampling network including a capacitor and a first switch, the first switch coupled between the input node and the capacitor, the filter-sampling network configured to connect or disconnect the capacitor to or from the input node via the first switch based on a first sampling-phase signal;
 - a digital-to-analog converter coupled to the successive approximation register, the digital-to-analog converter including a capacitor array and a second switch, the second switch coupled between the input node and the capacitor array, the capacitor array coupled between the second switch and the charge-sharing node, the digital-to-analog converter configured to connect or disconnect the capacitor array to or from the input node via the second switch based on a second sampling-phase signal; and
 - a charge-sharing switch coupled between the charge-sharing node and the capacitor, the charge-sharing switch configured to connect or disconnect the capacitor to or from the digital-to-analog converter based on a charge-sharing phase signal.

27. The apparatus of claim 26, further comprising:

another input node;

another charge-sharing node; and

another charge-sharing switch, wherein:

the comparator includes another input coupled to the other charge-sharing node;

the filter-sampling network includes another capacitor and a third switch, the third switch coupled between the other input node and the other capacitor, the other capacitor coupled between the third switch and the other charge-sharing switch, the filter-sampling network configured to connect or disconnect the other capacitor to or from the other input node via the third switch based on the first sampling-phase signal;

the digital-to-analog converter includes another capacitor array and a fourth switch, the fourth switch coupled between the other input node and the other capacitor array, the other capacitor array coupled between the fourth switch and the other charge-sharing node, the digital-to-analog converter configured to connect or disconnect the other capacitor array to or from the other input node via the fourth switch based on the second sampling-phase signal; and

the other charge-sharing switch is coupled between the other charge-sharing node and the other capacitor, the other charge-sharing switch configured to connect or disconnect the other capacitor to or from the digital-to-analog converter based on the charge-sharing phase signal.

28. The apparatus of claim 26, further comprising a processor, wherein:

the charge-sharing switch is configured to produce, based on a connection of the capacitor to the digital-to-analog converter, an average voltage at the charge-sharing node;

the successive approximation register is configured to generate a discrete voltage representative of the average voltage at the charge-sharing node; and

the processor is configured to accept the discrete voltage.

29. The apparatus of claim 28, wherein:

a capacitance of the capacitor differs from another capacitance of the capacitor array; and

the charge-sharing switch is configured to produce, based on the connection of the capacitor to the digital-to-analog converter, a weighted-average voltage as the average voltage at the charge-sharing node based on the capacitance and the other capacitance.

30. The apparatus of claim 26, wherein:

the filter-sampling network, the digital-to-analog converter, and the charge-sharing switch are jointly configured to implement a two-tap finite impulse response filter; and

a coefficient of the two-tap finite impulse response filter is based on a capacitance of the capacitor.