

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
28 May 2009 (28.05.2009)

PCT

(10) International Publication Number
WO 2009/067238 A1

(51) International Patent Classification:
H05K 7/10 (2006.01)

(21) International Application Number:
PCT/US2008/012981

(22) International Filing Date:
21 November 2008 (21.11.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/944,625 25 November 2007 (25.11.2007) US

(71) Applicant (for all designated States except US): **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, 94088-3453 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **SHAH, Sharad, M.** [US/US]; 6504 Pfeiffer Ranch Road, San Jose, CA 95120 (US).

(74) Agent: **DRAKE, Paul, S.**; Advanced Micro Devices, Inc., 7171 Southwest Parkway, Mail Stop B100.3.341, Austin, TX 78735 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: **MULTIPLE SIZE PACKAGE SOCKET**

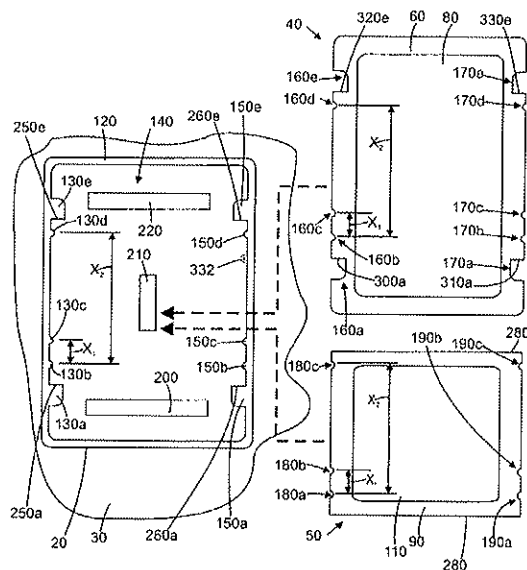


FIG. 3

(57) Abstract: Various sockets (20, 320) for multiple sizes of chip package substrates (40, 335) (50, 337) are disclosed. In one aspect, an apparatus is provided that includes a socket (20, 320) that has a peripheral wall (120, 340) defining an interior space (140, 350) adapted to receive either of a first semiconductor chip package substrate (40, 335) and a second semiconductor chip package substrate (50, 337). The first semiconductor chip package substrate (40, 335) has a first size and a first plurality of structural features (160a, 420a) and the second semiconductor chip package substrate (50, 337) has a second size different than the first size and a second plurality of structural features (180a, 490a). The socket (20, 320) has a third plurality of structural features (130a, 130b, 390a) operable to engage the structural features of either of semiconductor chip package substrates to selectively enable the first semiconductor chip package substrate (40, 335) to be located at a first preselected position in the interior space (140, 350) and the second semiconductor chip package substrate (50, 337) to be located at a second preselected position in the interior space (140, 350).