

ABSTRACT

A semiconductor device including a substrate, a wiring pattern in the substrate, a passivation layer on the substrate, the passivation layer and the substrate including a first recess penetrating a part of each of the passivation layer and the substrate and extending toward the wiring pattern, a post connected to the wiring pattern and including a first portion within the first recess and a second portion on the first portion and protruding from a top surface of the passivation layer, a signal bump including a seed layer on the post, a lower bump on the seed layer, and an upper bump on the lower bump, and a heat transfer bump apart from the signal bump, electrically insulated from the wiring pattern, and including another seed layer on the passivation layer, another lower bump on the another seed layer, and another upper bump on the another lower bump may be provided.

FIG. 2