What is claimed is:

1. A semiconductor package comprising:

a substrate;

a first die having a front side, a back side, and a plurality of through silicon interconnects, the first die being stacked onto the substrate; and

a second die having a front side, a back side, and a first plurality of conductive bumps formed at the back side of the second die, the second die being stacked onto the first die and having under-filled the first plurality of conductive bumps such that the first plurality of conductive bumps electrically communicate with the through silicon interconnects;

wherein a first mold material encapsulates the second die and the front side of the first die; and

a second mold material encapsulates the first die, the second die, and a plurality of solder interconnects.

2. The semiconductor package of claim 1, wherein each of the through silicon interconnects further comprises:

an end portion at the back side of the first die and a top portion at the front side of the first die;

a dielectric layer formed along internal walls of the through silicon interconnect;

a barrier metal layer formed over the dielectric layer;

a seed layer formed over the barrier metal layer; and

a metallic material filling space within the internal walls of the through silicon interconnect.

3. The semiconductor package of claim 2, further comprising:

a metallic layer and a passivation layer formed on the front side of the first die so as to be non-overlapping;

a metallic layer and a passivation layer formed on the back side of the first die so as to be non-overlapping;

a plurality of under bump metallization (UBM) pads formed on the metallic layer on the back side of the first die; and

a second plurality of conductive bumps formed on the UBM pads.