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# IMPROVED THIN AND HEAT RADIANT SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING

## BACKGROUND OF THE INVENTION

### TECHNICAL FIELD OF THE INVENTION

The present invention relates to a packaged semiconductor, a semiconductor package and a method for fabricating the package, and more particularly but not by way of limitation, to a thin semiconductor package having improvements in heat radiation and a method for manufacturing the same.

### HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal lead frames for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the lead frame are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a lead frame as the central supporting structure of such a package. A portion of the lead frame completely surrounded by the plastic encapsulant is internal to the package. Portions of the lead frame extend internally from the package and are then used to connect the package externally. More information relative to lead frame technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited

by R. Tummala and E. Rymaszewski and incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, consumer demand increases. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

Such conventional semiconductor packages are not without problems. Specifically, a typical semiconductor package is difficult to make slim because the thickness of the internal leads is equivalent to the thickness of the chip paddle. Further, the mounting of the semiconductor chip on the chip paddle increases the overall thickness of the package. The thickness is increased because of the input/output pads on the semiconductor chip mounted on the chip paddle are positioned at a higher level than the internal leads, thereby increasing the loop height of the conductive wires. The increased height may contribute to wire sweeping, caused by the encapsulation material during encapsulation.

In addition, mounting the semiconductor chip on a chip paddle having an externally exposed bottom surface has poorer heat radiation than having a direct externally exposed bottom surface of the semiconductor chip.

Finally, after the chip-mounting step and wire-bonding step are performed, the semiconductor package is encapsulated only after the leadframe is positioned on a mold. Thus, although the leadframe is in close contact with the lower mold die, some encapsulation material infiltrates through the interface between the leadframe and the lower mold die, resulting in the formation of so-called "flash". An extra de-flashing step must then generally be executed.

## BRIEF SUMMARY OF THE INVENTION

In one embodiment of the present invention, there is provided a semiconductor package comprising a semiconductor chip having an upper surface and a bottom surface. A plurality of input bond pads and output bond pads on the upper surface of the semiconductor chip and along the perimeter of the semiconductor chip are electrically connected to the semiconductor chip. A chip paddle may be provided which has a top surface, a side surface and a bottom surface. The chip paddle is bonded to the bottom surface of the semiconductor chip by an adhesive. The chip paddle has corners, a perimeter and a half-etched section at the lower edge of the chip paddle along the chip paddle perimeter.

A lead frame is provided having a plurality of tie bars. Each of the tie bars has a side surface and a bottom surface. The plurality of tie bars are connected to the corners of the chip paddle. The plurality of the tie bars externally extend from the chip paddle and have a half-etched section. A plurality of dam bars are provided on the lead frame help limit flow of encapsulation material on the leadframe.

A plurality of internal leads connect to the leadframe. Each of the leads has a side surface and a bottom surface. The leads are radially formed at regular intervals along and spaced apart from the perimeter to the chip paddle and extend towards the chip paddle. Each of the leads has a step shaped half-etched section facing the chip paddle.

A plurality of via conductive wires are electrically connected to and between the plurality of leads and the semiconductor chip. Encapsulating material encapsulates the semiconductor chip, conductive wires, chip paddle, and the leads to form a package body. The flow of the encapsulation material is limited by the dam bars formed on the leadframe. The dam bars also serve to stabilize the leads on the leadframe. After

encapsulation, the chip paddle, leads, and tie bars are externally exposed at respective bottom and side surfaces.

A ground ring may be provided on the leadframe having an upper surface and a lower surface. The conductive wires may be connected to the ground ring, which is exposed at the lower surface. The ground ring may further serve to function as a power ring.

## BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description when taken in conjunction with the accompanying Drawings wherein:

FIG.1A is a cross-section of a semiconductor package made in accordance with one embodiment of the present invention;

FIG. 1B is a cross-section of the semiconductor package of FIG. 1A with a ground ring included in the package;

FIG. 2A is a cross-section of an alternate embodiment of a semiconductor package made in accordance with the teachings of the present invention;

FIG. 2B is a cross-section of the semiconductor package of FIG. 2A with a ground ring included in the package;

FIG. 3 is a top plan view of a leadframe;

FIGS. 4-9 are side-elevation cross-sections of a preferred embodiment of the semiconductor package of the present invention from the initial to final construction; and

FIGS. 10-14 are side-elevation cross-sections of an alternate embodiment of the semiconductor package of the present invention from the initial to final construction.

## DETAILED DESCRIPTION OF THE INVENTION

Referring first to FIG. 1A and 1B, there is shown a cross sectional illustration of one embodiment of a semiconductor package 10 construed in accordance with the principles of the present invention. The semiconductor package 10 includes a corner 12 and bottom surface 15. The semiconductor package 10 further includes a semiconductor chip 20 having an upper surface 30, a perimeter 40 and a bottom surface 50. A plurality of input bond pads 60 and output bond pads 70 are disposed on the upper surface 30 of

the semiconductor chip 20. Conductive wires 75, including but not limited to gold or aluminum wires, electrically connect the semiconductor chip 20 to the respective input bond pads 60 or output bond pads 70.

In an alternate embodiment best seen in FIG. 2A and 2B, a chip paddle 80 having a upper surface 90, a side surface 100 and a bottom surface 110 is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a perimeter 140 and may include a half-etched section 150. The half-etched section 150 is located at a lower edge 160 of the chip paddle 80.

Referring now to FIG. 3, a leadframe 170 is shown having a plurality of tie bars 180 and a side surface 190. The tie bars 180 are connected to the corners 130 of the chip paddle 80 and externally extend from the chip paddle 80. The leadframe 170 also includes a plurality of dam bars 220.

A plurality of leads 230 are connected to the leadframe 170 and have an upper surface 235, a side surface 240 and a bottom surface 250 (FIGS. 1A and 2A). In a first embodiment seen in FIGS. 1A and 1B, the leads 230 are radially formed at regular intervals along the semiconductor chip perimeter 40 and spaced apart from the perimeter 40 of the semiconductor chip 20. The leads 230 extend towards the semiconductor chip 20 and have a half-etched section 260 facing the semiconductor chip 20.

In an alternate embodiment best seen in FIGS. 2A and 2B, the leads 230 are radially formed at regular intervals along the chip paddle perimeter 140 and spaced apart from the perimeter 140 of the chip paddle 80. The leads 230 extend towards the chip paddle 80, such that each of the plurality of leads 230 has a half-etched section 260 facing the chip paddle 80.

Referring back to FIGS. 1B and 2B, there is shown a ground ring 262 formed in the semiconductor package 10. The ground ring 262 is positioned between the semiconductor chip 20 and the plurality of leads 230, and may be interchangeably used as a power ring should circumstances require. Conductive wires 75 can connect the ground ring 262 to the respective input bond pads 60 or output bond pads 70, depending on the application. As seen in FIG. 1B, the upper surface 264 of the ground ring 262 is planar with the upper surface 30 of the semiconductor chip 20 and the upper surface 235 of the leads 230. However, as seen in FIG. 2B, the upper surface 264 of the ground ring 262 may be planar with the upper surface of the chip paddle 80 to minimize package

thickness. Likewise, the upper surface 235 of the leads 230 is planar with the upper surface 30 of the semiconductor chip 20 (FIGS. 1A and 1B) to minimize package thickness. In the alternate embodiments shown in FIGS. 2A and 2B, the upper surface 235 of the leads 230 is planar with the upper surface 90 of the chip paddle 80 to reduce package thickness.

Referring generally now to FIGS. 1A and 3, the semiconductor chip 20 and leads 230 are partially encapsulated with an encapsulation material 280 to form a semiconductor package body in which the semiconductor chip 20 and leads 230 are exposed directly to the outside at their respective bottom surfaces 50, 250. In the alternate embodiment shown in FIG. 2A and 2B, the chip paddle 80 is also encapsulated by the encapsulation material 280. In this alternate embodiment, the bottom surfaces 250, 110 of the leads 230 and chip paddle 80 are directly exposed to the outside. Likewise, for the embodiments shown in FIGS. 1B and 2B, the leads 230, semiconductor chip 20, and ground rings 262 are partially encapsulated to form a semiconductor package body in which the bottom surface 266 of the ground ring 262 is also exposed to the outside of the semiconductor package body.

Referring now to FIGS. 1 through 3 in general, dam bars 220 limit the flow of the encapsulation material 280 on the leadframe 170 and provide stability to the leads 230 on the leadframe 170. In the respective embodiment during encapsulation, the chip paddle 80, leads 230, and tie bars 180 may be externally exposed at peripheral side and bottom surfaces. The externally exposed portions of chip paddle 80, leads 230, and tie bars 180 may, but do no necessarily have to be, electroplated with corrosion-minimizing materials such as but not limited to, tin lead, tin, gold, nickel palladium, tin bismuth, or any other similar material known in the art. The respective half-etched sections 150, 260 of the chip paddle 80 and leads 230 are provided to increase the bonding strength of the encapsulation material 280 in the semiconductor package 10. It is contemplated that the respective half-etched sections 150, 260 may be eliminated without departing from the scope and spirit of this invention.

Referring now to FIGS. 4-9 in general, there is shown a cross-section of the semiconductor package 10 of FIG. 1A. It is to be recognized that the method for constructing the semiconductor package 10 of FIG. 1A may be used for constructing the embodiment shown in FIG. 1B without departing from the principles of this invention.

The leadframe having leads 230 and a space 290 large enough to accommodate a semiconductor chip 20, is first placed upon an adhesive tape 300. Next, a semiconductor chip 20 is fixed to the adhesive tape 300 within the space 290 as best seen in FIG. 5. The semiconductor chip 20 and the leads 230 are pressurized downwardly onto the tape 300 at a suitable temperature to make the tape 300 firmly adhere to the semiconductor chip 20 and leads 230.

As shown in FIG. 6, the input bond pads 60 and output bond pads 70 of the semiconductor chip 20 are next electrically connected to the leads 230 via conductive wires 75. Upper surface 235 of leads 230 may, but do not necessarily have to be, electroplated with a material that enhances electrical conductivity such as, for example, gold or silver. Typically, the conductive wires 75 are connected via an automated process, but may be connected in any alternate method in the industry.

The semiconductor chip 20, conductive wires 75, and leads 230 are then at least partially encapsulated with the encapsulation material 280, which may be an epoxy molding compound or a liquid encapsulation material, thereby forming a semiconductor package 10 as seen in FIG. 7. Referring to FIG. 8, the adhesive tape 300 is next removed from the bottom surface 15 of the semiconductor package 10. The leads 230 are next severed from the leadframe (not shown) by cutting through the dam bars (not shown) or neighboring areas of the semiconductor package 10 best seen in FIG. 9 as a singulation step. It is to be noted that this singulation step may occur before the adhesive tape 300 is removed.

After formation of the semiconductor package 10, a marking process (not shown) may be carried out by the use of ink or lasers. The removal of the adhesive tape 300 allows the semiconductor chip 20 and leads 230 to be exposed to the outside, thereby improving heat radiation. By adhering the adhesive tape 300 to the bottom surface 15 of the semiconductor package 10, which includes bottom surfaces 50, 250 of the semiconductor chip 20 and leads 230, flashes, which are typically formed during the molding process are not generated, thereby eliminating or reducing any further deflashing steps.

After the removal of the adhesive tape 300, a predetermined thickness of solder (not shown) may be plated over the bottom surface 250 of the of the leads 230 to allow easy union of the semiconductor package 10 with a motherboard (not shown).

Referring now generally to FIGS. 10-14, there are shown cross-sections of the semiconductor package 10 of FIG. 2A during various stages of construction. It is to be recognized that the method for constructing the semiconductor package 10 of FIG. 2A may be used for constructing the embodiment shown in FIG. 2B without departing from the principles of this invention. The leadframe (not shown) having leads 230 and a chip paddle 80 is first placed upon an adhesive tape 300 best seen in FIG. 10. The chip paddle 80 and the leads 230 are pressurized downwardly onto the tape 300 at a suitable temperature to make the tape 300 firmly adhere to the chip paddle 80 and leads 230.

As shown in FIG. 11, the semiconductor chip 20 is bonded to the upper surface 90 of the chip paddle 80 via an adhesive 120. The input bond pads 60 and output bond pads 70 of the semiconductor chip 20 are next electrically connected to the leads 230 via conductive wires 75. Upper surfaces 235 of leads 230 may, but do not necessarily have to be, electroplated with a material that enhances electrical conductivity such as, for example, gold or silver. Typically, the conductive wires 75 are connected via an automated process, but may also be connected in any alternate method in the industry.

As illustrated in FIG. 12, the semiconductor chip 20, chip paddle 80, conductive wires 75, and leads 230 are then at least partially encapsulated with the encapsulation material 280, which may be thermoplastics or thermoset resins, with thermoset resins including, for example, silicones, phenolics, and epoxies. The encapsulation material 280 forms a semiconductor package 10.

Referring to FIG. 13, the adhesive tape 300 is next removed from the bottom surface 15 of the semiconductor package 10. The leads 230 are next severed from the leadframe (not shown) by cutting through the dam bars (not shown) or neighboring areas of the semiconductor package 10 best seen in FIG. 14 in a singulation step. It is noted that this singulation step may occur before the adhesive tape 300 is removed.

Once the semiconductor package 10 is formed, a marking process (not shown) may be carried out by the use of ink or lasers. The removal of the adhesive tape 300 allows the chip paddle 80 and leads 230 to be exposed to the outside, thereby improving heat radiation. By adhering the adhesive tape 300 to the bottom surfaces 110, 250 of the chip paddle 80 and leads 230, respectively, flashes, which are typically formed during the molding process, are not generated, thereby eliminating or reducing any further deflashing steps. Bottom surfaces 110, 250 of the chip paddle 80 and leads 230, may be

electroplated with corrosion-minimizing materials such as, but not limited to, tin lead, tin, gold, nickel palladium, tin bismuth, or other similar materials known in the art.

After the removal of the tape 300, a predetermined thickness of solder (not shown) may be plated over the bottom surface 250 of the of the leads 230 to allow easy union of the semiconductor package 10 with a motherboard (not shown).

In such a semiconductor package as described and shown in FIGS. 1A and 1B, the bottom surface 15 of the semiconductor package 10 is in the same plane as the bottom surface 250 of the leads 230, so that the semiconductor package 10 is thin by limiting the height level of the conductive wires 75. In addition, the direct exposure of the semiconductor chip 20 provides for higher thermal radiation.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein:

| Attorney Docket No. | Title of Application | First Named Inventor |
|---|---|---|
| 09/687,331 | Lead Frame for Semiconductor Package and Mold for Molding the Same | Young Suk Chung |
| 09/687,532 | Method for Making a Semiconductor Package Having Improved Defect Testing and Increased Production Yield | Tae Heon Lee |
| 09/687,876 | Near Chip Size Semiconductor Package | Sean Timothy Crowley |
| 09/687,536 | End Grind Array Semiconductor Package | Jae Hun Ku |
| 09/687,048 | Leadframe and Semiconductor Package with Improved Solder Joint Strength | Tae Heon Lee |
| 09/687,585 | Semiconductor Package Having Reduced Thickness | Tae Heon Lee |
| 09/687,541 | Semiconductor Package Leadframe Assembly and Method of Manufacture | Young Suk Chung |
| 09/687,049 | Semiconductor Package and Method Thereof | Young Suk Chung |

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.

What Is Claimed Is:

1. A packaged semiconductor, comprising:

a semiconductor chip having a planar upper surface, a perimeter and a bottom surface;

a plurality of input bond pads on the planar upper surface of said semiconductor chip along the perimeter and electrically connected to said semiconductor chip;

a plurality of output bond pads on the planar upper surface along the perimeter of said semiconductor chip and electrically connected to said semiconductor chip;

a leadframe having a plurality of tie bars, said tie bars having a side surface and a bottom surface, said leadframe having a plurality of dam bars;

a plurality of internal leads connected to said leadframe, said plurality of internal leads having a side surface and a bottom surface, said plurality of internal leads being radially formed at regular intervals along and spaced apart from said perimeter of said semiconductor chip and extending towards said semiconductor chip, each of said plurality of internal leads having a half-etched section facing said semiconductor chip, each of said plurality of leads having an upper surface in the plane of said upper surface of said semiconductor chip;

a plurality of conductive wires for electrically connecting to said plurality of internal leads and to said semiconductor chip;

encapsulant material encapsulating said semiconductor chip, said plurality of conductive wires, and said plurality of internal leads to form a package body, wherein flow of said encapsulant material is limited by said plurality of dam bars formed on said leadframe; and

wherein said semiconductor chip, said plurality of internal leads and said plurality of tie bars are externally exposed at respective side and bottom surface.

2. The semiconductor package of claim 1, further comprising

a chip paddle connected to said leadframe, said chip paddle having a top surface, a side surface and a bottom surface, said chip paddle bonded to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

3. The semiconductor package of claim 2, wherein each of said plurality of tie bars are connected to said corners of said chip paddle.

4. The semiconductor package of claim 3, wherein each of said plurality of tie bars has a half-etched section, and whereas each of said plurality of tie bars externally extend from said chip paddle.

5. A packaged semiconductor, comprising:

a leadframe having a plurality of tie bars, said tie bars having a side surface and a bottom surface, said leadframe having a plurality of dam bars and a space for receiving a semiconductor chip;

a plurality of internal leads connected to said leadframe, said plurality of internal leads having a side surface and a bottom surface, said plurality of internal leads being radially formed at regular intervals along and spaced apart from said perimeter of said semiconductor chip and extending towards said semiconductor chip, each of said plurality of internal leads having a half-etched section facing said semiconductor chip, each of said plurality of leads having an upper surface in the plane of said upper surface of said semiconductor chip;

a plurality of conductive wires for electrically connecting to said plurality of internal leads and to said semiconductor chip;

encapsulant material encapsulating said semiconductor chip, said plurality of conductive wires, and said plurality of internal leads to form a package body, wherein flow of said encapsulant material is limited by said plurality of dam bars formed on said leadframe; and

wherein said semiconductor chip, said plurality of internal leads and said plurality of tie bars are externally exposed at respective side and bottom surface.

6. The semiconductor package of claim 5, further comprising:

a semiconductor chip having a planar upper surface, a perimeter and a bottom surface secured into said space on said leadframe.

7. The semiconductor package of claim 6, further comprising:

a plurality of input bond pads on the planar upper surface of said semiconductor chip along the perimeter and electrically connected to said semiconductor chip; and

a plurality of output bond pads on the planar upper surface along the perimeter of said semiconductor chip and electrically connected to said semiconductor chip;

8. The semiconductor package of claim 7, further comprising

a chip paddle connected to said leadframe, said chip paddle having a top surface, a side surface and a bottom surface, said chip paddle bonded to said bottom surface of said semiconductor chip by an adhesive, said chip paddle having corners, a perimeter and a half-etched section at a lower edge of said chip paddle along said chip paddle perimeter.

9. The semiconductor package of claim 8, wherein each of said plurality of tie bars are connected to said corners of said chip paddle.

10. The semiconductor package of claim 9, wherein each of said plurality of tie bars has a half-etched section, and whereas each of said plurality of tie bars externally extend from said chip paddle.

11. A method for making a semiconductor package, comprising the steps of:

placing a leadframe having a plurality of leads and a space for accommodating a semiconductor chip on an adhesive tape, said plurality of leads having a bottom surface;

affixing a semiconductor chip having a bottom surface, input bond pads and output bond pads within said space on said leadframe;

pressurizing said leadframe and said semiconductor chip downwardly onto said tape;

electrically connecting said input bond pads and said output bond pads of said semiconductor chip to said leads via wires;

encapsulating said semiconductor chip, said wires, and said leads by an encapsulant material to form a package body;

removing said adhesive tape from said package body while leaving said bottom surface of said leads and said bottom surface of said semiconductor chip externally exposed; and

cutting said package from said leadframe.

12. The method as in claim 11, wherein the steps are performed sequentially.

13. A method for making a packaged semiconductor, comprising the steps of:

placing a leadframe having a plurality of leads, a ground ring having a bottom surface, and a space for accommodating a semiconductor chip on an adhesive tape, said plurality of leads having a bottom surface;

affixing a semiconductor chip having a bottom surface, input bond pads and output bond pads within said space on said leadframe;

electrically connecting said input bond pads and said output bond pads of said semiconductor chip to said leads via wires;

encapsulating said semiconductor chip, said ground ring, said wires, and said leads by an encapsulant material to form a package body;

removing said adhesive tape from said package body while leaving said bottom surface of said leads, said bottom surface of said ground ring, and said bottom surface of said semiconductor chip externally exposed; and

cutting said package from said leadframe.

14. The method as in claim 13, wherein the steps are performed sequentially.

15. A method for making a packaged semiconductor, comprising the steps of:

placing a leadframe having a chip paddle having a bottom surface and a plurality of leads on an adhesive tape, said plurality of leads having a bottom surface;

affixing a semiconductor chip having a bottom surface, input bond pads and output bond pads onto said chip paddle via an adhesive;

electrically connecting said input bond pads and said output bond pads of said semiconductor chip to said leads via wires;

encapsulating said semiconductor chip, said wires, and said leads by an encapsulant material to form a package body;

removing said adhesive tape from said package body while leaving said bottom surface of said leads and said bottom surface of said semiconductor chip externally exposed; and

cutting said package from said leadframe.

16. The method as in claim 15, wherein the steps are performed sequentially.

17. The packaged semiconductor of claim 1, wherein said leadframe further comprises a ground ring having a bottom surface.

18. The packaged semiconductor of claim 17, wherein said bottom surface of said ground ring is externally exposed.

19. The semiconductor package of claim 5, wherein said leadframe further comprises a ground ring having a bottom surface.

20. The packaged semiconductor of claim 19, wherein said bottom surface of said ground ring is externally exposed.