What is claimed is:

1. A memory device, comprising:

a peripheral circuit region including a ~~first substrate and circuit elements on the first substrate, the circuit elements including a~~ row decoder and a page buffer; and

a cell ~~array~~ region including a plurality of wordlines stacked to each other, a plurality of channel structures penetrating the plurality of wordlines, and a plurality of cell contacts connected to the plurality of wordlines, the plurality of cell contacts are disposed in a first cell contact region and a second cell contact region,

wherein the first cell contact region and the second cell contact region are disposed on both sides of the plurality of channel structures, in a first direction,

~~wordlines, stacked on a second substrate on the peripheral circuit region, and~~

~~channel structures extending in a direction perpendicular to an upper surface of the second substrate and penetrating the wordlines; and~~

~~a~~ the cell ~~contact~~ region and the peripheral circuit region are stacked in a vertical direction in which the plurality of channel structures are extended~~including cell contacts connected to the wordlines and on both sides of the cell array region in a first direction parallel to the upper surface of the second substrate, the cell contacts including a first cell contact region and a second cell contact region, the first and second cell contact regions having different lengths to each other in the first direction~~,

~~wherein~~ each of the first cell contact region and the second cell contact region~~s includes~~ has a plurality of first pads and a plurality of second pads,

~~first pads having different lengths than each other~~ in the first direction, a length of each of the plurality of first pads is shorter than a length of each of the plurality of second pads, and

~~second pads different from the first pads,~~

~~the cell contacts are connected to the wordlines in the first pads, and~~

an area of at least one of the plurality of ~~the number of the~~ second pads included in the first cell contact region is greater than an area of at least one of the plurality of ~~the number of the~~ second pads included in the second cell contact region.

2. The memory device of claim 1, wherein~~, in the first direction,~~ a length of the first cell contact ~~region~~ is ~~greater~~ longer than a length of the second cell contact, in the first direction ~~region~~.

3. The memory device of claim 1 ~~or claim 2~~, wherein the row decoder includes a plurality of first pass elements and a plurality of second elements connected to the plurality of wordlines,

a portion of the plurality of wordlines are connected to the plurality of first pass elements and a remainder of the plurality of wordlines are connected to the plurality of second elements, and

each of the plurality of first pass elements is connected to one of the portion of the plurality of wordiness and each of the plurality of second pass elements is connected to one of the remainder of the plurality of wordlines~~a sum of areas of the first pads and the second pads included in the first cell contact region is greater than a sum of areas of the first pads and the second pads included in the second cell contact region~~.

4. The memory device of ~~any one of~~ claim~~s 1 to~~ 3, wherein the plurality of second pass elements are disposed between the plurality of first pass elements, in the first direction~~a sum of the number of the first pads and the number of the second pads included in the first cell contact region is greater than a sum of the number of the first pads and the number of the second pads included in the second cell contact region~~.

5. The memory device of ~~any one of~~ claim~~s 1 to 4~~3, wherein the number of the portion of the plurality of wordlines is greater than the number of the remainder of the plurality of wordlines~~the row decoder includes first pass elements and second pass elements connected to the wordlines, and~~

~~each of the first pass elements is connected to one of the wordlines, and each of the second pass elements is connected to two or more wordlines among the wordlines~~.

6. The memory device of claim ~~5~~3, wherein the cell region includes a first cell region and a second cell region adjacent to each other, in the first direction, and

at least one of the plurality of second pass elements is disposed between the first cell region and the second cell region, in the first direction~~the two or more wordlines, connected to one of the second pass elements, are at the same height in a direction perpendicular to the upper surface of the second substrate~~.

7. The memory device of claim ~~5 or claim 6~~3, wherein the cell region includes a first cell region and a second cell region adjacent to each other, in the first direction, and

at least one of the plurality of second pass elements is disposed under a boundary region between the first cell region and the second cell region in the first direction~~at least one of the second pass elements has an area larger than or equal to an area of each of the first pass elements~~.

8. The memory device of ~~any one of~~ claim~~s 5 to~~ 7, wherein the plurality of wordlines are not disposed over the at least one of the plurality of second pass element, in the vertical direction~~the number of the wordlines connected to the first pass elements is greater than the number of the wordlines connected to the second pass elements~~.

9. The memory device of ~~any one of~~ claim~~s 5 to 8~~7, wherein the at least one of the plurality of second pass element is connected to two or more of the reminder of the plurality of wordlines, by at least one vertical via extending in the vertical direction, and

in the vertical direction, a length of the at least one vertical via is longer than a length of each of the plurality of cell contacts~~each of the wordlines connected to the first pass elements has resistance higher than resistance of each of the wordlines connected to the second pass elements~~.

10. The memory device of ~~any one of~~ claim~~s 5 to~~ 9, wherein, in the vertical direction, the length of the at least one vertical via is longer than a length of each of the plurality of channel structures ~~each of the wordlines connected to the first pass elements has a thickness different from a thickness of each of the wordlines connected to the second pass elements~~.

11. The memory device of ~~any one of~~ claim~~s 5 to 10~~1, wherein the number of the plurality of second pads included in the first cell contact region is greater than the number of the plurality of second pads included in the second cell contact region~~each of the channel structures includes a lower channel structure extending from the upper surface of the second substrate, and an upper channel structure extending from the lower channel structure, and~~

~~the wordlines include lower wordlines and upper wordlines, the lower channel structure penetrates through the lower wordlines and the upper channel structure penetrates through the upper wordlines, and at least one of the lower wordlines is connected to at least one of the second pass elements~~.

12. ~~The~~ A memory device ~~of claim 11, wherein the upper wordlines are connected to the first pass elements~~, comprising:

a plurality of cell regions, each of the plurality of cell regions including a plurality of wordlines stacked in a vertical direction and extending in a first direction and a plurality of channel structures extending in the vertical direction and penetrating the plurality of wordlines; and

a peripheral circuit region including a plurality of pass elements, and disposed under the plurality of cell regions in the vertical direction,

wherein each of the plurality of cell regions includes a first cell region and a second cell region arranged in the first direction,

at least one pass element of the plurality of pass elements is disposed in a boundary region between the first cell region and the second cell region, and is connected to at least one vertical via crossing a boundary between the peripheral circuit region and the plurality of cell

regions, and

the at least one vertical via is commonly connected to at least one of the plurality of wordlines included in the first cell region and at least one of the plurality of wordiness included in the second cell region.

13. The memory device of ~~claim 11 or~~ claim 12, wherein the at least one of the plurality of wordlines included in the first cell region and the at least one of the plurality of wordiness included in the second cell region are disposed at the same height, in the vertical direction~~at least a portion of the upper wordlines has a thickness higher than a thickness of the lower wordlines~~.

14. The memory device of ~~any one of~~ claim~~s 11 to 13~~12, wherein the first cell region and the second region have a symmetrical structure, with respect to the boundary region~~the wordlines include at least one dummy wordline between the lower wordlines and the upper wordlines and adjacent to a boundary between the lower channel structure and the upper channel structure~~.

15. The memory device of ~~any one of~~ claim~~s 1 to 14~~12, wherein each of the first cell region and the second region includes a cell array region in which the plurality of channel structures are disposed and a first cell contact region and a second cell contact region disposed on both sides of the cell array region in the first direction, and

in the first direction, the boundary region is disposed between the second cell contact region of the first cell region and the second cell contact region of the second cell region~~the cell contact region includes upper interconnection lines, connected to the cell contacts, and vertical vias connected to the upper interconnection lines and extending to the peripheral circuit region in the direction perpendicular to the upper surface of the second substrate~~.

16. The memory device of claim 15, wherein a length of the second cell contact region is shorter than a length of the first cell contact region, in the first direction~~the vertical vias penetrate through at least one of the second pads~~.

17. The memory device of claim ~~16~~15, wherein each the at least one of the plurality of wordlines included in the first cell region and the at least one of the plurality of wordlines included in the second cell region is commonly connected to the at least one vertical via by cell contacts disposed in the second cell contact region~~the second substrate includes a plurality of second substrates, and~~

~~at least one of the vertical vias is between the second substrates~~.

~~18. A memory device comprising:~~

~~a peripheral circuit region including pass elements on a first substrate; and~~

~~a plurality of cell regions on a second substrate above the peripheral circuit region, each of the plurality of cell regions including at least one memory block,~~

~~wherein each of the plurality of cell regions includes~~

~~a cell array region, in which a plurality of wordlines are connected to the pass elements and a plurality of channel structures penetrating through the wordlines, and~~

~~a cell connect region, in which the wordlines extending from the cell array region are connected to a plurality of cell contacts, and~~

~~at least one of the pass elements is commonly connected to a pair of wordlines included in a pair of cell regions, adjacent to each other among the cell regions, and the pair of wordlines are on the same level from an upper surface of the second substrate.~~

~~19. The memory device of claim 18, wherein each of the cell regions includes a first cell contact region on a first side of the cell array region, and a second cell contact region on a second side of the cell array region, opposing the first side, and~~

an area of the first cell contact region covering the upper surface of the second substrate is larger than an area of the second cell contact region covering the upper surface of the second substrate.

20. A memory device comprising:

a peripheral circuit region including pass elements; and

a plurality of cell regions, each of the plurality of cell regions including a cell array region including

wordlines stacked on a substrate above the peripheral circuit region and

channel structures penetrating through the wordlines;

wherein each of the plurality of the cell regions include a first cell region and a second cell region, adjacent to each other in a first direction parallel to an upper surface of the substrate, and a third cell region and a fourth cell region adjacent to each other in the first direction, and

a distance between the cell array region of the first cell region and the cell array region of the second cell region is different from a distance between the cell array region of the third cell region and the cell array region of the fourth cell region.