

HIGH RESOLUTION SKEW DETECTION

APPARATUS AND METHOD

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FIELD OF THE INVENTION

The invention relates generally to automatic test equipment for testing semiconductor devices, and more particularly a high resolution skew detection system and method for timing calibration and/or timing verification on the equipment.

BACKGROUND OF THE INVENTION

The manufacture of semiconductor devices involves numerous processes that are carefully controlled to maximize throughput and device yields. One of the more important process steps employs automatic test equipment to confirm device functionality. The tests are often performed both at the wafer and packaged-device levels. Generally, the testing procedure includes the application and capture of tester waveforms to and from each device along tester channels, and a determination of whether the captured signals match expected values. The tester channels employ transmission lines to couple the tester to the DUT pins.

In order to successfully test a device-under-test (DUT), signals that are applied to the device pins along each transmission line must arrive at precise timings relative to each other. The transmission lines that route the tester signals to the DUT typically vary in length, contributing small but important relative delays in the propagation time for each signal. Consequently, in order to accurately control the signal timings, the delays for each channel generally must be known and compensated for prior to test in a timing calibration procedure.

One of the primary ways of determining the relative signal delays between tester channels involves driving signals along each channel transmission line and measuring the relative edge-to-edge timing variation, or skew. Once the skews are known, the timings for each signal can be manipulated to align the edges as required to achieve the desired timing accuracy at the DUT pins.

Many techniques are known in the art for measuring the relative skews between propagating tester signals. For example, one of the more popular methods for detecting skew, commonly referred to as the Vernier calibration technique, employs a D-flip-flop-based latching comparator. A target signal is input to the data port of the

flip-flop and a reference signal applied to the strobe port. Using this technique, the reference signal simply latches a high or low value based on the skew of the two signals. By using a reference oscillator with a slightly differing frequency or time position, enough information can be gathered from the output to determine the relative magnitude of the skew.

Another flip-flop-based technique for detecting skew employs an XOR gate coupled with a plurality of D-flip-flops, such as the Model AD9901 Phase/Frequency Discriminator available from Analog Devices Corporation. This construction produces a signal with a varying pulsewidth based on the skew magnitude as well as the signal skew polarity. When used in combination with a charge pump, this circuit can also provide a DC signal representing the level of skew detected.

Similar to the XOR-charge pump configuration described above, another skew detection scheme, proposed by Feldman, utilizes a Set-Reset (SR) flip-flop with a charge pump disposed at the output. The SR flip-flop is configured such that the reference signal clocks the flip-flop while the target signal feeds the SET port. The DATA port is held low throughout circuit operation. This particular circuit has an added benefit in that most of the voltage dependent elements such as current sources, switches, capacitors, etc. have a relatively constant voltage applied to them. This minimizes non-linearity problems.

While the flip-flop-based skew detection schemes described above are beneficial for their intended applications, they all have limited linear ranges because of metastability, or jitter. This is an inherent characteristic of flip-flops as they produce valid UP and DOWN signals. As a result, at higher frequencies of operation, the resolution of the detector degrades to the point at signal-signal skews are undetectable.

In an effort to avoid the metastability problems inherent in flip-flop-based skew detectors, a proposal by Otsuji utilizes a time-to-voltage conversion technique suitable for implementation on an integrated circuit. The technique employs a level converter block for receiving and normalizing a reference signal and a tester signal from one channel of a semiconductor tester. The outputs from the level converter block are coupled to the inputs of a differential amplifier. The amplifier produces a pulse having an amplitude proportional to the relative skew between the reference signal and the tester signal. The pulse is fed to a complementary D-latch, while strobe circuitry generates a strobe synchronously with the rising edges of one of the input signals. The output levels of the Q and Q/ ports are fixed to complementary logic levels according to the skew polarity.

While this circuit has the benefit in that an in-phase skew can be successfully transformed into the differential voltage even for very small skews, no provisions are provided for out-of-phase skews. With the expanding implementation of differential tester channels in semiconductor testers, out-of-phase skew detection is becoming increasingly important.

The conventional skew detection configurations and techniques described above illustrate the limits in achieving timing calibration and verification accuracies. Equally important however is the undesirable duration of the conventional timing calibration and/or verification procedure. Typically, once a tester has completed its calibration, an independent verification apparatus is employed to confirm the accuracy thereof. Usually, a robotic probe disposed proximate the DUT separately steps through each channel in an effort to detect channel-to-channel skew. Unfortunately, with modern testers employing anywhere from three-thousand to six-thousand channels, the conventional data acquisition time for a robotic probe may take upwards of fourteen hours or more. This results in lost tester time for production purposes, and correspondingly lower overall throughput.

What is needed and heretofore unavailable is a high resolution skew detection circuit and method for use in a semiconductor tester that accurately detects very small skews and provides an output signal that allows for rapid timing calibration verification. The high resolution skew detection circuit and method of the present invention satisfies these needs.

SUMMARY OF THE INVENTION

The high resolution skew detection circuit and method of the present invention provides an accurate detection of both in-phase and out-of-phase signal skews without the undesirable effects of metastable jitter. Moreover, the invention enables high throughput in a production environment by allowing straightforward measurements on multiple channels and devices in parallel.

To realize the foregoing advantages, the invention in one form comprises a high resolution skew detector including multi-phase input circuitry. The input circuitry has a reference signal input and a skew signal input and is adapted for receiving in-phase and/or out of phase skew signals. In response to a control signal, the input circuitry is operative to pass or invert the skew signals. The detector also includes time-to-voltage conversion circuitry having respective first and second inputs for receiving the skewed and reference signals, and a differential amplifier for generating a relative skew signal. The relative skew signal represents the relative skew between the reference signal and the skew signal. Capture circuitry is coupled to the output of the time-to-voltage conversion circuitry for detecting the relative skew signal.

In another form, the invention comprises a skew detection circuit for measuring the relative skew between a plurality of propagating signals and a reference signal. The skew detection circuit includes a selector circuit having a plurality of inputs adapted for receiving the propagating signals and an output for selectively passing one of the plurality of signals for comparison with the reference signal. The skew detection circuit employs a high resolution skew detector including multi-phase input circuitry. The input circuitry has a reference signal input and a skew signal input and is adapted for receiving in-phase and/or out of phase skew signals. In response to a control signal, the input circuitry is operative to pass or invert the skew signals. The detector also includes time-to-voltage conversion circuitry having respective first and second inputs for receiving the skewed and reference signals, and a differential amplifier for generating a relative skew signal. The relative skew signal represents the relative skew between the reference signal and the skew signal. Capture circuitry is coupled to the output of the time-to-voltage conversion circuitry for detecting the relative skew signal.

In yet another form, the invention comprises a method of determining the relative skew between a plurality of tester channels to compensate for signal propagation delays. The method includes the steps of generating tester signals along the plurality of channels; coupling the channels to a high resolution skew detection

circuit; supplying a reference signal to the skew detection circuit; and selecting one of the tester signals for comparing against the reference signal on the skew detection circuit. The comparing step includes the steps of converting the relative time difference between an edge of the reference signal and an edge of the passed tester
5 signal to a voltage, and providing the voltage at an output for use as a measurement of the relative skew between the tester signal and the reference signal.

Other features and advantages of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following more detailed description and accompanying drawings in which

FIG. 1 is a partial block diagram of a semiconductor tester employing one
5 embodiment of the present invention;

FIG. 2 is a high level block diagram of the skew detection circuit shown in Figure 1;

FIG. 3 is a partial schematic of one embodiment of a selector circuit for use in the skew detection circuit of Figure 2;

10 FIG. 4 is a schematic of a high resolution skew detector according to one embodiment of the present invention; and

FIG. 5 is a timing diagram for the high resolution skew detector of Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Figure 1, a semiconductor tester 10 is shown coupled to a handling apparatus 12 that includes a device interface board (DIB) 14. The tester includes a testhead (not shown) that houses a plurality of pin electronics channel cards 18 for generating tester waveforms along a plurality of channels 20. The channels direct the waveforms to the input pins of one or more DUTs (not shown), and receive output waveforms from the DUT(s). The DIB includes one or more sockets 22 for electrically coupling the DUT pins to the tester channels, thereby providing a convenient tester-to-DUT signal interface.

In order to ensure that timing signals propagating along the channels arrive at the DUT pins within predefined accuracies, a plurality of high resolution skew detection circuits, generally designated 30, are employed. The skew detection circuits accurately measure both in-phase and out-of-phase channel-to-channel skews for timing calibration or verification purposes.

Referring more particularly to Figure 2, each skew detection circuit 30 takes the form of an application specific integrated circuit (ASIC). The ASIC includes bias inputs 32 and 34 for receiving Vdd and Vss signals, and first and second reference signal inputs 36 and 37 for receiving reference clock signals VREF1 and VREF2. Selector circuitry 40 is provided on the ASIC with inputs coupled to a plurality of tester channels, and outputs feeding a high resolution skew detector 50 for measuring signal-to-signal skews on the order of 1 picosecond.

Further referring to Figure 2, the selector circuitry 40 includes a pair of N:1 analog multiplexers 42 and 43 having inputs coupled to N (preferably twenty-four) tester channel transmission line outputs. An address decoder 49 responsive to multi-bit DC address signals provides respective control inputs to the multiplexers. The analog multiplexers allow a single ASIC to process several tester channels (in this example, twenty-four) to maximize tester throughput during the calibration and/or verification process.

The inventors have discovered that the construction of the analog multiplexers plays an important role in successfully maximizing the number of selectable inputs for the HRSD while maintaining acceptable signal quality. While conventionally, a parallel array of N number of MOS gates might be employed to carry out the multiplexing function, such a scheme often ties the gate outputs in parallel to produce a single output, thereby defining an N:1 device. Unfortunately, for high accuracy applications, the lumped output capacitance of all the gates in the conventional

configurations often creates undesirable transients that affect the output signal integrity.

In an effort to minimize the transient effects noted above, and with particular reference to Figure 3, the analog multiplexers 42 and 43 each preferably include
5 twenty-four MOS transmission gate inputs V1 - V24, distributed in such a manner as to minimize capacitively coupled input-output transients. The input gates are grouped into four parallel arrays A1 - A4, with each array having a single output O1 - O4. Each output is fed to a series-connected output transmission gate OG1 - OG4. To
10 channel the undesirable transient feedthrough signals to ground, respective grounded feedthrough transmission gates FT1 - FT4 shunt the signal output paths. The outputs of the output transmission gates are tied and provide a high fidelity output signal Vout to the input of the HRSD 50.

Referring back to Figure 2, the high resolution skew detector (HRSD) 50 generally employs multi-phase input circuitry 56 for receiving the tester signal and the
15 reference signal, and time-to-voltage conversion circuitry 60 for generating an output signal representative of the relative skew between the tester signal and the reference signal. Capture circuitry 70 is disposed at the output of the time-to-voltage conversion circuitry to enable the detection of the generated output signal. The input
20 circuitry and the time-to-voltage conversion circuitry define first and second signal paths 52 and 54 for the respective input signals. For purposes of clarity, only the first path will be described in detail below.

Referring more particularly now to Figure 4, the multi-phase input circuitry 56 for the first signal path 52 comprises a level voltage converter LVC1 (Fig. 2) for
25 receiving the input signal IN1 (the tester transmission line output signal from one channel) and reducing the input signal voltage swing to a level (such as 450 mV) more suitable for high-speed processing. The level converter includes a differential pair Q1, Q2 driven by a current source I1. The collector output of Q2 feeds an emitter follower Q3 that produces the reduced signal level, and provides an input to a Gilbert Inverter
30 INV1.

The Gilbert inverter INV1 includes a differential control input (FLIP, FLIP/) fed to respective first and second differential pairs Q7, Q8 and Q9, Q10. A third
35 differential pair Q11, Q12 couples to the emitters of the first and second differential pairs, and receives the level converted tester signal from the output of the level voltage converter LVC1 and a bias signal VBIAS. Disposed at the emitter node of the third differential pair is a current source I3. Respective resistors R5 and R6 establish the DC biasing conditions for the inverter as is well known in the art. The collectors

of the transistors Q7 and Q9 are tied to an output node that feeds the time-to-voltage conversion circuitry 60. The output of the circuit is responsive to the differential control signal FLIP, FLIP/ to either pass or invert the level converted tester input signal IN1. This conveniently provides for the measurement of in-phase and out-of-phase skews.

With further reference to Figure 4, the time-to-voltage conversion circuitry 60 includes a delay element 64 coupled to the output of the Gilbert inverter INV1, and a differential amplifier.

As alluded to above, the second signal path 54 includes level conversion circuitry LVC2 (transistors Q4 through Q6, and resistors R3 through R4) and a Gilbert inverter INV2 (transistors Q13 through Q18, current source I4, and resistors R8, R9) configured similar to that of the first path 52, and warrants no further description. However, the second signal path is sampled by the capture circuitry 70, at 62, (described below) to provide a self-clocking scheme that eliminates the need for additional clock circuitry.

The differential amplifier 66 includes another differential pair of transistors Q19 and Q20 driven by a current source I5, and receives the level converted and Gilbert inverted inputs to generate a differential signal having an amplitude proportional to the relative skew between the input signals IN1 and IN2. The differential signal output is fed to the input of the capture circuitry 70.

Further referring to Figures 2 and 4, the capture circuitry 70 includes a latch block 72 clocked by a strobe pulse produced by strobe circuitry 74. The latch block includes an input differential pair Q21, Q22 having inputs coupled to the differential outputs of the differential amplifier 66. A second differential pair Q24, Q25 includes respective inputs cross-coupled to the outputs of the input differential pair to effectively create a D-type latch. A pair of emitter followers Q27 and Q28 provide a differential buffered output OUT+, OUT-. A third differential pair Q23, Q26 drives (or sources current from) the first and second differential pairs, and includes a current source I6. The third differential pair activates in response to differential input signals from the strobe circuitry 74.

With continuing reference to Figure 4, the strobe circuitry 74 includes an inverter module that feeds an AND/NAND gate 76. The inverter module comprises a differential pair Q29, Q30 that generates an inverted output fed to an emitter follower Q31. The inverted output is coupled through a delay element 78 to an input of the AND/NAND gate. A non-inverted version of the input signal is fed to a second input of the AND/NAND gate.

The construction of the AND/NAND gate 76 is of conventional ECL design, and well known to those skilled in the art.

Referring back to Figure 1, the output of the latch block 72 is preferably fed through an output buffer 79 to a charge pump or low pass filter 80. The charge pump or low pass filter generates a DC output in response to the latch signal. In this way, an off-chip DC voltage can be produced and quickly directed to a timing calibration or verification controller (not shown) that acquires the skew data for analysis.

As noted previously, to take advantage of the convenient interface provided by the DIB, and eliminate the need for an expensive and slow-performing robotic probe, the skew detection circuit of the present invention 30 is preferably disposed in integrated circuit form and packaged similar to that of a DUT. However, for devices having more than sixteen I/O pins, the present invention may be modularized as required in order to process the additional inputs. For example, since the preferred HRSD circuit 30 adequately steps through twenty-four channels (corresponding to twenty-four DUT I/O pins), for DUTs having 64 I/Os, three HRSD circuits may be implemented in a single ASIC. Consequently, to set-up the tester for timing calibration or verification, the ASIC packages are merely plugged into the DUT sockets to provide a complete external timing calibration or verification for a parallel array of device locations up to and including the socket traces.

The operation of the present invention is best described with reference to Figures 1, 2, 4 and the timing diagram of Figure 5. As previously described, the skew detection circuit 30 is preferably implemented as an ASIC, for installation into the socket of a DUT loadboard. In parallel memory test applications, the loadboard may include anywhere from thirty-two to one-hundred-twenty-eight device locations for high throughput parallel testing. The unique ASIC implementation allows for the installation of thirty-two to one-hundred-twenty-eight HRSD ASICs to carry out tester timing calibration and/or timing verification.

For purposes of clarity, the following description of operation will focus on a timing verification application, with the understanding that the method described is equally applicable to performing an initial timing calibration. A timing verification is merely an independent confirmation, or checkout, of the tester signal timing to ensure that the previously performed calibration resulted in timings within the required tolerance.

Once the HRSD ASICs are installed in the loadboard 14, the tester generates a predetermined test waveform pattern simulating actual tester operation. This involves

the transmission of tester signals along the tester channels 20 to each of the ASIC signal inputs.

To detect and measure channel-to-channel skew, for instance between channel 1 and channels 2 through 16, tester signals along channel 1 are used as a signal reference IN2, while the remaining channels are sequentially passed through the selector 40 to the HRSD 50. The sequencing through the analog multiplexers 42 and 43 are regulated by the 4-bit DC address signals (controlled by a verification controller, not shown) that specify which channel signals the multiplexers should pass.

The selected tester signal IN1, and the reference signal (from channel 1) IN2, are then conditioned by the level voltage conversion circuitry LVC1 and LVC2 into approximately 450 mV signals. This reduces the logic swing levels, enabling faster circuit performance.

The respective level converted signals for IN1 and IN2 are then processed as necessary by the Gilbert inverters INV1 and INV2 so that out-of-phase as well as in-phase skews are detected and used as differential input signals to the differential amplifier 66. As shown in Figure 5, the differential amplifier produces an output signal pulse DATA having an amplitude proportional to the relative skew between IN1 and IN2. Of particular importance is the generation of the output (for at least the duration of the input signal risetimes) even for relatively minute skew levels on the order of one picosecond. This provides a tremendous advantage in successfully detecting and measuring such small timing parameters.

In order to maintain the detected amplifier output (representing the relative skew), the strobe circuitry 74 produces a one-shot clocking signal (a strobe pulse) CLK (Fig. 5) triggered by the rising edge of the reference signal input IN2. This self-timing feature results by sampling the reference signal IN2 at 62 (Fig. 4), and ANDing/NANDing the signal with an inverted version. The strobe clock CLK then causes the latch circuitry 72 to maintain or "latch" the data signal DATA for an extended duration, thereby generating easily detectable output signals OUT+ and OUT-.

The output signal pulse is then further processed through the charge pump or low-pass filter 80 to extract the DC signal component, and establish a readily processable off-chip skew signal for analysis by the timing verification controller. The generalized procedure above occurs simultaneously for all of the HRSD ASICs, and repeats after the reference channel signal is compared to all the other channels. A new channel then substitutes the previous reference channel, and the procedure

repeated. Once the verification is complete, the tester may then proceed with production testing of semiconductor devices.

Those skilled in the art will appreciate the many benefits and advantages afforded by the present invention. Of particular importance is the high resolution
5 detection ability for detecting both in-phase and out-of-phase skews. This provides a substantially improved measure of accuracy for detecting timing variations. This is extremely important for modern semiconductor testers that employ numerous differential channel configurations. Moreover, by implementing the unique selector circuitry, verification times are dramatically minimized, resulting in substantial cost
10 savings by maximizing the availability of the tester for production operations and correspondingly increasing throughput.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from
15 the spirit and scope of the invention.

WHAT IS CLAIMED IS:

1 1. A high resolution skew detector including:
2 multi-phase input circuitry having a reference signal input and a skew
3 signal input, said skew signal input adapted for receiving in-phase and/or out of phase
4 skew signals, said input circuitry operative to pass or invert said skew signals in
5 response to a control signal;
6 time-to-voltage conversion circuitry having respective first and second
7 inputs for receiving said skewed and reference signals, said time-to-voltage
8 conversion circuitry including a differential amplifier for generating a relative skew
9 signal representing the relative skew between said reference signal and said skew
10 signal; and
11 capture circuitry coupled to the output of said time-to-voltage
12 conversion circuitry for detecting said relative skew signal.

1 2. A high resolution skew detector according to claim 1 wherein said
2 multi-phase input circuitry further includes:
3 level conversion circuitry for receiving and conditioning said
4 respective skew and reference signals into respective level converted skew and
5 reference signals.

1 3. A high resolution skew detector according to claim 2 wherein said
2 multiphase input circuitry further comprises:
3 a first Gilbert inverter having a first input coupled to the output of said
4 level conversion circuitry and a second input responsive to a control signal to invert
5 said skew signal; and
6 a second Gilbert inverter having a third input for receiving said level
7 converted reference signal.
8

1 4. A high resolution skew detector according to claim 1 wherein said
2 capture circuitry comprises:
3 strobe circuitry coupled to said time-to-voltage conversion circuitry
4 and having a pulse generation circuit operative to produce a pulse of a predetermined
5 width; and

6 latch circuitry coupled to said differential amplifier output and
7 responsive to said strobe circuitry timing to latch a signal indicative of the relative
8 skew between said skew signal and said reference signal.
9

10 5. A high resolution skew detector according to claim 4 wherein said
11 produced pulse is synchronous with said reference signal.

1 6. A high resolution skew detector according to claim 4 wherein said
2 produced pulse is synchronous with said skew signal.

1 7. A high resolution skew detector according to claim 1 wherein said
2 reference signal input is coupled to a calibration signal source.

1 8. A high resolution skew detector according to claim 1 wherein:
2 said skew signal input is coupled to a first tester channel; and
3 said reference signal input is coupled to a second tester channel.

1 9. A high resolution skew detector according to claim 1 wherein:
2 said multi-phase input circuitry, said time-to-voltage conversion
3 circuitry, and said capture circuitry are disposed on an integrated circuit.

1 10. A high resolution skew detector according to claim 9 and further
2 including:
3 a signal converter disposed at the output of said capture circuitry and
4 having an output configured to provide an off-chip signal.

1 11. A high resolution skew detector according to claim 10 wherein:
2 said signal converter comprises a charge pump.

1 12. A high resolution skew detector according to claim 10 wherein:
2 said signal converter comprises a low-pass filter.

1 13. A skew detection circuit for measuring the relative skew between a
2 plurality of propagating signals and a reference signal, said skew detection circuit
3 including:

4 a selector circuit having a plurality of inputs adapted for receiving said
5 propagating signals and an output for selectively passing one of said plurality of
6 signals for comparison with said reference signal; and

7 a high resolution skew detector including
8 multi-phase input circuitry having a reference signal input and a
9 skew signal input, said skew signal input adapted for receiving in-phase and/or out of
10 phase skew signals, said input circuitry operative to pass or invert said skew signals in
11 response to a control signal;

12 time-to-voltage conversion circuitry having respective first and
13 second inputs for receiving said skewed and reference signals, said time-to-voltage
14 conversion circuitry including a differential amplifier for generating a relative skew
15 signal representing the relative skew between said reference signal and said skew
16 signal; and

17 capture circuitry coupled to the output of said time-to-voltage
18 conversion circuitry for detecting said relative skew signal.

1 14. A skew detection circuit according to claim 13 wherein:
2 said selector circuit comprises an analog multiplexer, and said plurality
3 of inputs comprise respective tester channels.

1 15. A skew detection circuit according to claim 14 wherein said analog
2 multiplexer comprises:

3 a plurality of input gates corresponding to a plurality of input signals,
4 said plurality of input gates arranged into an integral number of groups, each of said
5 groups comprising a predetermined number of said input gates configured in parallel
6 and having a common output;

7 a plurality of output transmission gates corresponding to the number of
8 said common outputs, each of said plurality of output transmission gates coupled in
9 series to said common outputs, and having respective output paths tied to form a
10 single multiplexer output; and

11 a plurality of feedthrough transmission gates corresponding to the
12 number of said common outputs, each of said plurality of feedthrough transmission
13 gates having an input coupled to said common output and a grounded output.

1 16. A skew detection circuit according to claim 13 wherein:

said selector circuit and said high resolution skew detector are disposed on an integrated circuit.

17. A method of determining the relative skew between a plurality of tester channels to compensate for signal propagation delays, said method including the steps of:

- generating tester signals along said plurality of channels;
- coupling said channels to a high resolution skew detection circuit;
- supplying a reference signal to multi-phase input circuitry of said skew detection circuit;
- selecting one of said tester signals for comparing against said reference signal on said skew detection circuit, said comparing step including the steps of:
 - converting the relative time difference between an edge of said reference signal and an edge of said passed tester signal to a voltage, and
 - providing said voltage at an output for use as a measurement of the relative skew between said tester signal and said reference signal.

18. A high-bandwidth analog multiplexer, said multiplexer including:

- a plurality of input gates corresponding to a plurality of input signals, said plurality of input gates arranged into an integral number of groups, each of said groups comprising a predetermined number of said input gates configured in parallel and having a common output;
- a plurality of output transmission gates corresponding to the number of said common outputs, each of said plurality of output transmission gates coupled in series to said common outputs, and having respective output paths tied to form a single multiplexer output; and
- a plurality of feedthrough transmission gates corresponding to the number of said common outputs, each of said plurality of feedthrough transmission gates having an output coupled to said common output and a grounded output.