

METHODS FOR FORMING COPPER INTERCONNECT STRUCTURES BY CO-PLATING OF NOBLE METALS AND STRUCTURES FORMED THEREBY

5 FIELD OF THE INVENTION

The present invention relates to the field of microelectronic device processing, and more particularly to a method of forming a copper interconnect structure utilizing electroplating and/or electroless techniques and structures formed thereby.

10 BACKGROUND OF THE INVENTION

Transistors, as is well known in the art, are the building blocks of all integrated circuits. Modern integrated circuits interconnect literally millions of densely configured transistors that perform a wide variety of functions. To achieve such a dramatic increase in the density of circuit components has required
15 microelectronic manufacturers to scale down the physical dimensions of the circuit elements, as well as to utilize multiple levels of interconnection structures used to connect the circuit elements into functional circuitry.

One such interconnection process is known as the damascene process (FIG. 5), in which dielectric layers 202 and 202' are deposited over a substrate
20 200. Vias 204, 204' and trenches 206, 206' are etched into the dielectric layers 202,202'. Metal layers 208, 208', such as copper or aluminum, is then formed over the vias 204, 204' and trenches 206, 206'. This process can be repeated to achieve interconnection, through the trenches and vias, of multiple layers of metallization.

25 The utilization of copper metal in a damascene structure has many advantages, for example its lower electrical resistance as compared with previously used metals, such as aluminum. One technique for depositing copper

in a damascene structure is by electroless deposition, which is attractive because of its lower cost and high quality of deposition. In electroless plating, metal deposition occurs by a chemical reduction reaction in an aqueous solution which contains a reducing agent, wherein no external power supply is needed. However, 5 electroless deposition requires the activation of a nonconductive surface, for example by providing a seed layer, in order to electrolessly deposit the metal.

However, there are problems associated with the use of copper as an interconnect metal in a damascene structure. One such problem is that copper diffuses or drifts easily into the dielectric layers 202, 202' (referring again to 10 FIG.5), thus forming shorts between adjacent circuit elements. Copper interconnect structures must therefore be encapsulated by diffusion barrier layers, such as tantalum, tantalum nitride, titanium nitride (TiN) or titanium tungsten (TiW). Unfortunately, the addition of the diffusion barrier layer can increase the effective dielectric constant of the copper interconnect structure, which results in 15 an increase in the resistance-capacitance (RC) delay which degrades the electrical performance of the device.

Another problem associated with copper metallization is that copper is readily oxidized, especially during subsequent processing steps. The oxidized copper degrades the electrical and mechanical properties of the copper 20 interconnect. Accordingly, an hermetic encapsulating layer is generally employed in order to provide corrosion resistance for the copper layer, such encapsulating materials may include silicon carbide (SiC) and silicon nitride (SiN). This encapsulating layer may also serve as an etch stop, which prevents over-etching of the copper layer during subsequent processing steps. However, this

encapsulating layer can also increase the effective dielectric constant of the copper interconnect structure.

Yet another problem encountered with copper metallization is the electromigration of copper atoms at high current densities, which can result in voids in the metal interconnect structure. One method of reducing the amount of electromigration is to alloy the copper metal with aluminum, tin, indium or silicon; however, this may increase the copper resistance significantly.

Accordingly, there is a need for an improved copper interconnect fabrication process and structure that increases copper corrosion resistance and/or oxidation resistance, increases electromigration resistance, and/or decreases the effective dielectric constant of the copper interconnect structure.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which: FIGS. 1a-1f represent cross-sections of structures that may be formed when carrying out an embodiment of the method of the present invention.

FIG. 2 represents a cross-section of a structure that may be formed when carrying out an embodiment of the method of the present invention.

FIG. 3 represents a cross-section of a structure that may be formed when carrying out yet another embodiment of the method of the present invention.

FIG. 4 is a process flow diagram according to an embodiment of the present invention.

FIG. 5 is a cross-sectional illustration of a damascene interconnect structure, as is known in the art.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

5 In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different,
10 are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be
15 modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar
20 functionality throughout the several views.

 A method for making a copper interconnect structure is described. That method comprises forming an opening in a dielectric layer disposed on a substrate, forming a barrier layer over the opening, forming a seed layer over the metal layer, and forming a copper-noble metal alloy layer by electroplating and/or
25 electroless deposition on the seed layer, wherein the copper-noble metal alloy

layer improves the electrical characteristics and reliability of the copper interconnect structure. Either an etch stop layer or a cladding layer may then be formed on the copper alloy layer.

In an embodiment of the method of the present invention, as illustrated by
5 FIGS. 1a-1f, a dielectric layer 104 is formed on a substrate 102 (FIG. 1a). The substrate 102 may comprise materials such as silicon, silicon-on insulator, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Although several examples of materials from which the substrate 102 may be formed are described here, any material
10 that may serve as a foundation upon which a microelectronic device may be built falls within the spirit and scope of the present invention.

The dielectric layer 104 is formed on the substrate 102. Those skilled in the art will appreciate that the dielectric layer 104 may also be formed from a variety of materials, thicknesses or multiple layers of material. By way of illustration and
15 not limitation, the dielectric layer 104 may include silicon dioxide (preferred), organic materials or inorganic materials. Although a few examples of materials that may be used to form the dielectric layer 104 are described here, that layer may be made from other materials that serve to separate and insulate the different metal layers.

20 The dielectric layer 104 may be formed on the substrate 102 using a conventional deposition method, e.g., a chemical vapor deposition ("CVD"), a low pressure CVD ("LPCVD"), a physical vapor deposition ("PVD"), or an atomic layer deposition ("ALD"). Preferably, a CVD process is used. In such a process, a metal oxide precursor (e.g., a metal chloride) and steam may be fed at selected
25 flow rates into a CVD reactor, which is then operated at a selected temperature

and pressure to generate an atomically smooth interface between the substrate 102 and the dielectric layer 104. The CVD reactor should be operated long enough to form the dielectric layer 104 with the desired thickness. In most applications, the dielectric layer 104 is about one micron thick, and more
5 preferably between about 6,000 angstroms and about 8,000 angstroms thick.

The dielectric layer 104 may have at least one opening 105 formed in it (FIG. 1b), which comprises at least one via 106, and at least one trench 107, which may be used to connect to other metal layers in the microelectronic device (not shown), according to the conventional damascene technique as is known by
10 those skilled in the art. As such steps are well known in to those skilled in the art, they will not be described in more detail here.

Following the formation of the opening 105, a barrier layer 108 is deposited onto the opening 105 (FIG. 1c). Those skilled in the art will appreciate that barrier layer 108 may be formed from a variety of materials, thicknesses or multiple
15 layers of material. By way of illustration and not limitation, the barrier layer 108 may be deposited using conventional techniques such as PVD, ALD, conventional CVD, low pressure CVD or other such methods known to those skilled in the art. In a currently preferred embodiment, the barrier layer can include any one of the following materials: tantalum, tungsten, titanium, ruthenium, molybdenum, and
20 their alloys with nitrogen, silicon and carbon. Although a few examples of materials that may be used to form the barrier layer 108 are described here, that layer may be made from other materials that serve to prevent the diffusion of a metal across the barrier layer 108. The barrier layer 108 can range from about 10 angstroms to about 500 angstroms. A thinner barrier layer 108 is preferred
25 (between about 10 angstroms and 50 angstroms), as a thin barrier layer makes

less of a contribution to the overall resistance of the copper interconnect structure.

A seed layer 110 may then be optionally formed on the barrier layer 108 (FIG. 1d), and may comprise copper exclusively, or its alloys with tin, indium, cadmium, aluminum, magnesium, or its alloys with noble metals such as silver, palladium, platinum, rhodium, ruthenium, gold, iridium and osmium, or the seed layer 110 may comprise noble metals exclusively. Those skilled in the art will appreciate that the seed layer 110 may be formed from a variety of materials, thicknesses or multiple layers of material. In a currently preferred embodiment, the seed layer 110 is between about 10 angstroms and 2,000 angstroms thick, and comprises a copper-noble metal alloy. The atomic percentage of noble metal in the seed layer 110 is preferably about ten percent or less, and is most preferably between about 0.1 and 4 atomic percent. The seed layer 110 may be formed on the barrier layer 108 using a conventional deposition method, e.g., a conventional CVD, low pressure CVD, PVD, ALD, or other such methods known to those skilled in the art. Although a few examples of materials that may be used to form the seed layer 110 are described here, the seed layer 110 may be made from other materials that serve to activate the surface of the diffusion barrier layer in order to prepare it for the electroless deposition or the electroplating of copper.

In a preferred embodiment, the copper deposition process may be performed using a conventional copper electroplating process, which is well known in the art, in which a single or dual damascene structure is filled with copper by using a direct current (DC) electroplating process (see FIG.4). First, a surface (either the barrier layer 108 or the seed layer 110) is provided for the electroplating of copper 118. Next, the surface is exposed to an electroplating

solution 119. Then, a copper alloy layer 112 is formed on the surface 120. In addition, it is well known in the art that if the surface is the seed layer 110, the seed layer 110, may be consumed by the electroplating process, so that the seed layer 110 may become continuous with the copper alloy layer 112, as depicted in FIG. 1f. In addition, it is to be understood that the electroplating of copper may be formed directly on the barrier layer, since the seed layer is optional, and thus the seed layer may not be present in an embodiment of the invention (see FIG. 1f).

In a currently preferred embodiment, the electroplating solution may comprise copper ions, sulfuric acid, chloride ions, additives (such as suppressors i.e. polyethylene glycol, and anti-suppressors i.e. di-sulfide), noble metal ions, noble metals and complexing agents (such as thiosulfate and peroxodisulfate). Although a few examples of materials that may comprise the electroplating solution are described here, that solution may comprise other materials that serve to deposit noble metal alloys of copper onto a surface, such as the barrier layer 108 or the seed layer 110 (FIG. 1e and 1f).

Alternatively, the deposition of copper may be performed using an electroless deposition process, which includes any autocatalytic (i.e. no external power supply is applied) deposition of a film through the interaction of a metal salt and a chemical reducing agent. First, as is known in the art, preparing or treating a surface, such as the barrier layer 108, is necessary in order to produce an activated surface, i.e. a surface that is susceptible to the electroless deposition process. Methods for providing the activation of a surface for electroless deposition may include contact displacement, in which the surface is dipped or sprayed with a copper containing contact displacement solution, or the utilization of a seed layer, such as the seed layer 110. During the electroless deposition,

the seed layer 110 (see FIG. 1c) may serve as the activated surface upon which the electroless deposition forms. The seed layer 110 acts as a region which controls the placement of the deposited metal from the electroless deposition process, because the metal from the electroless deposition solution only deposits
5 on the seed layer 110. The inherent selectivity of the electroless deposition method results in a higher quality metallization film because it improves the uniformity and continuity of the electrolessly deposited metal layer.

Next, after the activated surface (the seed layer 110 in the current embodiment of the present invention) for electroless deposition has been
10 provided, the activated surface is exposed to the electroless deposition solution, by methods including immersing the activated surface in an electroless deposition solution or spraying the electroless deposition solution onto the activated surface. Finally, a metal, such as the copper alloy layer 112 of the present invention (see FIG. 1e), is electrolessly deposited on the activated surface.

15 The copper alloy layer 112 may comprise the following alloys: copper silver, copper palladium, copper platinum, copper rhodium, copper ruthenium, copper gold, copper iridium and copper osmium. The percentage of noble metal in the alloy is about four percent atomic weight, most preferably between about 0.1 and 4 percent atomic weight. The incorporation of the noble metals in the
20 copper alloy layer 112 increases copper corrosion resistance since the copper alloy layer 112 is less prone to oxidize than pure copper due to the un-reactive nature of the noble metal. The copper alloy layer 112 is also more electromigration resistant than pure copper because the low solubility of the noble metals facilitates the stuffing of the grain boundaries of the copper alloy layer 112
25 by the noble metals, as well as stuffing the interfaces the copper layer 112 makes

with the barrier layer 108 and an etch stop layer 114 (which may be deposited in a later step, see FIG. 2). This prevents the occurrence of a major failure path (shorts, etc.) for electromigration, which would otherwise occur along the grain boundaries and interfaces. In addition, the noble metal resistance to oxidation prevents failure paths through the cracked or porous copper oxide that may form on the top surface of copper alloy layer 112, as well as at the barrier layer 108-dielectric layer 104 interface. Thus, a method of forming a copper interconnect structure 113 has been disclosed (FIGS. 1e and 1f).

It is to be appreciated that multiple layers of metallization may be deposited on top of the copper interconnect structure 113, according to the method of the present invention, as shown in FIGS. 2 and 3. After the copper alloy layers 112, 112' are formed as previously described herein, etch stop layers 114, 114' may be formed above the copper alloy layers 112, 112' (FIG.2). The etch stop layers 114, 114' may comprise silicon carbide, silicon nitride, silicon carbon nitride, and other such materials as are known in the art. Those skilled in the art will appreciate that the etch stop layers 114, 114' may be formed from a variety of materials, thicknesses or multiple layers of material. Although a few examples of materials that may be used to form the etch stop layers 114, 114' are described here, that layer may be made from other materials that serve to stop the etching of copper alloy layer 112 during subsequent process steps, such as during subsequent lithographic, etching and cleaning processing steps. Since such processing steps are well known in the art, they will not be described in detail here. By way of illustration and not limitation, the etch stop layers 114, 114' may be deposited using conventional techniques such as PVD, ALD, conventional CVD, low pressure CVD or other such methods known to those skilled in the art.

The etch stop layer 114,114' can range from about 100 angstroms to about 1000 angstroms. A thinner etch stop layer 114,114' is preferred, as a thinner layer makes less of a contribution to the overall dielectric constant of the copper interconnect structure.

5 In another embodiment, cladding layers 116, 116' can be electrolessly deposited over the copper alloy layers 112, 112' instead of the etch stop layers 114, 114' (FIG. 3). The cladding layers 116, 116' may comprise noble metals or their alloys with refractory metals, for example silver tungsten, palladium tungsten. In addition, cladding layers 116, 116' may comprise electrolessly deposited cobalt
10 nickel alloys with refractory metals and/or their metalloids (i.e. boron or phosphorous). The use of the cladding layers allows for the elimination of the etch stop layer altogether, since no etch stop function is needed due to the high corrosion resistance of the copper alloy layer 112,112' and the cladding layers 116, 116'. The elimination of the etch stop layer reduces the effective dielectric
15 constant of the copper alloy layer, which improves the electrical performance and speed of the transistor device.

 As described above, the use of an electrolessly deposited noble metal-copper alloy metallization structure increases copper corrosion resistance and oxidation resistance, increases electromigration resistance, and decreases the
20 effective dielectric constant of the copper interconnect structure. Thus the reliability and speed of the microelectronic device are greatly enhanced. It is understood that the present invention includes both single and dual damascene structures, as well as multilevel metallization structures.

 Although the foregoing description has specified certain steps and
25 materials that may be used in the method of the present invention, those skilled in

the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims. In addition, it is appreciated that the fabrication

5 of a multiple metal layer structure atop a substrate, such as a silicon substrate, to manufacture a silicon device is well known in the art. Therefore, it is appreciated that the Figures provided herein illustrate only portions of an exemplary microelectronic device that pertains to the practice of the present invention. Thus the present invention is not limited to the structures described herein.

IN THE CLAIMS

What is claimed is:

- 5 1. A method of plating copper, comprising:
 plating a copper alloy layer on a surface by electroplating, wherein
 the copper alloy layer substantially comprises copper and a noble metal.
- 10 2. The method of claim 1 wherein the copper alloy layer is formed by
 electroplating.
3. The method of claim 1 wherein the copper alloy layer is formed by
 electroless deposition.
- 15 4. The method of claim 1 wherein the surface comprises either a seed
 layer or a barrier layer.
5. The method of claim 2 wherein the seed layer comprises less
 than about 10% atomic weight of the noble metal.
- 20 6. The method of claim 1 wherein the noble metal comprises less
 than about 4% of the atomic weight of the copper alloy layer.
7. The method of claim 1, wherein the noble metal substantially

comprises a material selected from the group consisting of silver, palladium, platinum, rhodium, ruthenium, gold, iridium, osmium, and combinations thereof.

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8. A method of forming a copper interconnect, comprising:
forming an opening in a dielectric layer disposed on a substrate;
forming a barrier layer over the opening;
forming a seed layer over the barrier layer; and

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forming a copper alloy layer on the seed layer, wherein the copper alloy comprises copper and a noble metal.

9. The method of claim 8 wherein the copper alloy layer is formed by electroplating.

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10. The method of claim 8 wherein the copper alloy layer is formed by electroless deposition.

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11. The method of claim 8 wherein the noble metal comprises less than about 4% of the atomic weight of the copper alloy layer.

12. The method of claim 8 wherein the seed layer comprises less than about 10% atomic weight of noble metals.

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13. The method of claim 8 wherein the noble metal substantially comprises a material selected from the group consisting of silver,

palladium, platinum, rhodium, ruthenium, gold, iridium and osmium and combinations thereof.

14. The method of claim 8 wherein the seed layer substantially comprises a material selected from the group consisting of copper, tin, aluminum, magnesium, silver, palladium, platinum, rhodium, ruthenium, gold, iridium, osmium and combinations thereof.

15. The method of claim 8 wherein the opening in the dielectric layer is a damascene structure.

16. The method of claim 8 wherein the barrier layer substantially comprises a material selected from the group consisting of tantalum, tungsten, titanium, ruthenium, tantalum nitride, tungsten nitride, titanium nitride, ruthenium nitride, tantalum silicide, tungsten silicide, titanium silicide, ruthenium silicide, tantalum carbide, tungsten carbide, titanium carbide, ruthenium carbide, and combinations thereof.

17. The method of claim 8 further including forming an etch stop layer.

18. The method of claim 17 wherein the etch stop layer substantially comprises a material selected from the group consisting of silicon carbide, silicon nitride, and combinations thereof.

19. The method of claim 18 wherein the etch stop layer is formed by chemical vapor deposition and is less than about 1000 angstroms thick.

20. The method of claim 8 further including forming a cladding layer.

21. The method of claim 20 wherein the cladding layer substantially
5 comprises a material selected from the group consisting of silver,
palladium, platinum, rhodium, ruthenium, gold, iridium, osmium, tungsten
and combinations thereof.

22. The method of claim 21 wherein the cladding layer is formed by
10 electroless deposition.

23. The method of claim 22, wherein the cladding layer substantially
comprises a material selected from the group consisting of cobalt, nickel,
tungsten, titanium, tantalum, molybdenum, zirconium, rhenium, boron,
15 phosphorus, and combinations thereof.

24. A copper interconnect, comprising:
a dielectric layer having an opening;
a barrier layer on the opening; and
20 a copper alloy layer on the barrier layer wherein the copper alloy
layer substantially comprises copper and a noble metal.

25. The method of claim 24 wherein the noble metal comprises less
than about 4% of the atomic weight of the copper alloy layer.

26. The copper interconnect of claim 25, further including forming a cladding layer on the copper alloy layer.

27. The copper interconnect of claim 26 wherein the cladding layer substantially comprises a material selected from the group consisting of silver, palladium, platinum, rhodium, ruthenium, gold, iridium, osmium, tungsten and combinations thereof.

28. The copper interconnect of claim 24, further including forming an etch stop layer on the copper alloy layer.

29. The copper interconnect of claim 28 wherein the etch stop layer substantially comprises a material selected from the group consisting of silicon carbide, silicon nitride, and combinations thereof.