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ALL DIGITAL IMPLEMENTATION OF CLOCK SPECTRUM SPREADING (DITHER) FOR LOW POWER/DIE AREA

CROSS-REFERENCES TO RELATED APPLICATIONS

5 [0001] This application claims priority to U.S. Provisional Patent Application No. 60/704,510, filed August 1, 2005, titled "ALL DIGITAL IMPLEMENTATION OF CLOCK SPECTRUM SPREADING (DITHER) FOR LOW POWER/DIE AREA," U.S. Provisional Patent Application No. 60/722,731, filed September 30, 2005, titled "ALL DIGITAL IMPLEMENTATION OF CLOCK SPECTRUM SPREADING (DITHER) FOR LOW
10 POWER/DIE AREA," and U.S. Patent Application No. 11/246,328, filed October 6, 2005, titled "ALL DIGITAL IMPLEMENTATION OF CLOCK SPECTRUM SPREADING (DITHER) FOR LOW POWER/DIE AREA," the disclosures of which are incorporated by reference herein in their entirety.

15 BACKGROUND OF THE INVENTION

[0002] The present invention generally relates to integrated circuits, and more particularly relates to digitally spreading a clock spectrum in digital circuits.

[0003] The spreading of a clock spectrum generally includes spreading the power of clock pulses over a range of frequencies. FIG. 1 is a simplified schematic of a first clock train 100 and a spread-spectrum clock train 105. The pulses in spread-spectrum clock train 105 are spread-spectrum pulses that may be generated from the clock pulses in the first clock train 100. The clock edges of the spread-spectrum pulses move in and out as indicated by the arrows in FIG. 1. A spread-spectrum clock train is typically generated for applications in which jitter sensitivity is generally low and/or in which lowering peak power of clock pulses
25 is desired.

[0004] Traditional circuits configured to spread the spectrum of a clock train often include both digital and analog circuits, which typically include a digital modulator and an analog phase interpolator. The digital modulator is configured to receive a clock train (e.g., the first clock train) from a clock generator. The clock train may be a digital clock train. The digital
30 modulator may be configured to modulate the clock train using a dithering waveform to generate a dithered waveform. The dithered waveform may then be transferred to the analog-



phase interpolator that is configured to phase interpolate the dithered waveform. Based on the phase interpolation of the dithered waveform, the analog-phase interpolator is configured to generate and output a spread-spectrum clock train.

[0005] These traditional circuits configured to spread the spectrum of a clock train have a number of inherent shortcomings especially for low power circuit applications. For example, typical digital modulators configured to modulate a clock train typically operate at the clock frequency of the clock train, which is typically the relatively high frequency of a free running clock (e.g., generated by a crystal oscillator). As traditional digital modulators are configured to operate at a free running clock frequency, these digital modulators tend to draw relatively high current.

[0006] Not only do the digital modulators included in these traditional circuits typically draw relatively high current, the analog-phase interpolators in these traditional circuits also typically draw relatively high current. For example, an analog-phase interpolator may draw as much as a digital modulator. Moreover, as these traditional circuits typically include analog devices (namely, an analog-phase interpolator), the shape of the spread-spectrum clock pulses and the amount of power reduction of these clock pulses is generally limited by the linearity of the analog-phase interpolator. Analog-phase interpolators having relatively high linearity are relatively costly to design and manufacture, and are relatively large. Also, as these traditional circuits often include both digital circuits and analog circuits, these traditional circuits tend to take up relatively large amounts of die space, which tends to make these circuits relatively costly to manufacture.

[0007] Therefore, new circuits are needed that are configured to spread the spectrum of a clock train, that draw relatively less current than traditional circuits that are configured to provide this function, and that take up relatively less die area than traditional circuits.

BRIEF SUMMARY OF THE INVENTION

[0008] Accordingly, embodiments of the present invention provide circuits, methods, apparatus, code for controlling circuits, code, and/or means to condition a clock train, and specifically to spread the spectrum of the clock train.

[0009] An exemplary embodiment of the present invention includes means for spreading a clock spectrum, and more specifically includes means for generating a phase value based on a frequency modulation waveform; and means for dividing a frequency of the clock train by a

divider value that includes a fixed value plus the phase value to generate a dithered clock train that is phase modulated by the phase value. The exemplary embodiment further includes means for accumulating the dithered clock train to generate the frequency modulation waveform; and means for accumulating the frequency modulation waveform to
5 generate a phase modulation signal and generate the phase value based on the phase modulation signal. The exemplary embodiment further includes means for tracking and locking onto the modulation of the dithered clock train. The exemplary embodiment further includes means for generating a spread-spectrum clock train that is the spread spectrum of the clock train based on tracking the modulation of the dithered clock train and filtering the
10 dithered clock train. The frequency modulation waveform is periodic or quasi periodic. The frequency modulation waveform is a triangle waveform. The frequency modulation waveform is a digital signal. The clock train is a digital clock train. The dithered clock train is a digital clock train. The phase value is proportional to the deviation of the frequency modulation waveform from the center of the frequency modulation waveform. The
15 exemplary embodiment further includes means for multiplying the frequency of the dithered clock train by a multiplier value. The average frequency of the spread-spectrum clock train is the frequency of the clock train multiplied by the multiplier value divided by the fixed value. The exemplary embodiment further includes means for splitting the phase modulation signal into a first phase modulation signal and a second phase modulation signal; means for
20 temporally delaying the second phase modulation signal with respect to the first phase modulation signal; and means for thereafter calculating the different between the first phase modulation signal and the second phase modulation signal to generate the phase value. The exemplary embodiment further includes means for adding the phase value to the fixed value to generate the divider value.

25 **[0010]** Another exemplary embodiment of the present invention includes means for spreading the spectrum of a clock train, and more specifically includes means for generating a dithered clock train, and means for accumulating the dithered clock train to generate a frequency modulation waveform. The exemplary embodiment further includes means for accumulating the frequency modulation waveform to generate a phase modulation signal; and
30 means for generating a temporally-varying divider value based on the phase modulation signal. The exemplary embodiment further includes means for digitally modulating the clock train based on the temporally-varying divider value. The exemplary embodiment further include means for tracking the modulation of the dithered clock train and filtering the

dithered clock train to generate a second clock train that is the spread spectrum of the first mentioned clock train. The temporally-varying divider value is a fixed-divider value plus a phase value. The phase value is determined from the frequency modulation waveform. The exemplary embodiment further includes means for generating the phase value based on the phase modulation signal. The exemplary embodiment further includes means for splitting the phase modulation signal into first and second phase modulation signals; and means for delaying the second phase modulation signal with respect to the first modulation signal to thereafter calculate the difference between first phase modulation signal and the second phase modulation signal to generate the phase value. The exemplary embodiment further includes means for adding the phase value to the fixed-divider value. The phase value is proportional to the deviation of the digital-frequency modulation waveform from the center of the digital-frequency modulation waveform. The frequency modulation waveform is a periodic or quasi-periodic. The frequency modulation waveform is a triangle waveform. The exemplary embodiment further includes means for generating the clock train.

[0011] According to a specific embodiment of the clock spreading means, the first clock train is a digital clock train. The closed-loop control means is configured for multiplying the frequency of the dithered clock train by a fixed-multiplier value. The temporally-varying divider value is a fixed-divider value plus a phase value, and the average frequency of the second clock train is the frequency of the first clock train multiplied by the fixed-multiplier value and divided by the fixed-divider value. The exemplary embodiment further includes means for calculating the difference between a first portion of the phase modulation signal and a second portion of the phase modulation signal, wherein the second portion is temporally retarded with respect to the first portion; and the difference is the phase value. The exemplary embodiment further includes means for adding the phase value to a fixed divider value to generate the temporally-varying-divider value. The means for tracking the modulation of the dithered clock train and filtering the dithered clock train to generate a second clock train is a phase-locked loop circuit.

[0012] A better understanding of the nature and advantages of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a simplified schematic of a first clock train and a spread-spectrum clock train that may be generated from the first clock train according to one embodiment of the present invention;

5 [0014] FIG. 2 is a simplified schematic of a digital circuit configured to generate a spread-spectrum clock train according to one embodiment of the present invention;

[0015] FIG. 3 is a high-level flow chart having steps for generating a spread-spectrum clock train according to one embodiment of the present invention; and

10 [0016] FIGs. 4A-4H illustrate various implementations of exemplary embodiments of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0017] The present invention generally provides a digital circuit apparatus and digital circuit method for conditioning a digital signal. More specifically, the present invention provides a digital circuit apparatus and digital circuit method for spreading a clock spectrum.

15 [0018] Spreading a clock spectrum, such as a digital clock spectrum, includes spreading power of clock pulses in a clock train over a range of frequencies. FIG. 1 is a simplified schematic of a first clock train 100 and a spread-spectrum clock train 105 that may be generated from the first clock train according to an embodiment of the present invention. The edges of the spread-spectrum clock train are dithered with respect to the first clock train as indicated by the arrows in FIG. 1. The clock pulses of the first clock train may be digitally conditioned to generate the spread spectrum clock pulses in the spread-spectrum clock train.

20 [0019] FIG. 2 is a simplified schematic of a circuit 200 according to one embodiment of the present invention. Circuit 200 includes a clock pulse generator 205, a variable divider 210, a first accumulator 215, a second accumulator 220, a delay circuit 225, and first adder 230, a second adder 235, and a phase-locked loop (PLL) 240. Delay circuit 225, adder 230, and adder 235 are sometimes referred to herein as the phase-value calculator. According to one embodiment, each of the foregoing listed circuits is a digital circuit. According to an alternative embodiment, the PLL may be a mixed signal circuit. Circuit 200 is configured to generate the first clock train 100, and condition the first clock train to generate the spread-spectrum clock train 105. The frequency “f₁” of the first clock train may be the oscillation

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frequency of a free running clock, such as a crystal oscillator. The average frequency “f2” of the spread-spectrum clock train can be less than, equal to, or greater than to f1.

[0020] According to one embodiment, clock pulse generator 205 is configured to generate the first clock train 100, which may be a digital clock train. The first clock train is transferred from an output of clock pulse generator 205 to an input of variable divider 210. Variable divider 210 is configured to generate a dithered clock train 245 that has a frequency “f3.” More specifically, the variable divider is configured to divide the frequency f1 of the clock train by a “divider” value $N + \delta$, wherein f3 is equal to $f1/(N+\delta)$. N may be a fixed value (e.g., 128) and δ may be a time varying value (referred to herein as a phase value).

Generation of the phase value is described in detail below. The phase value may be relatively small compared to the N. For example, the absolute value of δ may be 10 times less than N, or smaller (e.g., 20 times less than N). The value of N may be user specified or may be specified by other circuits (not shown) that are coupled to circuit 200. The value of N may be specified according to a particular application for which circuit 200 is intended.

[0021] Dithered clock train 245 may be transferred from an output of the variable divider to an input of accumulator 215 and to an input of PLL 240. Accumulator 215 (sometimes referred to herein as a frequency accumulator) is configured to accumulate the dithered clock train, and therefrom, generate a frequency modulation waveform 250, which may be a digital signal. The frequency modulation waveform may be periodic or quasi periodic and may have a variety of shapes, such as triangular, saw-toothed, teardrop, capricious or the like. The frequency modulation waveform is used by circuit 200 to modulate the phase of clock train 100 to generate the dithered clock train having dithered edges. Specifically, the frequency modulation waveform is transferred from an output of accumulator 215 to an input of accumulator 220 (sometimes referred to herein as the phase accumulator). Accumulator 220 is configured to accumulate the frequency modulation waveform and is configured to receive the dithered clock train from the variable divider. Accumulator 220 is further configured to generate a phase modulation signal 255 from the accumulated frequency modulation waveform.

[0022] According to one embodiment, the phase value is proportional to the deviation of the frequency modulation waveform from the center of the frequency modulation waveform. For example, if the frequency modulation waveform is a triangle waveform, the phase value may be proportional to a value of the triangle waveform above or below a reference line 260.

More specifically, to calculate the phase value, the phase modulation signal is transferred via two circuit paths 265a and 265b to adder 230. Circuit path 265a might be a non-delayed path. Circuit path 265b may include delay circuit 225 that is configured to delay the phase modulation signal in the second circuit path relative to the phase modulation signal in the first circuit path. Delay circuit 225 may delay the phase modulation signal in circuit path 265b based on the received dithered clock 245. Adder 230 is configured to subtract the delayed phase modulation signal from the phase modulation signal that is not delayed. Stated alternatively, adder 230 is configured to calculate the difference in the phase modulation signal at different “time points.” The calculated difference in the phase modulation signal at different time points is the phase value δ . The phase value δ is transferred from adder 230 to adder 235, which is configured to add the phase value to the fixed value N to generate the divider value $N + \delta$. δ may be negative or positive depending, for example, on the amount the phase modulation signal is delayed by the delay circuit.

[0023] As the frequency modulation waveform changes with time, so to does the phase value. For example, as the frequency modulation waveform rises, the phase value similarly rises, and as the frequency modulation waveform decreases, the phase value similarly decreases. The phase value may decrease from a positive value to a negative value as the phase modulation waveform changes. Further, as the phase value changes with time, so to does the divider value $N + \delta$. Further yet, as the divider value temporally changes, the variable divider divides the frequency f_1 of the first clock train by these temporally changing divider values. For example, as the divider values increase, the edges of the dithered clock train generated by the variable divider extend (i.e., the frequency of the dithered clock train decreases), and as the divider values decrease, the edges of the dithered clock train retract (i.e., the frequency of the dithered clock train increases). This phase change of the dithered clock train changes at approximately the frequency of the frequency modulation waveform.

[0024] According to one embodiment, the frequency of the phase change of the dithered clock train is within the operable detection range of PLL 240. Accordingly, the PLL can track and lock onto the modulation of the dithered clock train to filter the dithered clock train to generate the spread-spectrum clock train. As the edges (i.e., phase) of the dithered clock train dither, the edges of the clock pulses of the spread-spectrum clock train similarly dither.

[0025] According to one embodiment, the PLL may be configured to multiply the frequency of the dithered clock train by a multiplier value “M,” such that the average

frequency f_2 of spread-spectrum clock train 105 is $(M/N) \cdot f_1$. The value of M may be adjusted to tune the frequency f_2 to a variety of desired values.

[0026] FIG. 3 is a high-level flow chart having steps for spreading the spectrum of clock pulses composing clock train 100 to generate spread-spectrum clock train 105. It should be understood that the steps of the described high-level flow are exemplary and that various steps may be substituted with alternative steps, steps may be combined, and/or steps may be eliminated without deviation from the embodiment represented by the high-level flow chart. In an initial step 300, the variable divider receives the clock train and the temporally-varying divider value. In a step 305, the variable divider divides the frequency of the clock train by the temporally-varying divider value to phase modulate the clock train and thereby generate the dithered clock train. The temporally-varying divider value includes the fixed value plus the phase value, which temporally varies. In a step 310, the frequency accumulator receives the dithered clock train from the variable divider, and generates the frequency modulation waveform based on accumulation of the dithered clock train. In a step 315, the phase accumulator receives the frequency modulation waveform from the frequency accumulator and generates the phase modulation signal based on accumulation of the frequency modulation waveform. In a step 320, the phase-value calculator calculates the difference between different time points of the phase modulation signal; the difference is the phase value. In a step 325, the phase value is added to the fixed value to generate the temporally-varying divider value. In a step 330, a phase-locked loop (PLL) receives the dithered clock train from the variable divider. In a step 335, the PLL tracks the modulation of the dithered clock train and filters the dithered clock train to generate and output the spread-spectrum clock train.

[0027] Referring now to Figures 4A-4G, various exemplary implementations of the present invention are shown. Referring to Figure 4A, the present invention may be embodied in a hard disk drive 400. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 4A at 402. In some implementations, signal processing and/or control circuit 402 and/or other circuits (not shown) in HDD 400 may process data, perform coding and/or encryption, perform calculations, and/or format data that is output to and/or received from a magnetic storage medium 406.

[0028] HDD 400 may communicate with a host device (not shown) such as a computer, mobile computing devices such as personal digital assistants, cellular phones, media or MP3

players and the like, and/or other devices via one or more wired or wireless communication links 408. HDD 400 may be connected to memory 409, such as random access memory (RAM), a low latency nonvolatile memory such as flash memory, read only memory (ROM) and/or other suitable electronic data storage.

5 [0029] Referring now to Figure 4B, the present invention may be embodied in a digital versatile disc (DVD) drive 410. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 4B at 412, and/or mass data storage 418 of DVD drive 410. Signal processing and/or control circuit 412 and/or other circuits (not shown) in DVD 410 may process data, perform coding and/or encryption,
10 perform calculations, and/or format data that is read from and/or data written to an optical storage medium 416. In some implementations, signal processing and/or control circuit 412 and/or other circuits (not shown) in DVD 410 can also perform other functions such as encoding and/or decoding and/or any other signal processing functions associated with a DVD drive.

15 [0030] DVD drive 410 may communicate with an output device (not shown) such as a computer, television or other device via one or more wired or wireless communication links 417. DVD 410 may communicate with mass data storage 418 that stores data in a nonvolatile manner. Mass data storage 418 may include a hard disk drive (HDD) such as that shown in Figure 4A. The HDD may be a mini HDD that includes one or more platters having a
20 diameter that is smaller than approximately 1.8". DVD 410 may be connected to memory 419, such as RAM, ROM, low latency nonvolatile memory such as flash memory, and/or other suitable electronic data storage.

[0031] Referring now to Figure 4C, the present invention may be embodied in a high definition television (HDTV) 420. The present invention may implement either or both
25 signal processing and/or control circuits, which are generally identified in Figure 4C at 422, a WLAN interface and/or mass data storage of the HDTV 420. HDTV 420 receives HDTV input signals in either a wired or wireless format and generates HDTV output signals for a display 426. In some implementations, signal processing circuit and/or control circuit 422 and/or other circuits (not shown) of HDTV 420 may process data, perform coding and/or
30 encryption, perform calculations, format data and/or perform any other type of HDTV processing that may be required.

[0032] HDTV 420 may communicate with mass data storage 427 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices. At least one HDD may have the configuration shown in Figure 4A and/or at least one DVD may have the

configuration shown in Figure 4B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". HDTV 420 may be connected to memory 428 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. HDTV 420 also may support connections with a WLAN via a WLAN network interface 429.

[0033] Referring now to Figure 4D, the present invention implements a control system of a vehicle 430, a WLAN interface and/or mass data storage of the vehicle control system. In some implementations, the present invention implements a powertrain control system 432 that receives inputs from one or more sensors such as temperature sensors, pressure sensors, rotational sensors, airflow sensors and/or any other suitable sensors and/or that generates one or more output control signals such as engine operating parameters, transmission operating parameters, and/or other control signals.

[0034] The present invention may also be embodied in other control systems 440 of vehicle 430. Control system 440 may likewise receive signals from input sensors 442 and/or output control signals to one or more output devices 444. In some implementations, control system 440 may be part of an anti-lock braking system (ABS), a navigation system, a telematics system, a vehicle telematics system, a lane departure system, an adaptive cruise control system, a vehicle entertainment system such as a stereo, DVD, compact disc and the like. Still other implementations are contemplated.

[0035] Powertrain control system 432 may communicate with mass data storage 446 that stores data in a nonvolatile manner. Mass data storage 446 may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 4A and/or at least one DVD may have the configuration shown in Figure 4B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Powertrain control system 432 may be connected to memory 447 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Powertrain control system 432 also may support connections with a WLAN via a WLAN network interface 448. The control system 440 may also include mass data storage, memory and/or a WLAN interface (all not shown).

[0036] Referring now to Figure 4E, the present invention may be embodied in a cellular phone 450 that may include a cellular antenna 451. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 4E at 452, a WLAN interface and/or mass data storage of the cellular phone 450. In

some implementations, cellular phone 450 includes a microphone 456, an audio output 458 such as a speaker and/or audio output jack, a display 460 and/or an input device 462 such as a keypad, pointing device, voice actuation and/or other input device. Signal processing and/or control circuits 452 and/or other circuits (not shown) in cellular phone 450 may process data, perform coding and/or encryption, perform calculations, format data and/or perform other cellular phone functions.

[0037] Cellular phone 450 may communicate with mass data storage 464 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 4A and/or at least one DVD may have the configuration shown in Figure 4B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Cellular phone 450 may be connected to memory 466 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Cellular phone 450 also may support connections with a WLAN via a WLAN network interface 468.

[0038] Referring now to Figure 4F, the present invention may be embodied in a set top box 480. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 4F at 484, a WLAN interface and/or mass data storage of the set top box 480. Set top box 480 receives signals from a source such as a broadband source and outputs standard and/or high definition audio/video signals suitable for a display 488 such as a television and/or monitor and/or other video and/or audio output devices. Signal processing and/or control circuits 484 and/or other circuits (not shown) of the set top box 480 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other set top box function.

[0039] Set top box 480 may communicate with mass data storage 490 that stores data in a nonvolatile manner. Mass data storage 490 may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 4A and/or at least one DVD may have the configuration shown in Figure 4B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Set top box 480 may be connected to memory 494 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Set top box 480 also may support connections with a WLAN via a WLAN network interface 496.

[0040] Referring now to Figure 4G, the present invention may be embodied in a media player 472. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 4G at 471, a WLAN interface and/or mass data storage of the media player 472. In some implementations, media player 472 includes a display 476 and/or a user input 477 such as a keypad, touchpad and the like. In some implementations, media player 472 may employ a graphical user interface (GUI) that typically employs menus, drop down menus, icons and/or a point-and-click interface via display 476 and/or user input 477. Media player 472 further includes an audio output 475 such as a speaker and/or audio output jack. Signal processing and/or control circuits 471 and/or other circuits (not shown) of media player 472 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other media player function.

[0041] Media player 472 may communicate with mass data storage 470 that stores data such as compressed audio and/or video content in a nonvolatile manner. In some implementations, the compressed audio files include files that are compliant with MP3 format or other suitable compressed audio and/or video formats. The mass data storage may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 4A and/or at least one DVD may have the configuration shown in Figure 4B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Media player 472 may be connected to memory 473 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Media player 472 also may support connections with a WLAN via a WLAN network interface 474.

[0042] Referring to Figure 4H, the present invention may be embodied in a Voice over Internet Protocol (VoIP) phone 483 that may include an antenna 439. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 4H at 482, a wireless interface and/or mass data storage of the VoIP phone 483. In some implementations, VoIP phone 483 includes, in part, a microphone 487, an audio output 489 such as a speaker and/or audio output jack, a display monitor 491, an input device 492 such as a keypad, pointing device, voice actuation and/or other input devices, and a Wireless Fidelity (Wi-Fi) communication module 486. Signal processing and/or control circuits 482 and/or other circuits (not shown) in VoIP phone 483 may process data, perform coding and/or encryption, perform calculations, format data and/or perform other VoIP phone functions.

[0043] VoIP phone 483 may communicate with mass data storage 502 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices, for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in Figure 4A and/or at least one DVD may have the configuration shown in Figure 4B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". VoIP phone 483 may be connected to memory 485, which may be a RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. VoIP phone 483 is configured to establish communications link with a VoIP network (not shown) via Wi-Fi communication module 486. Still other implementations in addition to those described above are contemplated.

[0044] It is to be understood that the exemplary embodiments described above are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims. For example, while exemplary embodiment 200 is described and shown as including a phased-locked loop circuit, it is to be understood that other embodiments may use a frequency locked-loop, delay locked loop, or any other closed-loop control circuitry adapted to track and filter the phase or frequency of the dithered clock train. Therefore, the above description should not be understood as limiting the scope of the invention as defined by the claims.

WHAT IS CLAIMED IS:

1. A method for spreading the spectrum of a clock train comprising:
generating a phase value based on a frequency modulation waveform;
dividing a frequency of the clock train by a divider value that includes a fixed value plus the phase value to generate a dithered clock train that is phase modulated by the phase value;
accumulating the dithered clock train to generate the frequency modulation waveform;
accumulating the frequency modulation waveform to generate a phase modulation signal and generate the phase value based on the phase modulation signal;
tracking and locking onto the modulation of the dithered clock train;
based on the tracking and locking steps, generating a spread-spectrum clock train that is the spread spectrum of the clock train.
2. The method of claim 1, wherein the frequency modulation waveform is periodic or quasi periodic.
3. The method of claim 2, wherein the frequency modulation waveform is a triangle waveform.
4. The method of claim 1, wherein the frequency modulation waveform is a digital signal.
5. The method of claim 1, wherein the clock train is a digital clock train.
6. The method of claim 1, wherein the dithered clock train is a digital clock train.
7. The method of claim 1, wherein the phase value is proportional to the deviation of the frequency modulation waveform from the center of the frequency modulation waveform.
8. The method of claim 1, further comprising multiplying the frequency of the dithered clock train by a multiplier value.

9. The method of claim 8, wherein the average frequency of the spread-spectrum clock train is the frequency of the clock train multiplied by the multiplier value divided by the fixed value.

10. The method of claim 1, further comprising
splitting the phase modulation signal into a first phase modulation signal and a second phase modulation signal;
temporally delaying the second phase modulation signal with respect to the first phase modulation signal; and thereafter
calculating the different between the first phase modulation signal and the second phase modulation signal to generate the phase value.

11. The method of claim 10, further comprising adding the phase value to the fixed value to generate the divider value.

12. A digital circuit configured to spread the spectrum of a clock train comprising:

a variable divider configured to digitally modulate the width of clock pulses composing the clock train to generate a dithered clock train;

a first accumulator configured to accumulate the dithered clock train to generate a frequency modulation waveform;

a second accumulator configured to accumulate the frequency modulation waveform to generate a phase modulation signal;

a phase-value calculator configured generate a temporally-varying divider value based on the phase modulation signal, wherein the variable divider is configured to digitally modulate the width based on the temporally-varying divider value; and

a closed-loop control circuit configured to track and filter the modulation of the dithered clock train to generate a second clock train that is the spread spectrum of the first mentioned clock train.

13. The digital circuit of claim 12, wherein the temporally-varying divider value is a fixed-divider value plus a phase value.

14. The digital circuit of claim 13, wherein the phase value is determined from the frequency modulation waveform.

15. The digital circuit of claim 13, wherein the phase-value calculator is further configured generate the phase value based on the phase modulation signal.

16. The digital circuit of claim 15, wherein the phase-value calculator is further configured to split the phase modulation signal into first and second phase modulation signals and delay the second phase modulation signal with respect to the first modulation signal to thereafter calculate the difference between first phase modulation signal and the second phase modulation signal to generate the phase value.

17. The digital circuit of claim 16, wherein the phase-value calculator is further configured add the phase value to the fixed-divider value.

18. The digital circuit of claim 13, wherein the phase value is proportional to the deviation of the digital-frequency modulation waveform from the center of the digital-frequency modulation waveform.

19. The digital circuit of claim 18, wherein the frequency modulation waveform is a periodic or quasi-periodic.

20. The digital circuit of claim 19, wherein the frequency modulation waveform is triangle waveform.

21. The digital circuit of claim 12, further comprising a clock generator configured to generate the clock train.

22. The digital circuit of claim 12, wherein the first clock train is a digital clock train.

23. The digital circuit of claim 12, wherein the closed-loop control circuit is configured to multiple the frequency of the dithered clock train by a fixed-multiplier value.

24. The digital circuit of claim 23, wherein the temporally-varying divider value is a fixed-divider value plus a phase value, and wherein the average frequency of the second clock train is the frequency of the first clock train multiplied by the fixed-multiplier value and divided by the fixed-divider value.

25. The digital circuit of claim 12, wherein:

the phase-value calculator includes first and second circuit paths configured to transfer the phase modulation signal to a first adder,

the second circuit path includes a delay circuit that is configured to temporally delay the phase modulation signal in the second circuit path relative to the phase modulation signal in the first circuit path, and

the first adder is configured to calculate the difference between the phase modulation signal received from the first circuit path and the second circuit path, and the difference is the phase value.

26. The digital circuit of claim 25, wherein the phase-value calculator further includes a second adder configured to add the phase value to a fixed divider value to generate the temporally-varying-divider value and transfer the temporally-varying-divider value to the variable divider.

27. The digital circuit of claim 12, wherein the closed-loop control circuit is a phase-locked loop circuit.