WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor package, the method comprising:

providing a semiconductor chip;

forming a redistribution substrate; and

fabricating a package including the semiconductor chip disposed on the redistribution substrate,

wherein the forming of the redistribution substrate comprises:

forming a first insulating layer on a substrate, the first insulating layer having a first opening formed therein;

forming an integrally formed first redistribution pattern in the first opening and on the first insulating layer, so that a first portion of the first redistribution pattern is in the first opening, and a second portion of the first redistribution pattern is on the first insulating layer such that part of the first insulating layer is between the second portion of the first redistribution pattern and the substrate;

forming a second insulating layer on the first insulating layer to cover the first redistribution pattern; and

performing a planarization process on the second insulating layer to expose the first redistribution pattern,

wherein the performing of the planarization process comprises:

removing the second insulating layer disposed on the first redistribution pattern to expose a surface of the first redistribution pattern; and

planarizing the exposed surface of the first redistribution pattern.

2. The method of claim 1, wherein the forming of the redistribution substrate further comprises: forming a first seed layer on a sidewall and a bottom surface of the first opening.

3. The method of claim 2, wherein, after forming the second insulating layer, the first seed layer does not extend between the first redistribution pattern and the second insulating layer.

4. The method of any one of claims 1 to 3, wherein the forming of the redistribution substrate further comprises: forming a resist pattern on the first insulating layer, the resist pattern having a first guide opening, and wherein the first redistribution pattern is formed in the first guide opening.

5. The method of claim 4, wherein the second portion of the first redistribution pattern is formed in the first guide opening and includes sidewalls that are vertical compared to tapered sidewalls of the first portion of the first redistribution pattern.

6. The method of any one of claims 1 to 5, wherein the forming of the redistribution substrate further comprises:

forming a third insulating layer having a second opening on the first redistribution pattern, the second opening exposing the first redistribution pattern;

forming a second redistribution pattern in the second opening and on the third insulating layer;

forming a fourth insulating layer covering the second redistribution pattern on the third insulating layer; and

performing a planarization process on the fourth insulating layer,

wherein the performing of the planarization process on the fourth insulating layer comprises:

removing the fourth insulating layer disposed on a surface of the second redistribution pattern; and

planarizing the surface of the second redistribution pattern.

7. A method of fabricating a semiconductor package, the method comprising:

forming a redistribution substrate configured to be electrically connected to a chip pad of a semiconductor chip,

wherein the forming of the redistribution substrate comprises:

forming a first insulating layer on a substrate, the first insulating layer having an opening formed therein;

forming a resist pattern on the first insulating layer, the resist pattern having a guide opening formed therein; and

forming a redistribution pattern in the opening and the guide opening,

wherein the forming of the redistribution substrate further comprises:

forming a second insulating layer on the first insulating layer to cover the redistribution pattern; and

planarizing the second insulating layer to expose a surface of the redistribution pattern, and

wherein the planarizing of the second insulating layer comprises:

removing the second insulating layer disposed on the redistribution pattern to expose the surface of the redistribution pattern; and

planarizing the exposed surface of the redistribution pattern.

8. The method of claim 7, wherein the forming of the redistribution substrate further comprises: forming a first seed layer in the opening and on the first insulating layer, and wherein the resist pattern is formed on the first seed layer.

9. The method of claim 8, wherein the forming of the redistribution substrate further comprises:

removing the resist pattern to expose the first seed layer; and

removing the first seed layer exposed by the redistribution pattern.

10. The method of any one of claims 7 to 9, wherein the planarizing of the exposed surface of the redistribution pattern is performed by a chemical mechanical polishing (CMP) method or a surface cutting method.

11. The method of any one of claims 7 to 10, further comprising:

mounting the semiconductor chip on the redistribution substrate; and

forming a molding layer covering the semiconductor chip on the redistribution substrate, wherein the redistribution substrate extends onto a bottom surface of the molding layer.

12. The method of claim 11, wherein the substrate includes a carrier substrate, the method further comprising:

removing the carrier substrate to expose a bottom surface of the first insulating layer,

wherein the semiconductor chip and the molding layer are disposed on a surface of the redistribution substrate opposite to the exposed bottom surface of the first insulating layer.

13. The method of any one of claims 7 to 12, wherein the semiconductor chip comprises: a semiconductor substrate; integrated circuits on the semiconductor substrate; an interconnection line connected to the integrated circuits; and the chip pad connected to the interconnection line,

wherein the substrate includes the semiconductor substrate such that forming a first insulating layer on a substrate includes forming the first insulating layer on the semiconductor substrate of the semiconductor chip, and

wherein the opening exposes the chip pad.

14. The method of any one of claims 7 to 13,

wherein a first portion of the redistribution pattern is in the opening, and a second portion of the redistribution pattern is in the guide opening and on the first insulating layer, and

wherein the second portion of the redistribution pattern includes sidewalls that are vertical compared to tapered sidewalls of the first portion of the redistribution pattern.