FIG. 1

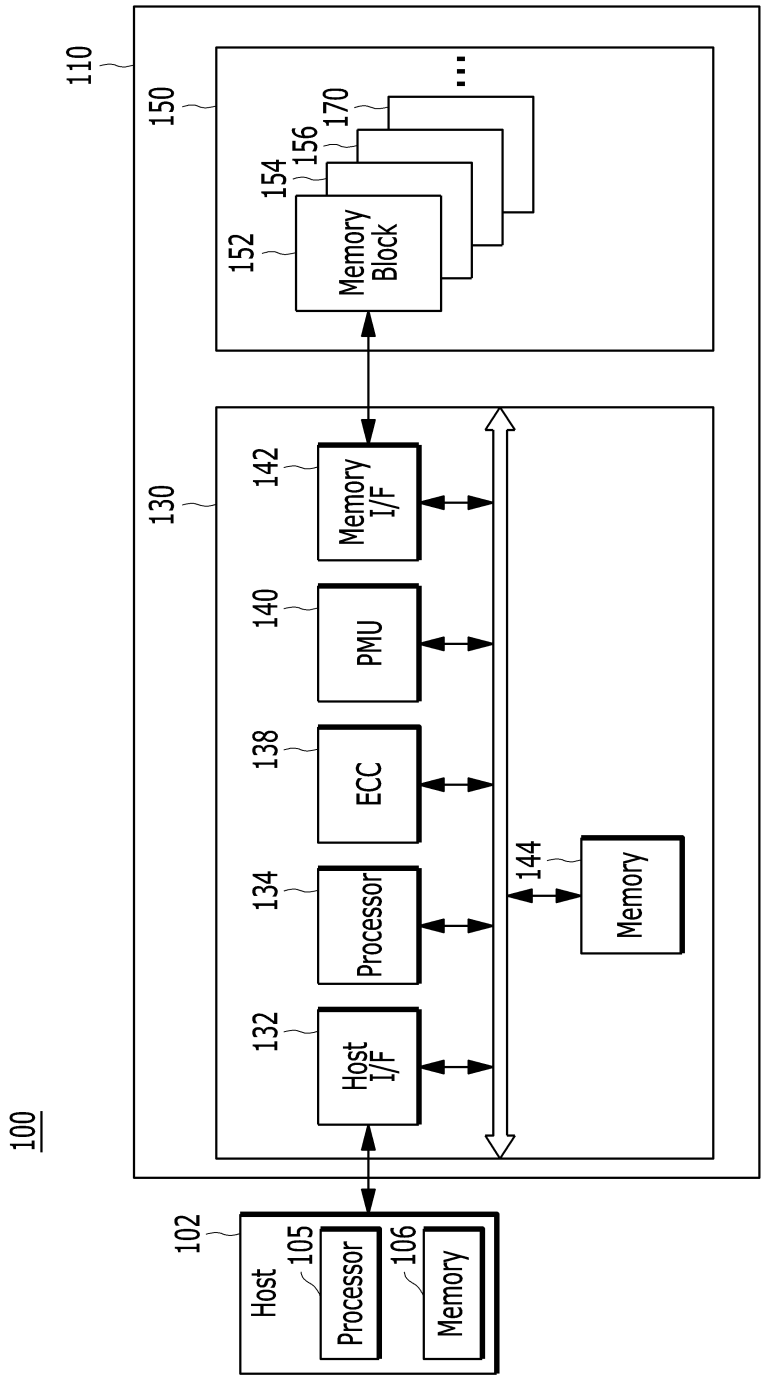

100
110
150
152
Memory Block
154
156
170
130
142
Memory I/F
140
PMU
138
ECC
134
Processor
132
Host I/F
144
Memory
102
Host
105
Processor
106
Memory

FIG. 2

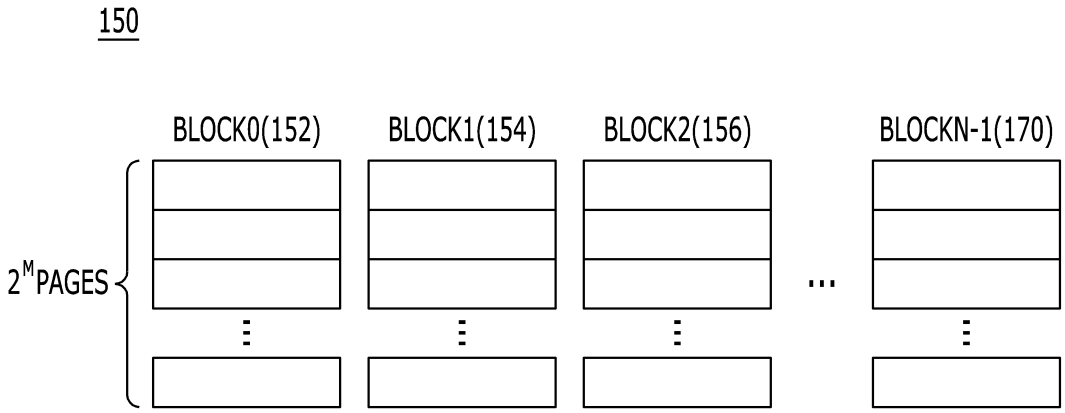


FIG. 3

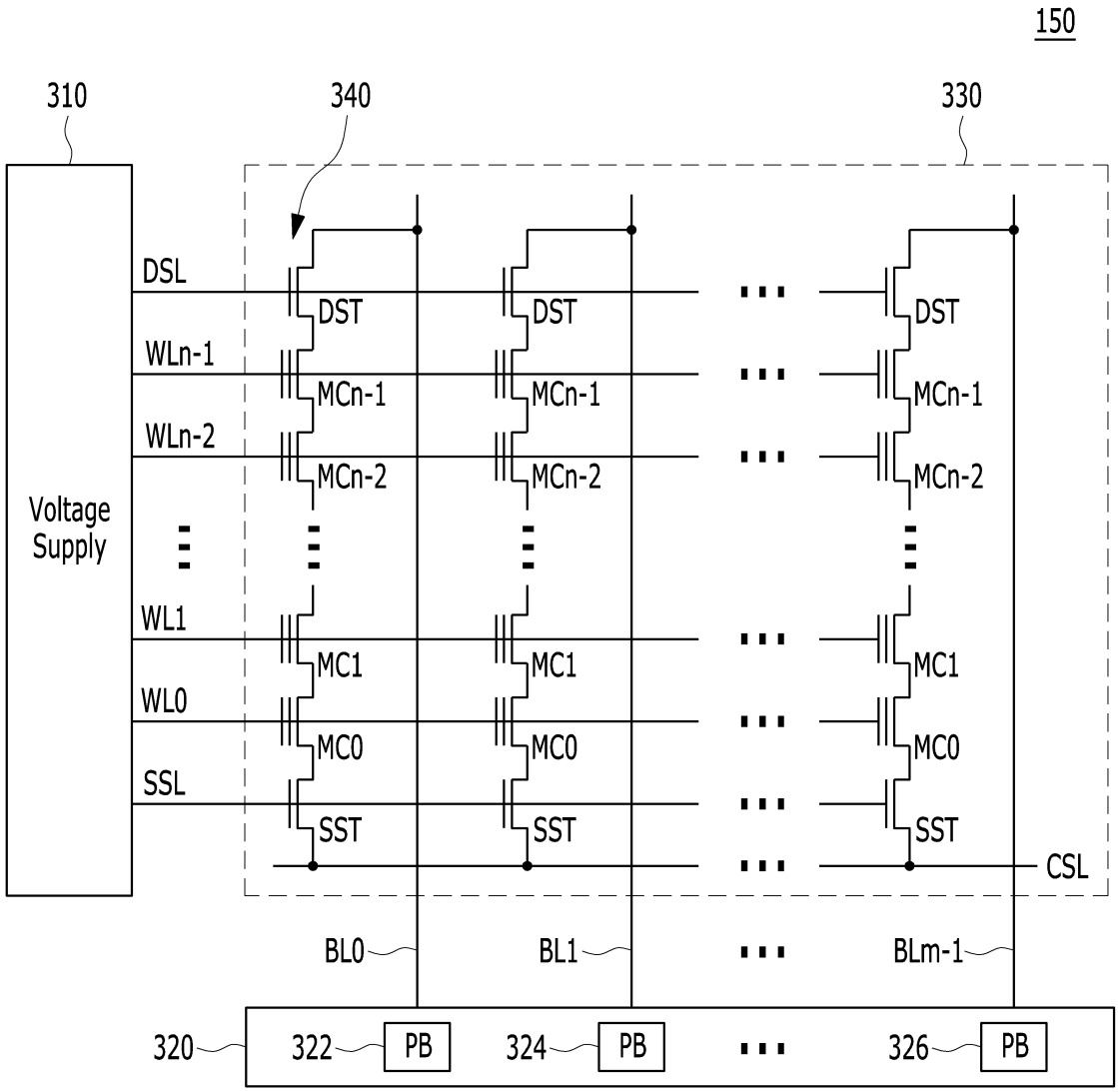

150
310
340
330
Voltage Supply
DSL
WLn-1
WLn-2
WL1
WL0
SSL
DST
MCn-1
MCn-2
MC1
MC0
SST
CSL
BL0
BL1
BLm-1
320
322
324
326
PB

FIG. 4

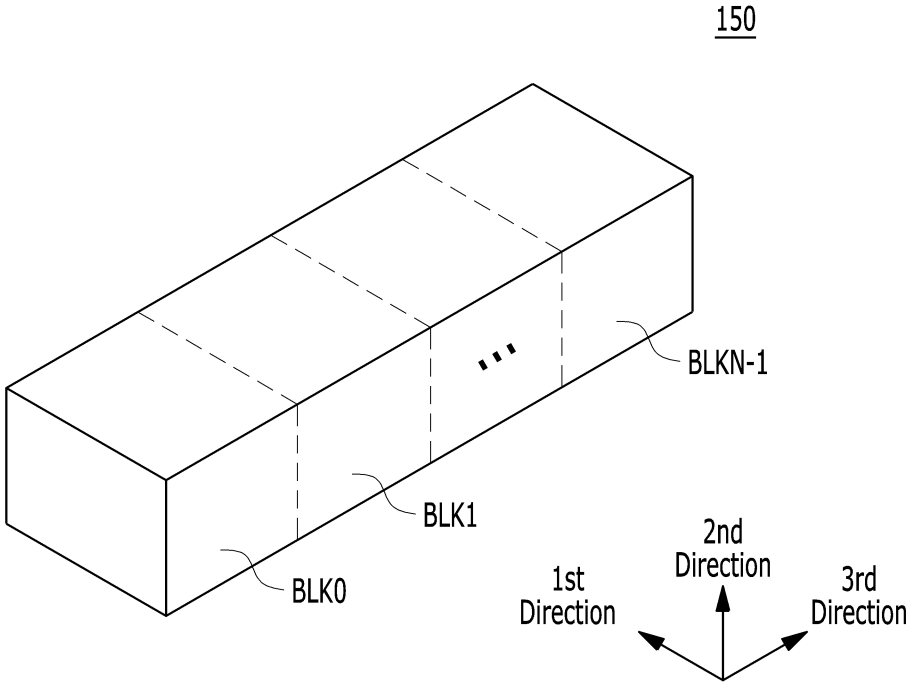

150
BLKN-1
BLK1
BLK0
2nd
Direction
1st
Direction
3rd
Direction

FIG. 5

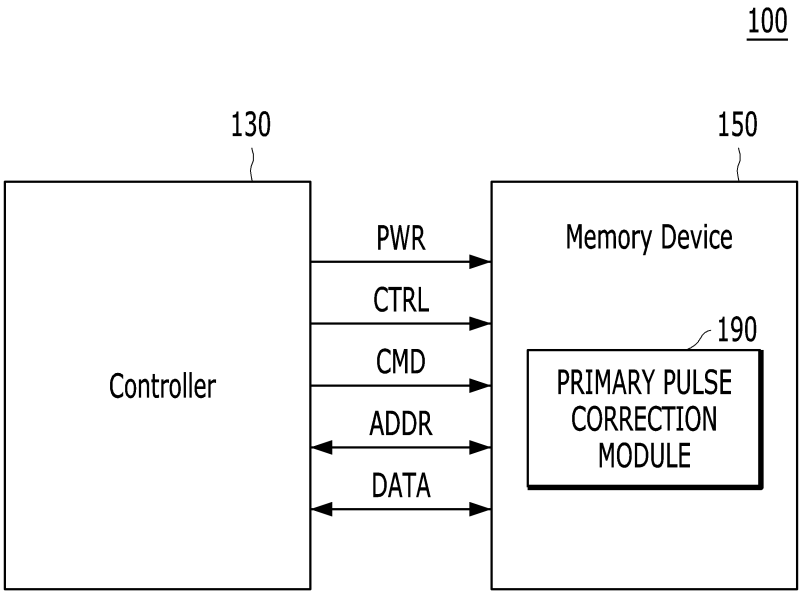

100
130
150
Controller
PWR
CTRL
CMD
ADDR
DATA
Memory Device
190
PRIMARY PULSE
CORRECTION
MODULE

FIG. 6

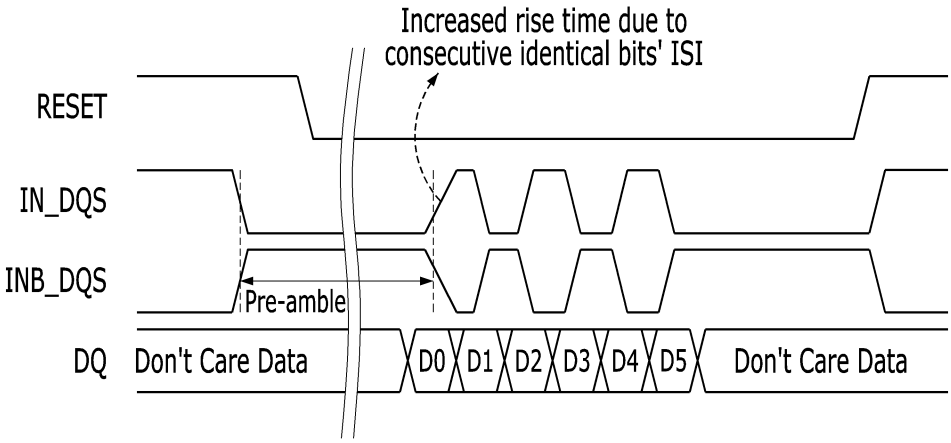

Increased rise time due to
consecutive identical bits' ISI
RESET
IN_DQS
INB_DQS
Pre-amble
DQ
Don't Care Data
D0
D1
D2
D3
D4
D5
Don't Care Data

FIG. 7

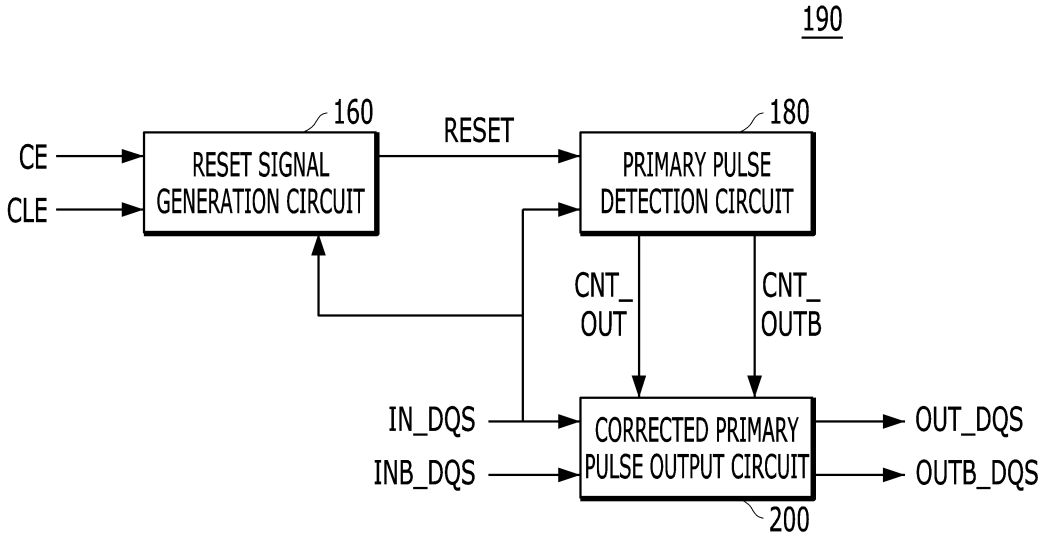

190
160
RESET
180
CE
CLE
RESET SIGNAL
GENERATION CIRCUIT
PRIMARY PULSE
DETECTION CIRCUIT
CNT_
OUT
CNT_
OUTB
IN_DQS
INB_DQS
CORRECTED PRIMARY
PULSE OUTPUT CIRCUIT
OUT_DQS
OUTB_DQS
200

FIG. 8

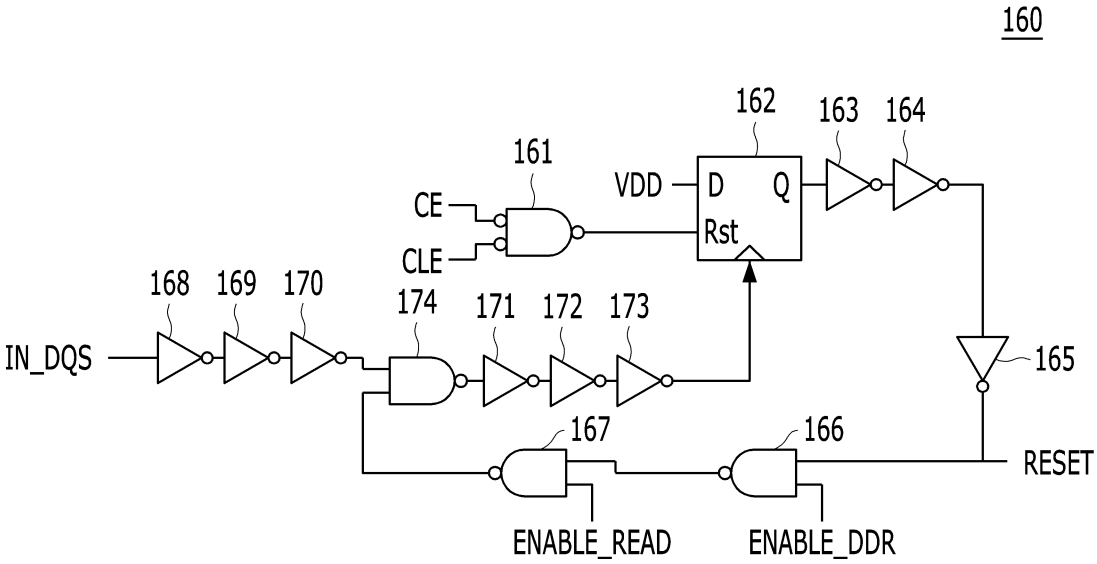

160
162
163
164
161
VDD
D
Q
CE
Rst
CLE
168
169
170
174
171
172
173
165
IN_DQS
167
166
RESET
ENABLE_READ
ENABLE_DDR

FIG. 9

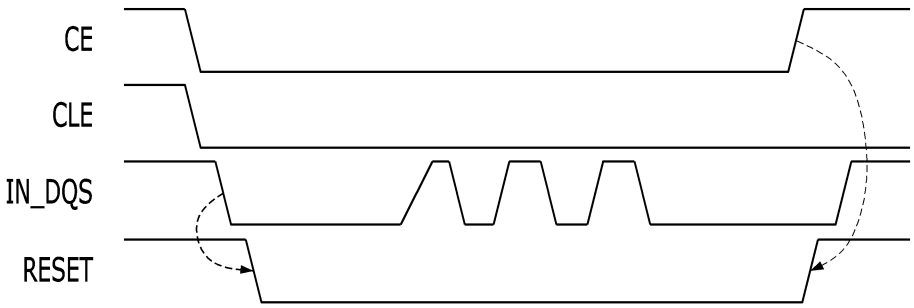

CE
CLE
IN_DQS
RESET

FIG. 10

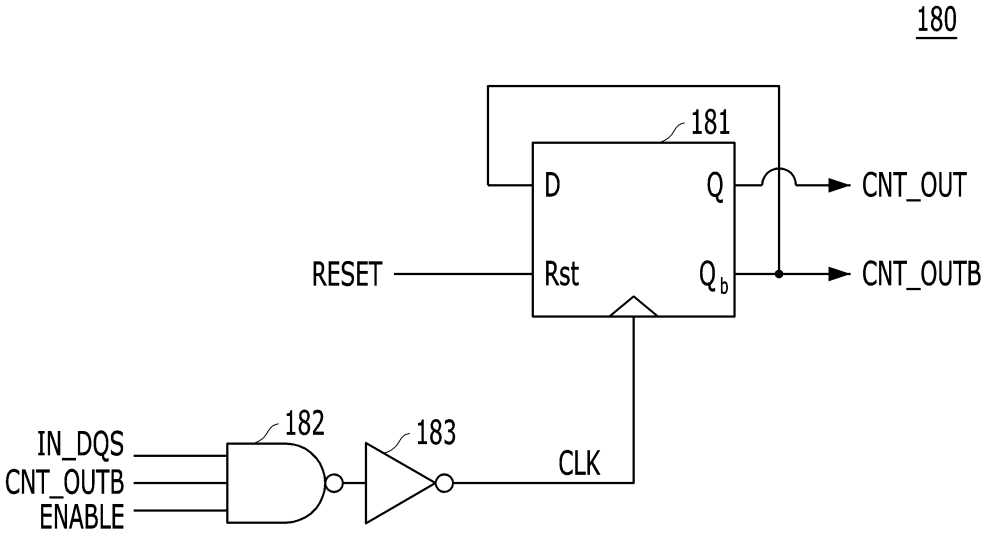

180
181
D
Q
CNT_OUT
RESET
Rst
Q_b
CNT_OUTB
182
183
IN_DQS
CNT_OUTB
ENABLE
CLK

FIG. 11

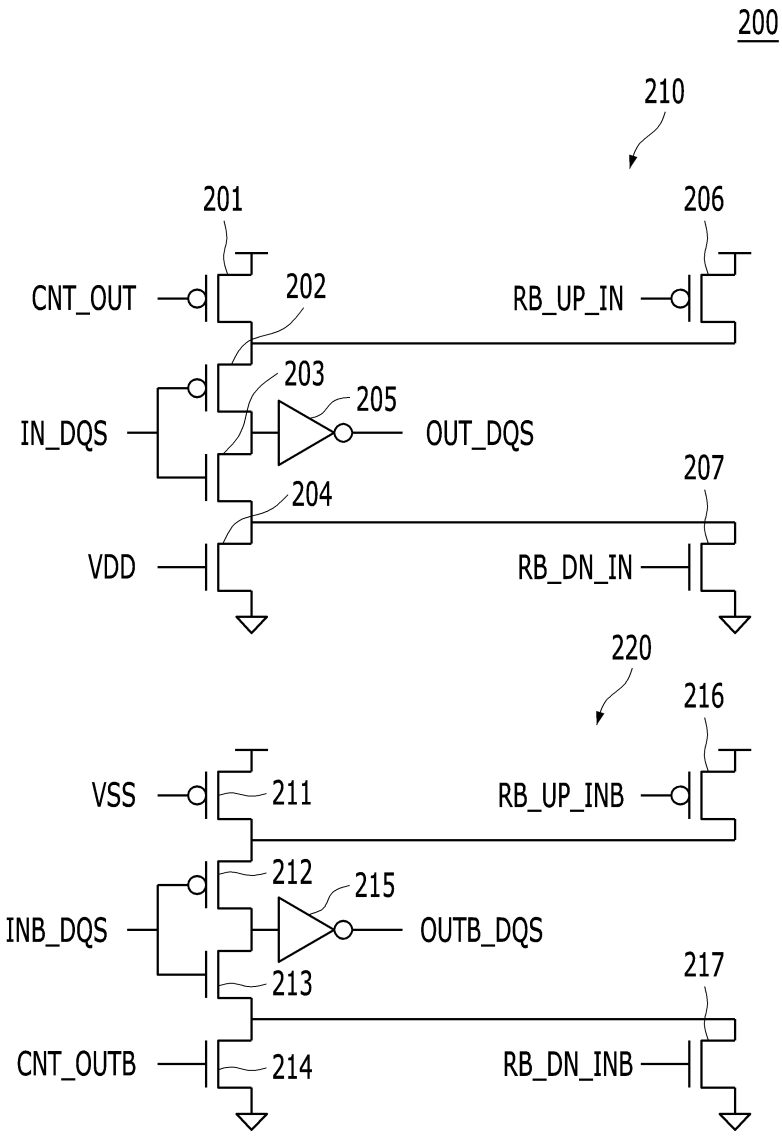

200
210
201
206
CNT_OUT
202
RB_UP_IN
203
205
IN_DQS
OUT_DQS
207
204
VDD
RB_DN_IN
220
216
VSS
211
RB_UP_INB
212
215
INB_DQS
OUTB_DQS
217
213
CNT_OUTB
214
RB_DN_INB

FIG. 12

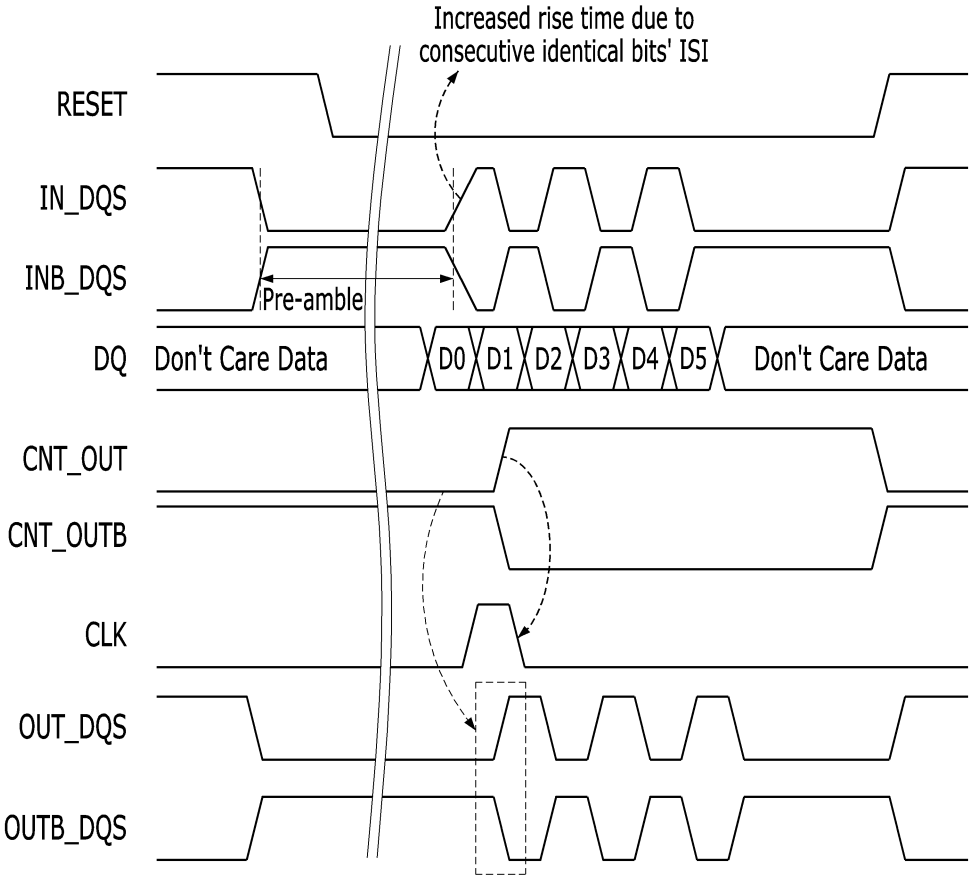

Increased rise time due to
consecutive identical bits' ISI
RESET
IN_DQS
INB_DQS
Pre-amble
DQ
Don't Care Data
D0
D1
D2
D3
D4
D5
Don't Care Data
CNT_OUT
CNT_OUTB
CLK
OUT_DQS
OUTB_DQS

FIG. 13

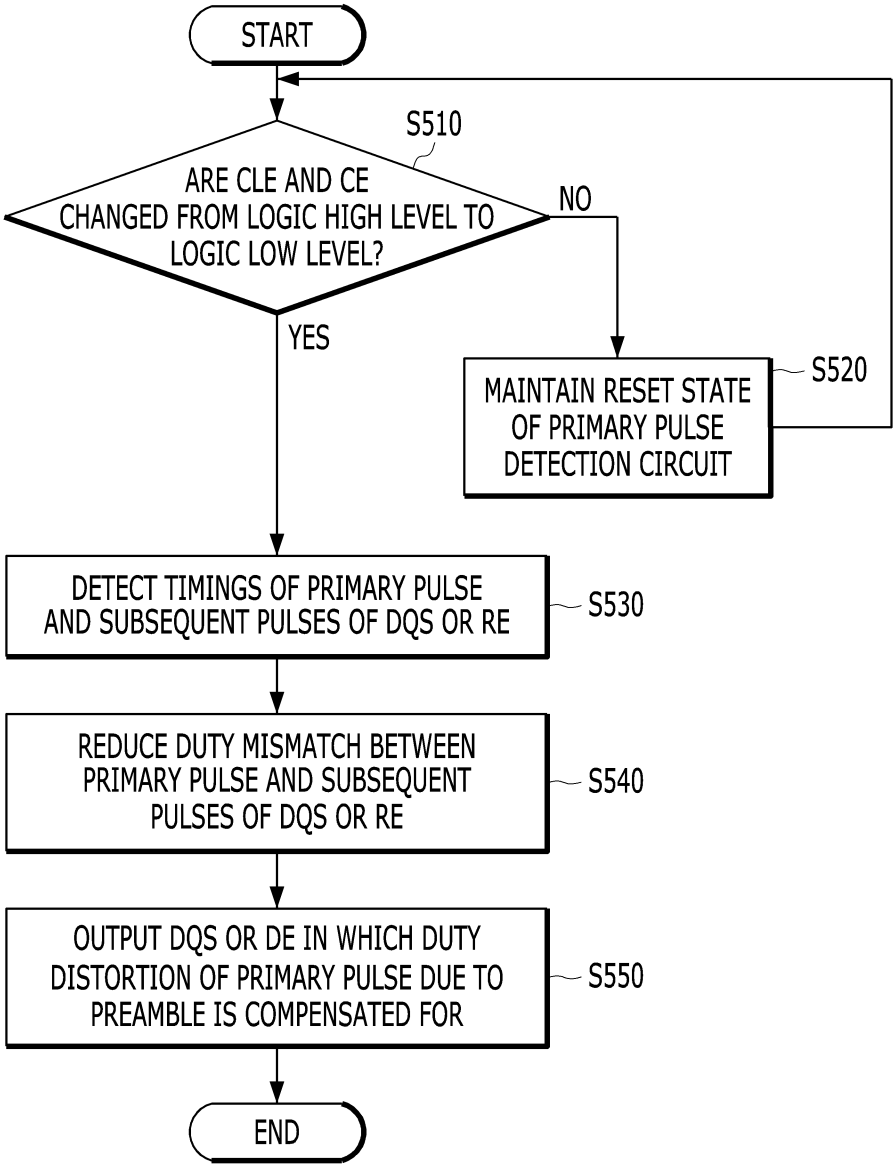
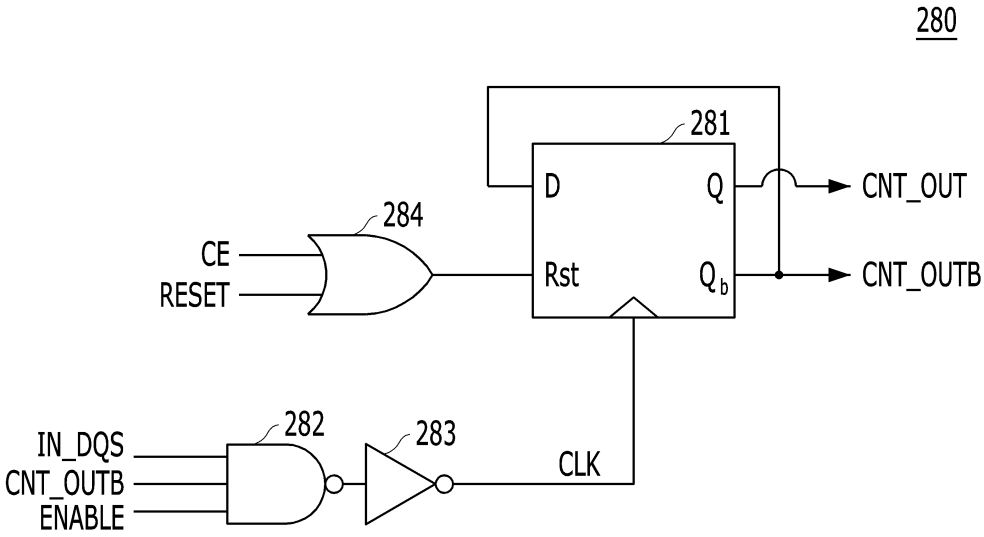

START
S510
ARE CLE AND CE CHANGED FROM LOGIC HIGH LEVEL TO LOGIC LOW LEVEL?
NO
YES
MAINTAIN RESET STATE OF PRIMARY PULSE DETECTION CIRCUIT
S520
DETECT TIMINGS OF PRIMARY PULSE AND SUBSEQUENT PULSES OF DQS OR RE
S530
REDUCE DUTY MISMATCH BETWEEN PRIMARY PULSE AND SUBSEQUENT PULSES OF DQS OR RE
S540
OUTPUT DQS OR DE IN WHICH DUTY DISTORTION OF PRIMARY PULSE DUE TO PREAMBLE IS COMPENSATED FOR
S550
END

FIG. 14


280
281
D
Q
CNT_OUT
284
CE
RESET
Rst
Qb
CNT_OUTB
282
283
IN_DQS
CNT_OUTB
ENABLE
CLK