A METHOD TO IMPROVE SHALLOW TRENCH ISOLATION PERFORMANCE

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The present invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of forming planarized shallow trench isolation (STI) in the fabrication of integrated circuits.

(2) DESCRIPTION OF THE PRIOR ART

As device technology is scaled down to the quarter micron regime, the use of the conventional local oxidation of silicon (LOCOS) isolation will be confined by smaller channel-width encroachment (bird's beak). Shallow trench isolation (STI) can be used to eliminate these encroachments, especially in ultra large scale integrated (ULSI) circuit devices.

However, in forming shallow trench isolation regions, after the trench has been filled, the removal of the pad oxide also results in the removal of the corner regions of the shallow trench isolation (STI) region, as shown in Fig. 1. STI region 20 formed in the semiconductor substrate

10 has had its corners removed as shown by 25 in the figure. This results in a wraparound corner or abrupt transition between the active region and the isolation region. Also, this results in subthreshold humps in the MOS transistors formed in the active regions. The subthreshold hump is an abnormal MOS device I_{DS} - V_{GS} curve caused by a parasitic top corner transistor due to the trench top corner wraparound.

A number of patents have addressed the formation of shallow trenches. U.S. Patent 5,258,332 to Horioka et al teaches etching away a portion of the silicon oxide layer at the edge of a trench and then using chemical dry etching to round the upper and lower corners of the trench. U.S. Patents 5,578,518 to Koike et al teaches isotropically etching the silicon oxide at the edge of a trench so that the liner oxide will form rounded corners of the trench. U.S. Patent 5,554,256 to Pruijmboom et al etches a silicon nitride layer isotropically and then forms a trench wherein the dielectric filling the trench extends over the edge of the substrate to protect it from dopant penetration from an overlying polysilicon layer. U.S. Patent 5,229,316 to Lee et al discloses trench filling above the surface of a substrate and then planarizing the trench filling to the surface.

SUMMARY OF THE INVENTION

Accordingly, the primary object of the invention is to provide a process for forming shallow trench isolation in the fabrication of integrated circuits.

A further object of the invention is to provide a process for forming shallow trench isolation in which there is a smooth transition between active areas and the isolation region.

Still another object is to provide a process for forming shallow trench isolation wherein the critical dimension of the nitride line is less than the critical dimension of the silicon line.

In accordance with the objects of the invention, a method for forming shallow trench isolation having a smooth transition between active areas and isolation regions is achieved. A pad oxide layer is deposited on the surface of a semiconductor substrate. A nitride layer is deposited overlying the pad oxide layer. The nitride layer and pad oxide layer are etched through where they are not covered by a mask to provide openings where the surface of the semiconductor substrate is exposed. A trench is etched

into the semiconductor substrate where it is exposed within the opening. A liner oxide is grown within the trench. Thereafter, the nitride layer is isotropically etched away from the edges of the trench. An oxide layer is deposited overlying the nitride layer and filling the trench wherein the oxide layer filling the trench forms a shallow trench isolation region. The oxide layer is polished away with a polish stop at the nitride layer. The nitride layer is removed. The pad oxide layer is removed whereby the corners of the oxide layer within the trench are rounded completing formation of the shallow trench isolation region in the fabrication of an integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 is a cross-sectional representation of an embodiment of the prior art.

Figs. 2 through 10 are cross-sectional representations of a preferred embodiment of the present invention.

Fig. 11 is a cross-sectional representation of a completed integrated circuit device fabricated by the process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to Fig. 2, there is shown a semiconductor substrate 10. A layer of pad silicon oxide 12 is grown on the surface of the semiconductor substrate to a thickness of between about 50 and 200 Angstroms. A layer of silicon nitride 14 is deposited over the pad oxide layer 12 to a thickness of between about 1000 and 2000 Angstroms.

A photoresist mask 18 is formed over the surface of the nitride layer with an opening 19 where the shallow trench isolation region is to be formed. Using conventional photolithography and etching techniques, the nitride and pad oxide layers are etched to expose the semiconductor substrate where the isolation region is to be formed, as shown in Fig. 3. The photoresist mask is removed.

Referring now to Fig. 4, using the silicon nitride as a hard mask, the semiconductor substrate exposed within the opening is etched into to a depth of between about

2000 and 5000 Angstroms to form a trench 22.

A layer of liner oxide 24 is grown within the trench 22 by thermal oxidation to a thickness of between about 50 and 200 Angstroms, as shown in Fig. 5.

Before the liner oxidation, the critical dimension of the nitride line is equal to the critical dimension of the silicon line. After liner oxidation, the critical dimension of the nitride line is greater than the critical dimension of the silicon line because the thermal oxidation causes silicon consumption where $Si + O_2 = SiO_2$.

As illustrated in Fig. 6, the silicon nitride layer 14 is isotropically etched away from the edges of the trench to a distance of about 200 to 500 Angstroms from the trench edge. This key isotropic etching is performed using a chemical dry etch (CDE) using fluorine-based chemistry at a high pressure of between about 500 and 5000 mTorr. In this method, the vertical and lateral etch rates are almost the same.

During the isotropic etching, the critical dimension of the silicon is unaffected. The liner oxide protects the silicon from etching. The etch rate ratio of

nitride to oxide is about 9-20 to 1. After isotropic etching, the critical dimension of the nitride line is less than the critical dimension of the silicon. The critical dimension of the nitride line is reduced by the isotropic etch of the present invention which reduces the silicon nitride thickness and width simultaneously. The high silicon nitride to oxide selectivity keeps the oxide almost entirely intact thereby protecting the underlying silicon from being etched. The critical dimension difference between the silicon nitride and the silicon provides the lateral distance from the silicon nitride edge to the silicon edge. After gap filling and silicon nitride removal, this difference will balance the silicon dioxide loss during the subsequent silicon dioxide strip step and thus provide a wraparound-free trench.

Referring now to Fig. 7, an oxide layer 30 is deposited by CVD over the surface of the substrate and filling the trench. The oxide layer 30 has a thickness of between about 4000 and 8000 Angstroms.

The oxide layer 30 is now polished using CMP with a polish stop at the nitride layer 14, as illustrated in Fig. 8.

Referring to Fig. 9, the silicon nitride layer 14 is removed using a conventional wet etch, such as hydrofluoric acid (HF) dip and H_3PO_4 strip.

Next, the pad oxide 12 is removed. Because the oxide 30 extends partially over the surface of the pad oxide layer at the edges of the trench, the corners of the oxide 30 within the trench are not etched away, as in Fig. 1 of the prior art. Instead, the corners of the oxide 30 within the trench are slightly rounded, allowing for a smooth transition between the STI region and the active regions, as shown in Fig. 10.

Processing continues as is conventional in the art. For example, polysilicon layer 32 is deposited over the surface of the substrate as shown in Fig. 10. The polysilicon layer is patterned to form gate electrodes 34. Source and drain regions 36 may be formed in the active regions between isolation regions as is conventional in the art. Electrical contacts 40 may be made through dielectric isolation layer 38, as shown in Fig. 11.

The process of the present invention results in the formation of shallow trench isolation (STI) having a smooth transition between the isolation region and active

regions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. A method of forming shallow trench isolation in the fabrication of an integrated circuit device comprising:

depositing a pad oxide layer on the surface of a semiconductor substrate;

depositing a nitride layer overlying said pad oxide layer;

etching through said nitride layer and said pad oxide layer where they are not covered by a mask to provide an opening wherein the surface of said semiconductor substrate is exposed;

etching a trench into said semiconductor substrate where it is exposed within said opening;

growing a thermal oxide liner within said trench;

thereafter, isotropically etching said nitride layer away from the edges of said trench;

depositing an oxide layer overlying said nitride layer and filling said trench;

polishing away said oxide layer with a polish stop at said nitride layer;

removing said nitride layer; and

removing said pad oxide layer whereby the corners of said oxide layer within said trench are rounded completing said formation of said shallow trench isolation in said fabrication of said integrated circuit device.

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2. The method according to Claim 1 wherein said pad oxide layer has a thickness of between about 50 and 200 Angstroms.

3. The method according to Claim 1 wherein said nitride layer is deposited to a thickness of between about 1000 and 2000 Angstroms.

4. The method according to Claim 1 wherein said trench has a depth of between about 2000 and 5000 Angstroms.

5. The method according to Claim 1 wherein said thermal oxide liner has a thickness of between about 50 and 200 Angstroms.

6. The method according to Claim 1 wherein said step of isotropically etching said nitride layer is performed using a chemical dry etch using fluorine-based chemistry.

7. The method according to Claim 1 wherein said step of isotropically etching said nitride layer comprises etching away said nitride layer to a distance of between about 200 and 500 Angstroms from the edge of said trench.



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8. The method according to Claim 1 wherein said oxide layer is deposited by low pressure chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

9. The method according to Claim 1 wherein said step of polishing away said oxide layer comprises chemical mechanical polishing (CMP).

10. The method according to Claim 1 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said shallow trench isolation.

11. A method of forming shallow trench isolation in the fabrication of an integrated circuit device comprising:

depositing a pad oxide layer on the surface of a semiconductor substrate;

depositing a nitride layer overlying said pad oxide layer;

etching through said nitride layer and said pad oxide layer where they are not covered by a mask to provide an opening wherein the surface of said semiconductor substrate is exposed;

etching a trench into said semiconductor substrate



where it is exposed within said opening;

growing a thermal oxide liner within said trench;

thereafter, isotropically dry etching said nitride layer away from the edges of said trench;

depositing an oxide layer overlying said nitride layer and filling said trench;

polishing away said oxide layer with a polish stop at said nitride layer wherein said oxide layer extends above the surface of said substrate;

removing said nitride layer; and

removing said pad oxide layer whereby the corners of said oxide layer within said trench are rounded completing said formation of said shallow trench isolation in said fabrication of said integrated circuit device.

12. The method according to Claim 11 wherein said pad oxide layer has a thickness of between about 50 and 200 Angstroms.

13. The method according to Claim 11 wherein said nitride layer is deposited to a thickness of between about 1000 and 2000 Angstroms.



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14. The method according to Claim 11 wherein said trench has a depth of between about 2000 and 5000 Angstroms.

15. The method according to Claim 11 wherein said thermal oxide liner has a thickness of between about 50 and 200 Angstroms.

16. The method according to Claim 11 wherein said step of isotropically etching said nitride layer is performed using a chemical dry etch having fluorine-based chemistry.

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17. The method according to Claim 11 wherein said step of isotropically etching said nitride layer comprises etching away said nitride layer to a distance of between about 200 and 500 Angstroms from the edge of said trench.

18. The method according to Claim 11 wherein said oxide layer is deposited by low pressure chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

19. The method according to Claim 11 wherein said step of polishing away said oxide layer comprises chemical



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mechanical polishing (CMP).

20. The method according to Claim 11 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said shallow trench isolation.

21. A method of forming shallow trench isolation in the fabrication of an integrated circuit device comprising:

depositing a pad oxide layer on the surface of a semiconductor substrate;

depositing a silicon nitride layer overlying said pad oxide layer;

etching through said silicon nitride layer and said pad oxide layer where they are not covered by a mask to provide an opening wherein the surface of said semiconductor substrate is exposed;

etching a trench into said semiconductor substrate where it is exposed within said opening;

growing a thermal oxide liner within said trench;

thereafter, isotropically dry etching said silicon nitride layer to a distance of between about 200 and 500 Angstroms away from the edges of said trench;

depositing an oxide layer overlying said silicon

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nitride layer and filling said trench;

polishing away said oxide layer with a polish stop at said silicon nitride layer wherein said oxide layer extends above the surface of said substrate;

removing said silicon nitride layer; and

removing said pad oxide layer whereby the corners of said oxide layer within said trench are rounded completing said formation of said shallow trench isolation in said fabrication of said integrated circuit device.

22. The method according to Claim 21 wherein said nitride layer is deposited to a thickness of between about 1000 and 2000 Angstroms.

23. The method according to Claim 21 wherein said step of isotropically etching said nitride layer is performed using a chemical dry etch having fluorine-based chemistry.

24. The method according to Claim 21 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said shallow trench isolation.

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ABSTRACT

A METHOD TO IMPROVE SHALLOW TRENCH ISOLATION PERFORMANCE

A new method for forming shallow trench isolation having a smooth transition between active areas and isolation regions is described. A pad oxide layer is deposited on the surface of a semiconductor substrate. A nitride layer is deposited overlying the pad oxide layer. The nitride layer and pad oxide layer are etched through where they are not covered by a mask to provide openings where the surface of the semiconductor substrate is exposed. A trench is etched into the semiconductor substrate where it is exposed within the opening. A liner oxide is grown within the trench. Thereafter, the nitride layer is isotropically etched away from the edges of the trench. An oxide layer is deposited overlying the nitride layer and filling the trench wherein the oxide layer filling the trench forms a shallow trench isolation region. The oxide layer is polished away with a polish stop at the nitride layer. The nitride layer is removed. The pad oxide layer is removed whereby the corners of the oxide layer within the trench are rounded completing formation of the shallow trench isolation region in the fabrication of an integrated circuit device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)

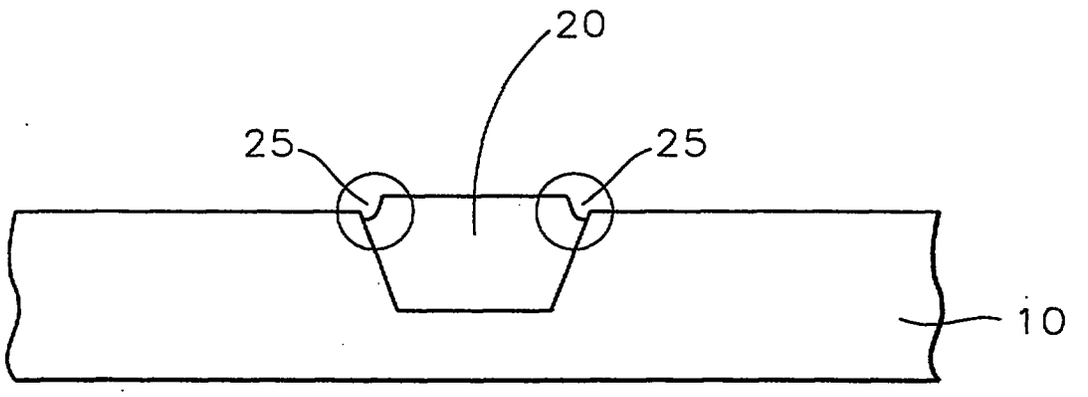


FIG. 1

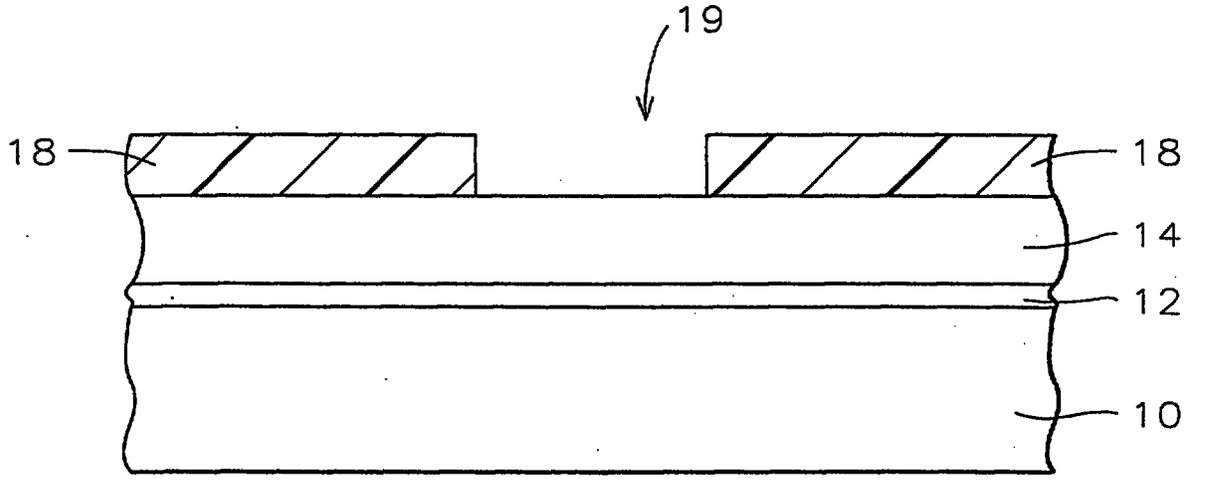


FIG. 2

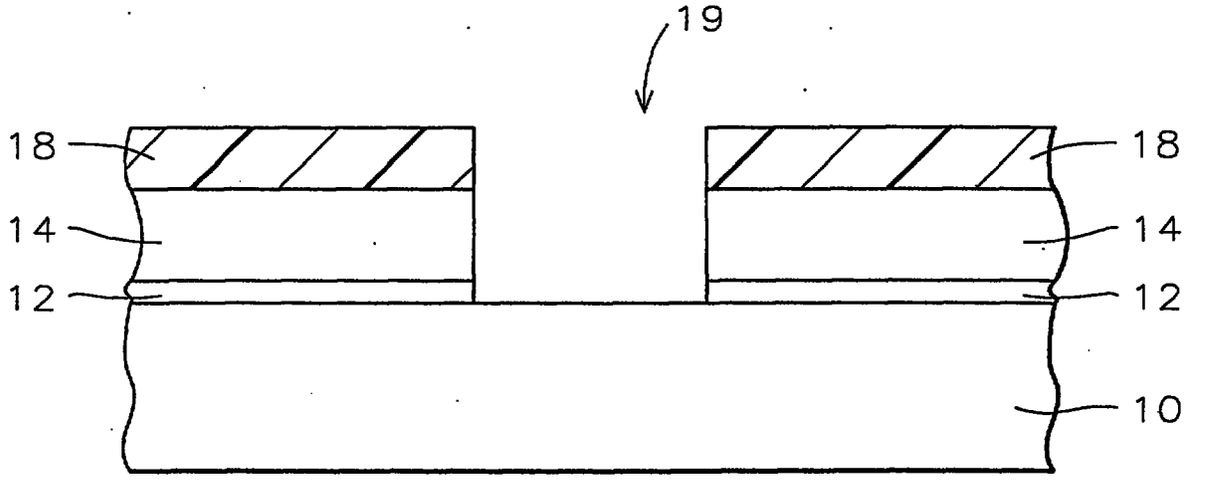


FIG. 3

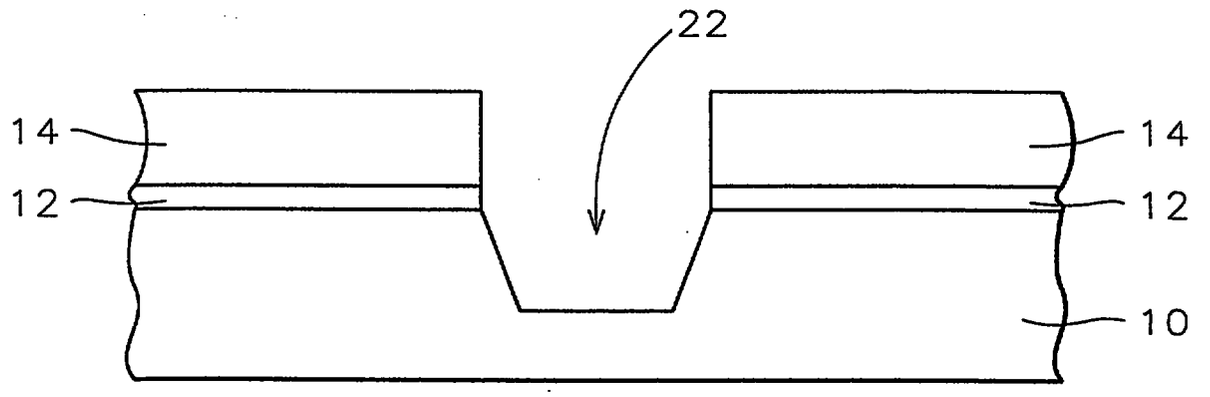


FIG. 4

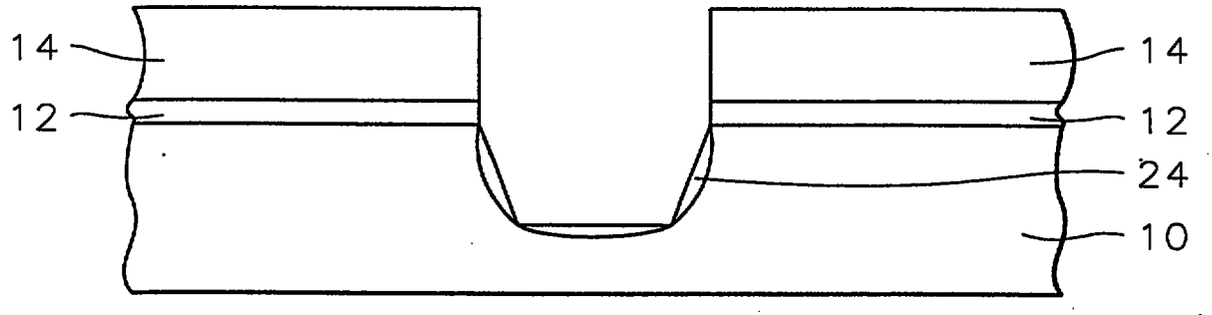


FIG. 5

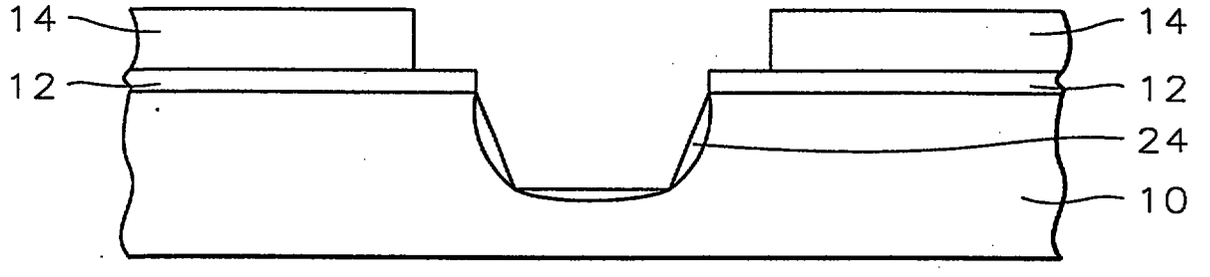


FIG. 6

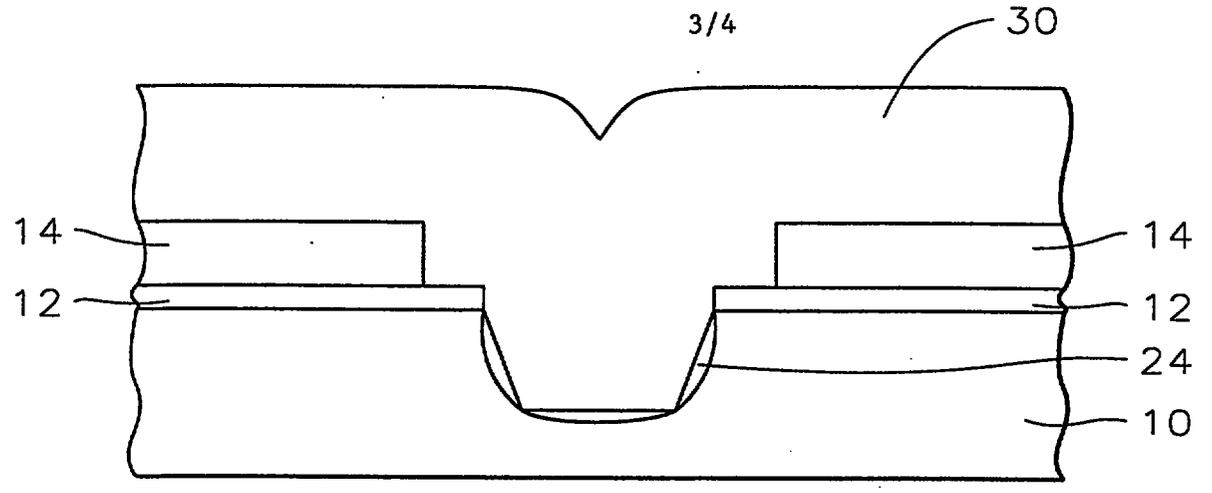


FIG. 7

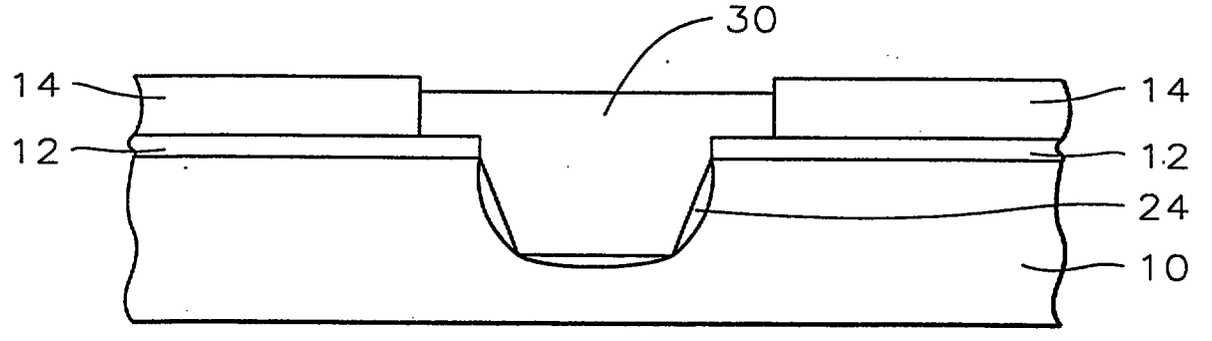


FIG. 8

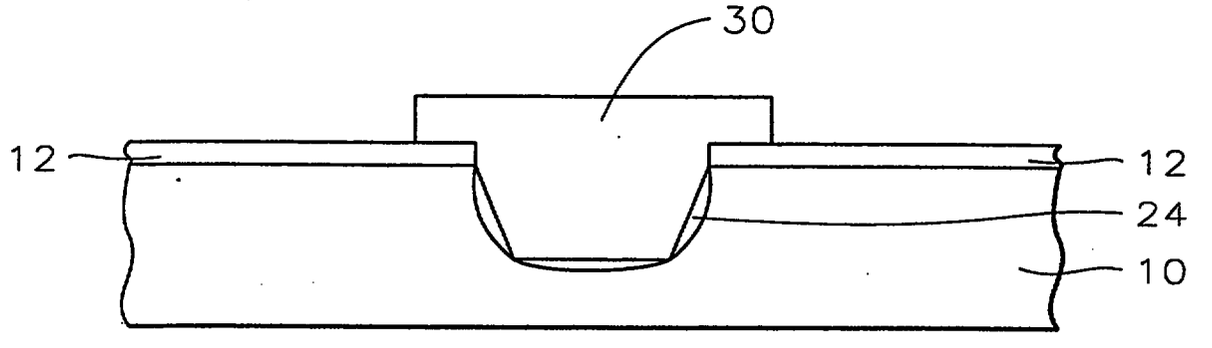


FIG. 9

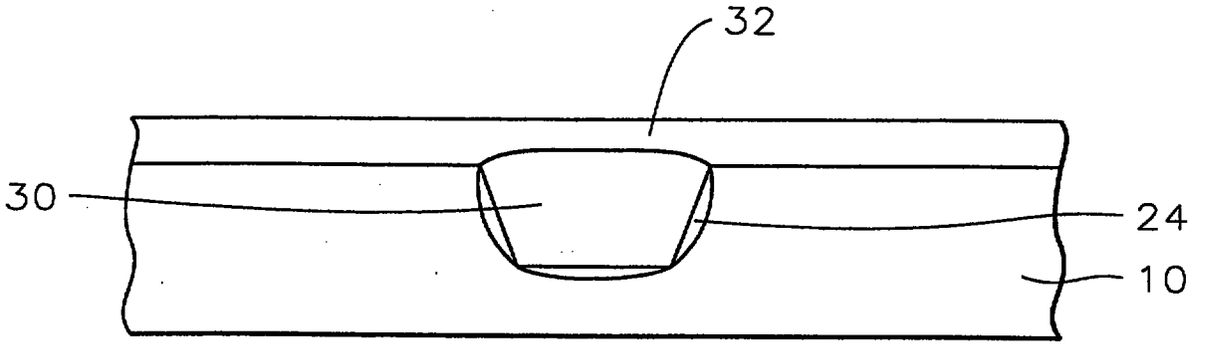


FIG. 10

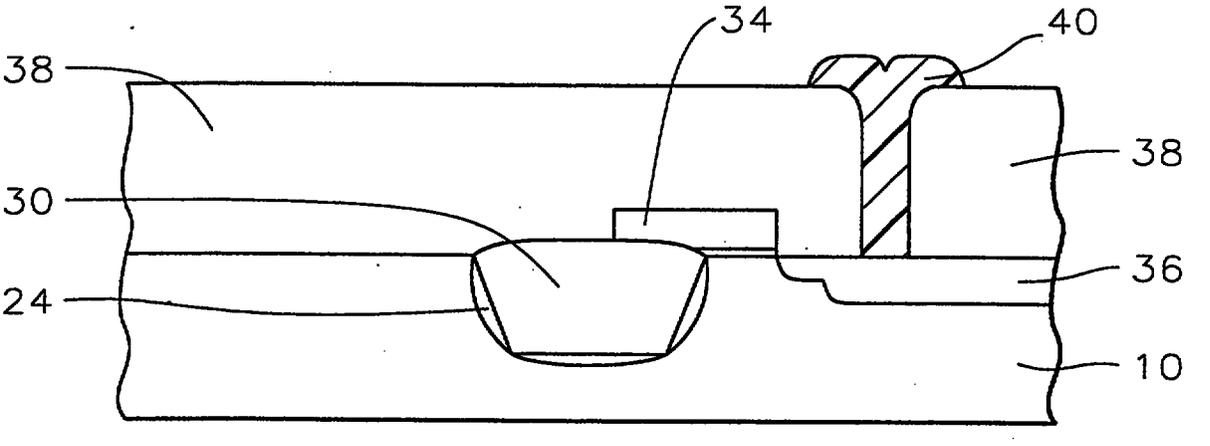


FIG. 11

REPLACEMENT SHEET
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CLAIMS

1. A method of forming shallow trench isolation in the fabrication of an integrated circuit device comprising:

depositing a pad oxide layer on the surface of a semiconductor substrate;

depositing a nitride layer overlying said pad oxide layer;

etching through said nitride layer and said pad oxide layer where they are not covered by a mask to provide an opening wherein the surface of said semiconductor substrate is exposed;

etching a trench into said semiconductor substrate where it is exposed within said opening using said nitride layer as a mask;

growing a thermal oxide liner within said trench;

thereafter, isotropically etching said nitride layer away from the edges of said trench;

depositing an oxide layer overlying said nitride layer and filling said trench;

polishing away said oxide layer with a polish stop at said nitride layer;

removing said nitride layer; and

removing said pad oxide layer whereby the corners of said oxide layer within said trench are rounded completing said formation of said shallow trench isolation in said fabrication of said integrated circuit device.

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2. The method according to Claim 1 wherein said pad oxide layer has a thickness of between about 50 and 200 Angstroms.

3. The method according to Claim 1 wherein said nitride layer is deposited to a thickness of between about 1000 and 2000 Angstroms.

4. The method according to Claim 1 wherein said trench has a depth of between about 2000 and 5000 Angstroms.

5. The method according to Claim 1 wherein said thermal oxide liner has a thickness of between about 50 and 200 Angstroms.

6. The method according to Claim 1 wherein said step of isotropically etching said nitride layer is performed using a chemical dry etch using fluorine-based chemistry.

7. The method according to Claim 1 wherein said step of isotropically etching said nitride layer comprises etching away said nitride layer to a distance of between about 200 and 500 Angstroms from the edge of said trench.



8. The method according to Claim 1 wherein said oxide layer is deposited by low pressure chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

9. The method according to Claim 1 wherein said step of polishing away said oxide layer comprises chemical mechanical polishing (CMP).

10. The method according to Claim 1 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said shallow trench isolation.

11. A method of forming shallow trench isolation in the fabrication of an integrated circuit device comprising:

depositing a pad oxide layer on the surface of a semiconductor substrate;

depositing a nitride layer overlying said pad oxide layer;

etching through said nitride layer and said pad oxide layer where they are not covered by a mask to provide an opening wherein the surface of said semiconductor substrate is exposed;

etching a trench into said semiconductor substrate

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using said nitride as a mask where it is exposed within said opening;

growing a thermal oxide liner within said trench;

thereafter, isotropically dry etching said nitride layer away from the edges of said trench;

depositing an oxide layer overlying said nitride layer and filling said trench;

polishing away said oxide layer with a polish stop at said nitride layer wherein said oxide layer extends above the surface of said substrate;

removing said nitride layer; and

removing said pad oxide layer whereby the corners of said oxide layer within said trench are rounded and wherein said oxide layer within said trench does not extend laterally over the surface of said substrate thereby completing said formation of said shallow trench isolation in said fabrication of said integrated circuit device.

12. The method according to Claim 11 wherein said pad oxide layer has a thickness of between about 50 and 200 Angstroms.

13. The method according to Claim 11 wherein said nitride layer is deposited to a thickness of between about 1000 and 2000 Angstroms.

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14. The method according to Claim 11 wherein said trench has a depth of between about 2000 and 5000 Angstroms.

15. The method according to Claim 11 wherein said thermal oxide liner has a thickness of between about 50 and 200 Angstroms.

16. The method according to Claim 11 wherein said step of isotropically etching said nitride layer is performed using a chemical dry etch having fluorine-based chemistry.

17. The method according to Claim 11 wherein said step of isotropically etching said nitride layer comprises etching away said nitride layer to a distance of between about 200 and 500 Angstroms from the edge of said trench.

18. The method according to Claim 11 wherein said oxide layer is deposited by low pressure chemical vapor deposition to a thickness of between about 4000 and 8000 Angstroms.

19. The method according to Claim 11 wherein said step of polishing away said oxide layer comprises chemical

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mechanical polishing (CMP).

20. The method according to Claim 11 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said shallow trench isolations.

21. A method of forming shallow trench isolation in the fabrication of an integrated circuit device comprising:

depositing a pad oxide layer on the surface of a semiconductor substrate;

depositing a silicon nitride layer overlying said pad oxide layer;

etching through said silicon nitride layer and said pad oxide layer where they are not covered by a mask to provide an opening wherein the surface of said semiconductor substrate is exposed;

etching a trench into said semiconductor substrate where it is exposed within said opening using said nitride layer as a mask;

growing a thermal oxide liner within said trench;

thereafter, isotropically dry etching said silicon nitride layer to a distance of between about 200 and 500 Angstroms away from the edges of said trench;

depositing an oxide layer overlying said silicon

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nitride layer and filling said trench;

polishing away said oxide layer with a polish stop at said silicon nitride layer wherein said oxide layer and extends outward from said trench distance of between 200 and 500 Angstroms extends above the surface of said substrate; from said edges of said trench

removing said silicon nitride layer; and said oxide layer extending outward from said trench is etched back and removing said pad oxide layer whereby the corners of said oxide layer within said trench are rounded thereby completing said formation of said shallow trench isolation in said fabrication of said integrated circuit device.

22. The method according to Claim 21 wherein said nitride layer is deposited to a thickness of between about 1000 and 2000 Angstroms.

23. The method according to Claim 21 wherein said step of isotropically etching said nitride layer is performed using a chemical dry etch having fluorine-based chemistry.

24. The method according to Claim 21 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said shallow trench isolations.

